SEMIKRON
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Technical Explanation
Rectifier Diodes and Thyristors

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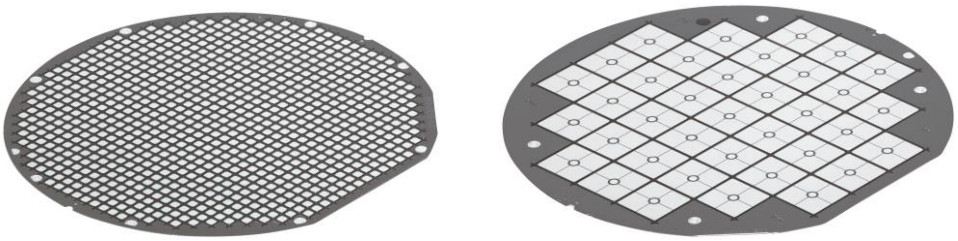
1. Introduction and Scope of Document

SKR/SKN rectifier diodes and SKT thyristors are mainly used in grid-side input rectifier bridge configurations. Depending on the chosen combination of diodes and thyristors, uncontrolled, half-controlled, and fully controlled configurations are possible [2].
SEMIKRON's rectifier diodes and thyristors are designed primarily for the 1600V voltage class, covering a wide range of common line voltages.
Since switching losses are negligible in case of 50/60 Hz operation, the devices are optimized for low forward losses (low V_F and V_T, respectively) and a high intrinsic surge current robustness (I_{FSM}/I_{TSM}).

Figure 1: Product Pictures



Rectifier Diode Wafer (left) and Thyristor Wafer with Center Gate (right)

The scope of this document is mainly to explain the data sheet specifications as well as the required handling of bare die rectifier diodes and thyristors. It alludes to device physics as well as application related knowledge only in a very concise way. For excellent additional information regarding rectifier diodes and thyristors and their use in power electronics, please refer to SEMIKRON's *Application Manual Power Semiconductors* [2].

2. General Considerations Regarding Choice of Diode or Thyristor

The properties of a power rectifier diode or thyristor depend heavily on the assembly and interconnection technology it is used in. Table 1 gives an overview over the existing portfolio for rectifier diodes and thyristors with some basic parameters taken from the bare die data sheets. The specifications given in the bare die data sheet reflect the proven performance in an industry standard power module-like assembly with specific electrical and thermal properties. Moreover, certain characteristics like the maximum repetitive reverse voltage (V_{RRM}) might not be achieved on the non-assembled bare die due to the limited dielectric strength under ambient conditions (i.e. in air).

Table 1: Rectifier Diode and Thyristor Portfolio Overview (status Q3/2015)

Device Type	Voltage Class	T_{jmax}	$I_{F(DC)}$ / $I_{T(DC)}$	I_{FSM} / I_{TSM} @T_{jmax}	Feed Size	Chip Area
Rectifier Diode (SKR/SKN)	1600 V	150°C	25 … 770 A	200 … 9450 A	3.5 … 22.4 mm	12.3 … 502.8 mm^2
Thyristor (SKT) – Center Gate	1600 V	130°C	105 … 480 A	1000 … 8200 A	8.9 … 24.3 mm	79.2 … 590.5 mm^2
Thyristor (SKT) – Corner Gate	1600 V	130°C	60 … 165 A	280 … 1800 A	5.6 … 12.4 mm	31.4 … 153.8 mm^2

Using a different set-up (e.g. altering thermal or electrical properties), different ratings might be reached. Therefore, the nominal or mean forward current $I_{F(DC)}/I_{T(DC)}$ and the surge current rating I_{FSM}/I_{TSM} can only be understood as a guideline for choosing the correct chip size for a given application. In section 3.4, the definition and boundary conditions of these ratings will be explained in more detail.
The fundamental relationship between thermal and electrical properties of a power semiconductor device shall be briefly mentioned here. The (electrical) power loss P_v occurring during operation of a semiconductor device (i.e. heat) needs to be dissipated by means of cooling:

$$P_v = V \cdot I = \frac{T_j - T_s}{R_{th(j-s)}} \qquad (1)$$

The equation shows that the ampacity of a device with given electrical characteristics (and junction temperature T_j) is determined by the heatsink temperature T_s and the thermal resistance R_{th}, which are both primarily given by the assembly.

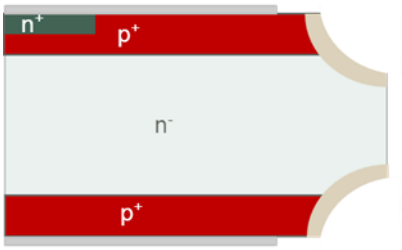
Otherwise, for a setup with fixed T_s and R_{th}, the ampacity is limited by the maximum allowable temperature of the device known as maximum junction temperature T_{jmax}. The higher the maximum junction temperature, the higher the current density/performance of a device is.
It is important to understand that T_{jmax} describes the maximum allowable *local* temperature of any part of the semiconductor device under all conditions which means that a safety margin is required in real-world applications. This safety margin is typically up to 25°C, and sometimes described as maximum operation temperature T_{jop}. It is also the reason why in data sheets, static parameters required for loss calculations are often given at 25°C below T_{jmax}.
To calculate the required chip size for a given power rating, some boundary conditions have to be taken into account. This is rather straight forward for a grid-side rectifier application where dynamic losses can be neglected: only R_{th} and T_s have to be given to calculate a mean forward current of a sinusoidal or DC signal, $I_{F(AV)}$ and $I_{F(DC)}$, respectively. Please refer to [2] for an in-depth coverage.

3. Bare Die Diode/Thyristor Products: Technology and Variants

3.1 Mesa Junction Termination Technology

The diodes and thyristors discussed in this document follow a common device design principle: the termination of the p-n junction at the edge of the chip is implemented by means of the mesa technology. Mesa technology means that a groove or trench modifies the electric field at the discontinuity from bulk to dicing line at the edge of the chip. This is required to optimize the blocking behavior and minimizes the leakage currents.
Figure 2 shows the mesa principle for a thyristor. The edge of the chip is shown on the right hand side, while the active area/bulk of the device is shown on the left hand side. Since a thyristor has two major p-n junctions which need to withstand a high breakdown voltage (forward and reverse direction), a mesa termination has to be implemented on top and bottom side of the chip. This is commonly referred to as double mesa design.
A passivation material is applied to the trench to further optimize the electric behavior, and protecting the surface from environmental influences such as contaminants.

Figure 2: Mesa Junction Termination Principle (Thyristor)



Schematic thyristor cross-section. Chip center/start of active area depicted on the left hand side, chip edge on the right hand side.

The mesa technology has two major advantages. Firstly, the process technology needed is less complex compared to other semiconductor solutions.
Secondly, the required area for the edge termination is smaller than in planar design alternatives. This means that a higher fraction of the total chip area is available for current conduction, leading to smaller chip sizes at a given current rating. This effect is especially pronounced at small chip sizes.

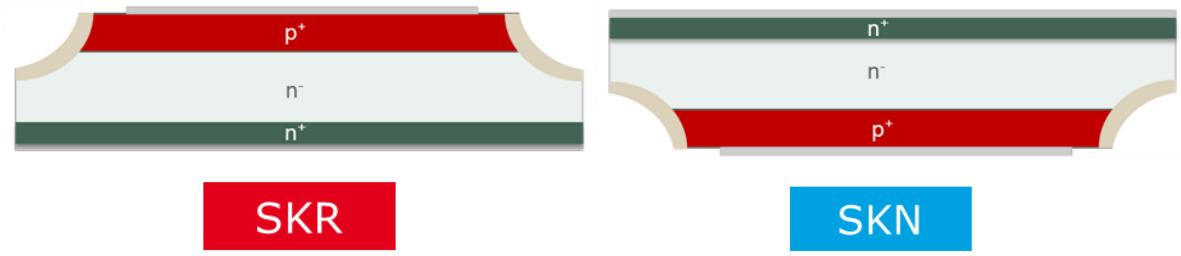
3.2 Options for Rectifier Diodes

Depending on chip size, the standard delivery format of SKR rectifier diodes varies. For feed sizes smaller or equal to 10.3 mm, the diodes are delivered as sawn-on-frame. For chip sizes larger than 10.3 mm, the standard delivery format is waffle pack/tray. Please refer to section 5 for more information on delivery formats and packaging.
In the original mesa design, the anode represents the top contact of the diode while the bottom side is the cathode connection. This configuration is known as "SKR", and represents the majority of the portfolio.
In certain topologies, it can be beneficial to have the cathode on the top of the die and the anode on the bottom. To achieve this, the die can be turned upside down after singulation. This flip-chip configuration is

referred to as "SKN" (cf. Figure 3), and mostly used for very large dies. Moreover, the metallized contact systems are reversed in the flip-chip layout. SKN diodes are always delivered in trays.

The standard metallization is an Al contact on top, and a solderable Ni/Ag contact system on the bottom. More information can be found in section 5.3.
For some chip sizes, a solderable top metallization is available on request.

Figure 3: Rectifier Diode Configurations



3.3 Naming Convention for Rectifier Diodes

As an example of product nomenclature, a common rectifier type is used: SKR 5,6 Qu bo /16. For explanation of the naming, please refer to Table 2.

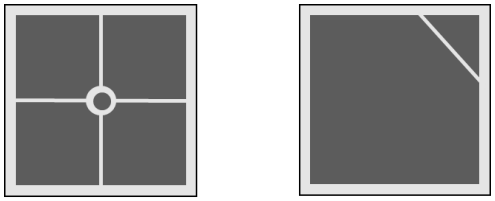
Table 2: Naming Convention Rectifier Diodes

Name	SKR	5,6 Qu	bo	/16	Frame
Meaning	**S**emi**K**ron **R**ectifier	Chip size given as feed size in mm. (Qu= quadratic) 5,6 Qu = 5.6 x 5.6 mm^2	Topside metal contact	Voltage class (V_{rrm}/100)	Delivery format
Variants	SKR *(anode on top)*	*Various* If chip is not square, both feed sizes are given in mm: 16,3x18,2 = 16.3 x 18.2 mm^2	bo: bondable (Al)	/16: 1600V	Frame: sawn-on-frame
	SKN *(cathode on top)*		löt Ag: solderable (Ni/Ag)		*default*: tray

3.4 Options for Thyristors

All SKT thyristors feature the same orientation: anode connection is on the back side of the chip while cathode and gate connections are on the top side.
In order to switch into the conductive state in a controlled way, the thyristor has to be triggered via the gate connection. Two different gate configurations are available: center gate and corner gate, as shown in Figure 4.
While center gate is the most symmetric layout (and therefore the only configuration available for larger die sizes), corner gate shows some benefits regarding bond layout. It should be noted that the difference between center gate and corner gate is not purely a geometric one, but also the triggering behavior of these two gate designs is different (e.g. corner gate version exhibits a lower gate trigger current than the center gate version).

Figure 4: Thyristor Gate Configurations



Center Gate (ZG) Corner Gate (RG)

All thyristors are delivered in trays/waffle packs. It is not possible to deliver thyristors as sawn-on-frame.

Standard metallization for thyristors is the same as for rectifier diodes: bondable Al contact on top (cathode and gate connections), and a solderable Ni/Ag contact system on the bottom. For some chip sizes, a solderable top metallization is available on request.

3.5 Naming Convention for Thyristors

Thyristor nomenclature is similar to the one of rectifier diodes, however taking some specific design features of thyristors into account.

Table 3: Naming Convention Thyristors

Name	SKT	8,9 Qu	ZG	bond	/16
Meaning	**S**emi**K**ron **T**hyristor	Chip size given as feed size in mm. (Qu= quadratic) 8,9 Qu = 8.9 x 8.9 mm^2	Gate configuration	Topside metal contact	Voltage class (V_{rrm}/100)
Variants	-	*Various* If chip is not square, both feed sizes are given in mm.	ZG: center gate	bo or bond: bondable (Al)	/16: 1600V
			RG: corner gate	löt Ag: solderable (Ni/Ag)	

4. Data Sheets

The latest version of data sheets is available on the internet [1]. They typically comprise of different paragraphs which are described in more detail in the sections below. It is important to note that the specification given in the data sheet is only valid for a properly assembled chip, i.e. with suitable thermal and electrical connections as well as die protection (e.g. soft mold).

4.1 Data Sheets of Rectifier Diodes

4.1.1 Highlights Column

On the left hand side of the data sheet, a column with grey background highlights the basic features of the device, including the voltage class as well as the mean forward current for a direct current signal $I_{F(DC)}$.

$I_{F(DC)}$ is calculated similar to $I_{F(AV)}$ (cf. section 4.1.2) but for an ideal direct current, and is regarded as the nominal current of the diode. The boundary conditions for these ratings can be taken from the sections on the right hand side of the data sheet.

Moreover, a photograph of a wafer is shown which represents the whole product family, not the individual die size.

4.1.2 Absolute Maximum Ratings

In this paragraph, the basic limitations of the device are given. Strictly speaking, these parameters do not reflect an "absolute" rating of the bare die device since the (assembly related) boundary conditions such as R_{th} or electrical interconnection technology play a decisive role. The values given in the data sheet are based on a typical assembly type which is a common standard in power semiconductors industry.

First parameter is the voltage class, represented by the maximum repetitive reverse voltage (V_{RRM}) at room temperature and a given leakage current level. The break-down voltage $V_{(BR)}$ is temperature dependent and will decrease by lowering the temperature.

$I_{F(AV)}$ is the mean forward current for a sine signal under the conditions stated in the data sheet. It can be written as:

$$I_{F(AV)}(F_i) = \frac{\sqrt{{V_{(T0)}}^2 + 4 \cdot \frac{{F_i}^2 \cdot r_T \cdot (T_j - T_s)}{R_{th(j-s)}}} - V_{(T0)}}{2 \cdot {F_i}^2 \cdot r_T} \tag{2}$$

Essentially, this is an approximate solution of equation (1).
$\Delta T = T_j - T_s$ and R_{th} have the same meaning as above. T_j and T_s are stated in the data sheet "conditions" column of $I_{F(AV)}$.
F_i is a form factor taking the shape of the electric signal into account. In case of $I_{F(AV)}$, a sinusoidal signal of 10 ms period, F_i is equal to $\pi/2$. In case of a DC signal ($I_{F(DC)}$), $F_i=1$.
$V_{(T0)}$ and r_T are linearly approximizing the maximum I-V forward characteristics following

$$V_{F\,(approximation)} = V_{(T0)} + r_T I_F \tag{3}$$

The meaning of this linear approximation will be explained in more detail in section 4.1.3.

The capability of the device to withstand short-term forward current stress is given by the surge current rating for a half sine wave signal of 10 ms at room temperature and T_{jmax}. The i^2t value is calculated from the maximum surge current:

$$i^2t = {I_{FSM}}^2 \cdot \frac{10\ \text{ms}}{2} \tag{4}$$

The maximum junction temperature T_{jmax} describes the temperature not to be exceeded at any time and point of the semiconductor device. Running the die above T_{jmax} might lead to degradation of the device's functionality and reliability.

4.1.3 Electrical Characteristics

This section specifies the behavior of the device in forward and reverse direction. Typically, the elevated temperature characterization is done at the recommended operation temperature for application simulation purposes.

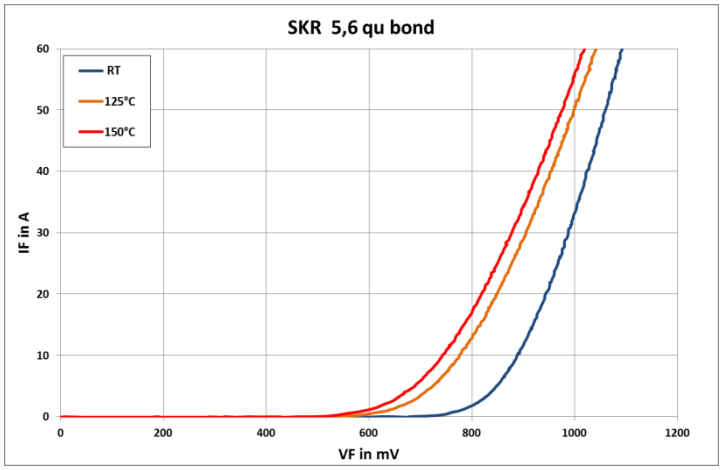
The maximum reverse current is given at the defined V_{RRM} voltage and at different temperatures.

The forward I-V characteristics are specified by the V_F typical and maximum value at a certain current density level, therefore the same V_F values are stated throughout the portfolio. Since the wafer test does not allow a current density testing equivalent to the nominal current in most cases, this current level is below $I_{F(DC)}$ rating. The indicated current density level is chosen to be close to the wafer test conditions for most diodes.
The forward characteristics are stated at T_1=25°C and T_2=125°C. An example of typical I-V characteristics and its temperature dependence are given in Figure 5. It can be seen that the rectifier diode exhibits a negative temperature coefficient at and below nominal current $I_{F(DC)}$ for the temperatures indicated.

For simulation purposes only, a linear approximation of the I-V forward characteristics is also given in the data sheets as parameters $V_{(T0)}$ and r_T. Is follows equation (3).

The two points of the I-V curve used for the linear approximation are chosen from the sufficiently straight part of the I-V curve. The maximum curve approximation by means of parameters $V_{(T0)}$ and r_T include adequate safety margins. With this linear approximation, $I_{F(AV)}$ and $I_{F(DC)}$ can be calculated using equation (2). The validity of this approximation depends on the application and must be verified on the customer side.

Figure 5: Example of Diode Forward I-V Characteristics

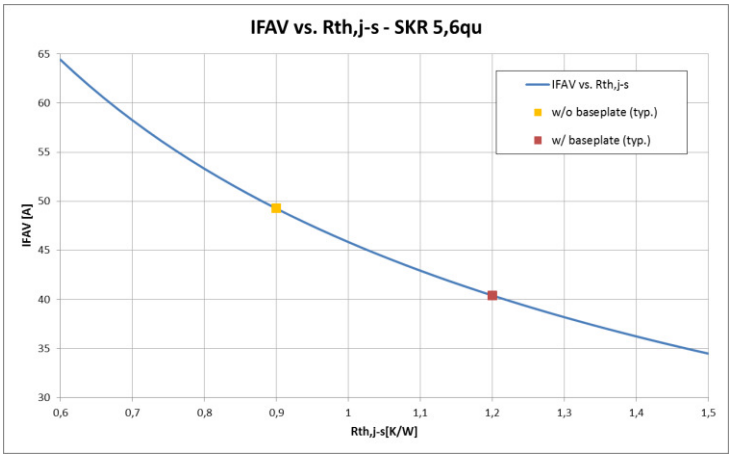


As mentioned above, dynamic losses are negligible in a 50Hz/60Hz application. A typical reverse recovery time t_{rr} under small signal conditions is given to characterize the dynamic behavior. For the definition of t_{rr} and its relation to other dynamic parameters, please refer to chapter 3.2 of the *Application Manual* [2].

4.1.4 Thermal Characteristics

Thermal characteristics given in the data sheets are the range of junction temperature T_j and storage temperature T_{stg}, respectively.
Solder temperature T_{solder} recommendations are given for two different time intervals. Exceeding the thermal budget as described in the data sheet might lead to an altering of chip properties including reliability. More details on assembly processes can be found in section 5.3.
The thermal resistance junction to sink $R_{th(j-s)}$ is given for a specific assembly, and is not a generic chip property. It is used to calculate $I_{F(AV)}$ as described in section 4.1.2.
Figure 6 illustrates the influence of R_{th} on the $I_{F(AV)}$ rating in case of a SKR 5,6 qu diode. For the data sheet value of $I_{F(AV)}$, typically a baseplate module is used. However, using a state-of-the-art baseplate-less assembly like MiniSKiiP®, different R_{th} values apply. Especially for smaller dies, a baseplate-less assembly can lead to better R_{th} values resulting in a significantly higher $I_{F(AV)}$ performance.

Figure 6: Rth Dependence of IF(AV)



4.1.5 Mechanical Characteristics

Mechanical characteristics include the die dimensions and area. The dimensions are given as the raster size of the die on the wafer which is in fact an upper limit for the actual chip outline since some material will be consumed during the dicing process.

Moreover, the chip metallizations are described. In most cases, the anode (upper) metallization is an Al contact suitable for thick wire bonding. The cathode (backside) metallization is a multilayer contact system whose main components are nickel and a terminating Ag layer. This contact is compatible with a wide range of assembly processes.

Most SKR diodes (those <= 10.3 mm feed size) are delivered as sawn-on-frame dies (150 mm diameter wafer). The "Chips/Package" information therefore defines the number of chips per wafer. This is also the *maximum* number of good dies per wafer which might vary due to variation in yield.
For SKR diodes > 10.3 mm and SKN diodes, dies are delivered in waffle packs/trays. The packaging unit is a tray pack, consisting of 6 trays. If there are no further conditions stated at "Chips/Package", the number of dies refers to a single tray. If "1 tray pack (6 trays)" is indicated, the total number of the packaging unit is given.

4.2 Data Sheets of Thyristors

4.2.1 Highlights Column

The left-hand side column in the data sheet features the same items as in the rectifier diode data sheets, cf. section 4.1.1.

4.2.2 Absolute Maximum Ratings

Similar to the diode data sheets, the basic limitations of the device are stated in this paragraph.
Due to the bi-directional blocking behavior of the thyristor, the maximum repetitive peak voltage is given as V_{RRM} (reverse direction; voltage applied from cathode to anode) as well as maximum repetitive peak off-state voltage in forward direction V_{DRM} (voltage applied from anode to cathode, thyristor not triggered).
Both parameters are valid at room temperature. Please note: the break-down voltage $V_{(BR)}$ is temperature dependent and will decrease by lowering the temperature.

$I_{T(AV)}$ has the same meaning for the thyristor as $I_{F(AV)}$ for the diode: it reflects the maximum mean on-state current allowed at the thermal boundary conditions described by the data sheet. $I_{T(AV)}$ and $I_{T(DC)}$ are determined using the same preconditions as explained for the diode in section 4.1.2.

Surge on-state current I_{TSM} for a half sine wave signal of 10 ms is specified at T_{jmax} in an industry standard assembly. It is worth to note again that surge current capability can be limited by the interconnection technology. The i^2t value is calculated from the maximum surge current using equation (4).

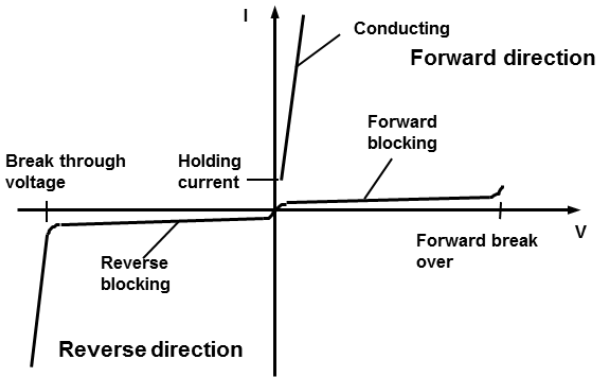
The maximum junction temperature T_{jmax} describes the temperature not to be exceeded at any time and point of the semiconductor device.

4.2.3 Electrical Characteristics

In general, a thyristor can be described as a semiconductor device which can be switched from a high-impedance, low-current off-state to a low-impedance, high-current on-state [3]. Specifically, the SKT thyristor blocks in the reverse direction but can be switched on in the forward direction by means of a gate. Therefore, the thyristor is a three terminal device (anode, cathode, gate) which is often also referred to as semiconductor controlled rectifier (SCR).
Figure 7 shows the schematic current voltage characteristics of a thyristor [2]. In the reverse direction, only a small leakage current is present until the breakdown voltage is reached (> V_{RRM}).
In the forward direction, the device initially behaves similar to the reverse direction if a voltage is applied. A suitable gate current pulse flowing from gate to cathode will trigger a current-amplification in the thyristor, and therefore the device will switch from the (blocking) off-state to the (conducting) on-state.

There are also (undesirable) effects which can cause a firing of a thyristor like exceeding the forward break-over voltage, high dv/dt triggering, light incidence or thermal triggering.
More in-depth coverage of thyristor properties and functionality can be found in [2].

Figure 7: Schematic I-V Characteristics of a Thyristor



The "Electrical Characteristics" section specifies the parameters of the on-state.
The maximum on-state voltage V_T at T_{jmax} is given at a certain current level. A linear approximation of the max. forward characteristics is defined following the procedure described in section 4.1.3 for the diode. This linear approximation can be used for simulation purposes, however, it should be verified that the approximation is appropriate for the actual application.

Moreover, two gate current parameters (and related voltages) are specified.
The gate trigger current I_{GT} and gate trigger voltage V_{GT} are the maximum values at which any thyristor triggers[1]. They are specified at room temperature. From an application standpoint, these are the minimum values the driver has to supply to ensure a safe triggering of all thyristors.

I_{GD} and V_{GD} are the minimum values of gate trigger current and voltage, respectively; below these values, none of the individual thyristors will be triggered. With respect to application considerations, they define the maximum disturbance level preventing unwanted thyristor triggering.
Since current increases with temperature, the parameters are given at elevated temperatures (115°C and 130°C, respectively).

The on-state current of the thyristor is characterized by two more parameters.
The holding current I_H is the minimum current which needs to flow through the thyristor to remain in the on-state.
The latching current I_L is the minimum current through the device at the end of of the gate trigger signal. Below this value, the thyristor will switch back into the off-state.
Both parameters are stated as maximum values at 25°C (same reasoning as for gate currents).

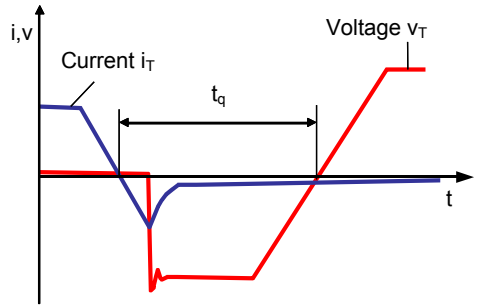
4.2.4 Dynamic Characteristics

The thyristor is turned off if the current falls below the holding current level. The charge carriers need to be gradually removed from the base before the thyristor can pick up forward blocking voltage. A reverse recovery current is flowing for a finite time (Figure 8, [2]). If the device is switched back into the forward voltage regime in this state, the thyristor might be firing again without a trigger signal.

Therefore, the circuit commutated turn-off time t_q describes the minimum time which has to pass during turn-off between zero-current-crossing of the forward current and the moment when a (forward direction) voltage can be applied without re-firing the thyristor. A typical value of t_q is stated in the data sheet. t_q depends on several dynamic boundary conditions as well as temperature; please refer to [2] for further information.

[1] In other words, the maximum value given in the data sheet is above the trigger parameter distribution of the individual devices.

Figure 8: Turn-Off Behavior of a Thyristor



The switching behavior is limited by two further dynamic parameters. A fast rise of the forward voltage can cause a displacement current due to the capacitive nature of the p-n junction. This current can lead to an unwanted triggering of the thyristor. $(dv/dt)_{cr}$ is the critical rate of rise of the forward voltage at which the thyristor is not triggered. It is given as a maximum value at T_{jmax} in the data sheet. The boundary conditions for the parameter specification usually are open gate circuit, $T_j=T_{jmax}$, and an exponential voltage rise to 2/3 of V_{DRM} [2].
When a thyristor is triggered, the current conduction does not take place over the entire device instantaneously. On the contrary, conduction starts in a small area where the gate current density is highest (typically, the area closest to the gate), and then spreads over the device at velocities of the order of magnitude of 100µm per µs. Since excessive current densities might lead to thermal destruction of the device, the total current in the initial on-state phase has to be limited. This is achieved by defining a critical rate of rise of the on-state current $(di/dt)_{cr}$ at T_{jmax} in the data sheet. The value is valid for 50 to 60 Hz operation, a current amplitude of $3xI_{T(AV)}$, and gate pulses of $5xI_{GT}$ with a rising edge of at least 1 A/µs. It is a total value including load current rise and discharge current of a potentially available RC snubber [2].

4.2.5 Thermal Characteristics

Thermal characteristics given in the data sheets are the range of junction temperature T_j and storage temperature T_{stg}, respectively.
Solder temperature T_{solder} recommendations are given as maximum values. Exceeding the thermal budget as described in the data sheet might lead to an altering of chip properties including reliability. More details on assembly processes can be found in section 5.3.
The thermal resistance junction to sink $R_{th(j-s)}$ is given for a specific assembly, and is not a generic chip property. It is used to calculate $I_{T(AV)}$ as described in section 4.2.2.
The same considerations regarding R_{th} impact on current rating apply as in section 4.1.4.

4.2.6 Mechanical Characteristics

Mechanical characteristics include the die dimensions and area. The dimensions are given as the raster size of the die on the wafer which is in fact an upper limit for the actual chip outline since some material will be consumed during the dicing process.

Moreover, the chip metallizations are described. In most cases, the cathode/gate (upper) metallization is an Al contact suitable for thick wire bonding. The anode (backside) metallization is a multilayer contact system whose main components are nickel and a terminating Ag layer. This contact is compatible with a wide range of assembly processes.

SKT dies are delivered in waffle packs/trays. The packaging unit is a tray pack, consisting of 6 trays. If there are no further conditions stated at "Chips/Package", the number of dies refers to a single tray. If "1 tray pack (6 trays)" is indicated, the total number of the packaging unit is given.

4.3 Drawings

The drawings attached to the data sheets are primarily meant to support the die bonding and bond layout design processes at the customer site. A general tolerance of +/-0.20 mm for all lateral dimensions and +/-0.4 mm for roundness should be considered. The specified mean max. chip thickness includes topological features such as metallization, thus the general tolerance of +/-0.03 mm includes the variations of several distinct processes.

4.4 Reliability Tests

During qualification, rectifier diodes and thyristors have been subject to reliability testing. An (non-exclusive) example of reliability tests applied can be found in Table 4.
All chip related reliability tests must be performed in an assembled state (e.g. standard module). Interaction between the chip itself and the assembly might influence the results of the reliability testing. Hence, reliability performance need to be verified on the customer side in the specific assembly used.

Table 4: Reliability Tests for Rectifier Diodes and Thyristors

Test	Reference
High temperature storage (HTS)	IEC 60068-2-2 Test B
Low temperature storage (LTS)	IEC 60068-2-1
Storage in damp heat (with voltage load)	IEC 60068-2-67
High temperature reverse bias (HTRB)	IEC 60749-23
Power cycling (PC)	IEC 60749-34
Thermal Cycling	IEC 60068-2-14 Test Na

5. Instructions and Recommendations for Use

The following chapter deals with packaging, labeling, and handling of SEMIKRON rectifier diodes and thyristors when shipped to the customer. Moreover, some general considerations regarding assembly are given. Mishandling of semiconductor devices might compromise their electrical or mechanical properties.

5.1 Delivery Formats and Packaging

The standard delivery format is technology and size dependent. While all thyristors are delivered in waffle-packs/trays, smaller SKR up to feedsize of 10.3mm are delivered as a 150 mm wafer mounted and diced on an adhesive tape with the aid of a fitting wafer frame (“sawn-on-frame”).
An overview is given in Table 5.

Table 5: Delivery Format Overview (status Q3/2015)

Device Type	Voltage Class	Feed Size	Delivery format
Rectifier Diode (SKR)	1600 V	3.5 … 10.3 mm	Sawn-on-frame (150 mm wafer)
Rectifier Diode (SKR)	1600 V	12.4 … 22.4 mm	Chip Tray/Waffle Pack (4’’ x 4’’)
Rectifier Diode (SKN)	1600 V	all	Chip Tray/Waffle Pack (4’’ x 4’’)
Thyristor (SKT)	1600 V	all	Chip Tray/Waffle Pack (4’’ x 4’’)

5.1.1 Sawn-On-Frame Format

The packaging is equivalent to CAL diodes [4]. The figures below show a SKR diode label example.

Figure 9: Wafer Packaging

Each wafer is packaged in an evacuated bag with protective inlays (cf. Figure 9). Prior to customer shipment, up to 25 wafers of one lot are placed into a cardbox for transport. If less than 25 wafers are shipped, filling material is used.
Chips can only be shipped as multiples of wafers. Due to the varying yield on the wafer, the exact amount of good dies might be different per wafer. Orders have thus to be placed with an appropriate delivery tolerance (typically +/-10%).

5.1.2 Product Labeling: Sawn-on-frame Wafer Shipment

There are three different labels in order to allow customers to identify SEMIKRON hardware at the different stages of the assembly process. The first one is on the outer cardbox packaging, the second one on the bag around the wafer, and the third one ("frame label") on the red wafer frame which is readable when all surrounding packing material has been removed. The barcodes used on these labels are according to the Code 128 standard.

The label on the cardbox consists of the SEMIKRON logo and the product name as well as 4 different barcodes (refer to Figure 10):

(1) barcode/text: **P** customizable material no. (not always applicable)
(2) barcode/text: **H** SEMIKRON lot no. (10 digits)
(3) barcode/text: **Q** wafer qty/good die qty/country code ("D")/SK lot no.
(4) barcode/text: **X** SEMIKRON article no.

Figure 10: Label on Cardbox Packaging

The bar code on the foil bag label and the frame label has the same structure. However, the outer label has some more information given in plain text. The outer label (foil bag) contains:

- Type of chip
- SEMIKRON article number
- Lot number
- Chip Quantity
- Delivery date

- Signature field for "QC pass" (quality conformity)
- Bar code field
- "process until" date for wafer

The frame label contains the following information:

- SEMIKRON article number
- Type of chip
- Bar code field

Pictures of the two different labels can be found in Figure 11.
As mentioned above, the barcode of the two labels on the two wafer packaging labels has the same structure:

- digits 1- 8: SEMIKRON article number
- digits 9-13: good dies per wafer
- digits 14-17: "use-by date" given by the calendar week and year (wwyy)
- digits 18-27: customizable (0 by default)
- digits 28-37: lot number
- digits 38-40: split number
- digits 41-42: wafer number

The barcode is also given as text underneath the code.

Figure 11: Labels on single wafer packaging

5.1.3 Chip Tray Deliver Format

If chips are delivered in trays, only good dies are supplied. The usual packaging unit is a tray pack consisting of six 4'' x 4'' trays and a lid. In most cases, tray packs are completely filled but there might also be only partially filled tray packs since dies of different lots are kept separately.
A label similar to the outer label (foil bag) described in section 5.1.2 is applied to the lid of the tray pack[2]. The pack is sealed in a moisture barrier bag (MBB), and the same label is applied to the bag due to its non-transparent nature. Details can be seen in Figure 12.

Figure 12: Tray Packaging

[2] The only difference is the meaning of digits 41-42 which do not coincide with the wafer number.

Tray pack sealed in MBB foil with outer label (left) and unpackaged with inner label (right). Top Views.

5.2 Storage Conditions

SEMIKRON guarantees a shelf life of 6 months after shipment from production line to SEMIKRON stock for the unopened package if handled appropriately.
For handling and storage recommendations, please refer to IEC 62258-3 [5].
Required storage conditions for unopened package at the customer site:

- temperature 20-26°C
- relative humidity rH < 60%

Dies in opened packages are intended for immediate use.

5.3 Assembly process

SEMIKRON rectifier diodes and thyristors have been tested to be compatible with different industry standard assembly processes. It can be used in a reflow or preform solder process. A second soldering process is possible.
The thermal budget given in the data sheet (i.e. for SKR diodes T_{solder} for 10 min at 250°C or T_{solder} for 5 min at 320°C) shall not be exceeded. The appropriate temperature profile used during soldering depends on the process as well as the materials (e.g. solder paste) used.
Special care should be exercised to keep the passivated chip termination free from solder or flux residues as this might influence the electric properties.

The anode Al metallization is comparably thick by industry standards and allows thick-wire bonding connections. The Al wire diameter should be smaller or equal to 500 µm.

6. Summary

SEMIKRON rectifier diodes and thyristors are a cost efficient, robust technology solution for input rectifier applications. They are being used successfully in a wide range of different interconnection and assembly techniques.
Bare die customers stand to benefit from the long-term experience of SEMIKRON, the market leader in diode and thyristor modules [6].

7. Appendix: List of Bare Die Products

Table 6: Rectifier Diodes and Thyristors Standard Portfolio (status Q3/2015)

Voltage Class	Technology Family	Chip Name	$I_{F(DC)}$ [A]	Area [mm²]	T_{jmax} [°C]
1600 V	SKR qu	SKR 3,5 Qu bond	18	12,3	150
1600 V	SKR qu	SKR 4,2 Qu bond	28	17,6	150
1600 V	SKR qu	SKR 4,8 Qu bond	35	23,0	150
1600 V	SKR qu	SKR 5,6 Qu bond	40	31,4	150
1600 V	SKR qu	SKR 6,2 Qu bond	50	38,4	150
1600 V	SKR qu	SKR 7,0 Qu bond	60	49,0	150
1600 V	SKR qu	SKR 8,9 Qu bond	110	79,2	150
1600 V	SKR qu	SKR 10,3 Qu bond	135	106,1	150
1600 V	SKR qu	SKR 12,4 Qu bond	190	153,8	150
1600 V	SKR qu	SKR 15,2 Qu bond	270	231,0	150
1600 V	SKR qu	SKR 16,3 x 18,2 Qu bond	305	296,7	150
1600 V	SKN qu	SKN 18,2 Qu bond	320	331,2	150
1600 V	SKN qu	SKN 22,4 Qu bond	630	501,8	150
1600V	SKT qu - corner gate	SKT 5,6 Qu RG bond	45	31,4	130
1600V	SKT qu - corner gate	SKT 7,0 Qu RG bond	55	49,0	130
1600V	SKT qu - corner gate	SKT 8,9 Qu RG bond	80	79,2	130
1600V	SKT qu - center gate	SKT 8,9 Qu ZG bond	80	79,2	130
1600V	SKT qu - corner gate	SKT 10,3 Qu RG bond	95	106,1	130
1600V	SKT qu - center gate	SKT 10,3 Qu ZG bond	95	106,1	130
1600V	SKT qu - corner gate	SKT 12,4 Qu RG bond	130	153,8	130

1600V	SKT qu - center gate	SKT 12,4 Qu ZG bond	130	153,8	130
1600V	SKT qu - center gate	SKT 13,5 Qu ZG bond	145	182,3	130
1600V	SKT qu - center gate	SKT 15,2 Qu ZG bond	175	231,0	130
1600V	SKT qu - center gate	SKT 18,2 Qu ZG bond	205	331,2	130
1600V	SKT qu - center gate	SKT 24,3 Qu ZG bond SG	400	590,5	130

Symbols and Terms

Letter Symbol	Term
$(di/dt)_{cr}$	critical rate of rise of the on-state current (thyristor)
$(dv/dt)_{cr}$	critical rate of rise of the forward voltage (thyristor)
F_i	form factor of electric signal
i^2t	permitted limit integral
I_F	forward current
$I_{F(AV)}$	mean forward current (sine signal)
$I_{F(DC)}$	mean forward current (DC signal)
I_{FSM}	maximum forward surge current
I_{GD}	maximum gate non-trigger current
I_{GT}	Minimum gate trigger current
I_H	holding current
I_L	latching current
I_T	forward on-state current (thyristor)
$I_{T(AV)}$	mean on-state current (sine signal)
$I_{T(DC)}$	mean on-state current (DC signal)
I_{TSM}	maximum on-state surge current
P_v	power dissipation
r_T	forward slope resistance (linear approximation)
R_{th}	thermal resistance
T_j	junction temperature
T_{jmax}	maximum junction temperature
T_{jop}	maximum operation junction temperature
t_q	Circuit commutated turn-off time (thyristor)
t_{rr}	reverse recovery time
T_s	(heat) sink temperature
T_{solder}	soldering temperature
T_{stg}	storage temperature

$V_{(BR)}$	avalanche break-down voltage
V_{DRM}	maximum repetitive peak off-state voltage in forward direction
V_F	forward voltage
V_{GD}	gate non-trigger voltage
V_{GT}	gate trigger voltage
V_{RRM}	maximum repetitive peak reverse voltage
V_T	on-state voltage (thyristor)
$V_{(T0)}/V_{T(TO)}$	forward threshold voltage (linear approximation)

A detailed explanation of the terms and symbols can be found in the *Application Manual Power Semiconductors* [2].

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HISTORY

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