SEMIKRON
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Technical Explanation
SEMiX®5

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Keyword: SEMiX®5, MLI, TMLI, GARL, GD

1. Introduction

SEMiX®5 was introduced as part of SEMIKRON's new line of IGBT modules at SPS 2014. SEMiX®5 is a compact baseplate module with AC DC screw connections. A solder-free assembly process for the gate driver connections is possible thanks to the press-fit signal connections. With an optimized internal layout and a housing material ready for high temperature operations, the SEMiX®5 is the perfect match for demanding applications for UPS, solar and motor drive.

1.1 Features

Main key features of SEMiX®5 are

- Low stray inductance thanks to optimized commutation paths
- Superior dynamic performances
- Solder-free assembly of driver boards
- Press-fit signal pins and screw power terminals
- 17mm height
- Baseplate solution
- Reliable mechanical design
- Robust housing with enhanced properties that allows reaching high operating temperature being ready for new chip generations at 175 degrees and above.
- Optimised thermal performance thanks to optimized internal layout
- Competitive and comprehensive product range
- Common collector horizontal leg for T-NPC configuration allowing easy parallelization
- High flexibility for custom design

1.2 Customer advantages and benefits

In this chapter we will analyse deeper the customer advantages due the special design of SEMiX®5

1.2.1 Wide and competitive portfolio

SEMiX®5 offers the most comprehensive and competitive product portfolio for this type of modules.

- 6-pack configuration 650V, 1200V, 1700V
- 3-level configurations 650V up to 400A
- T-type 3-level configuration both 650V/1200V and 1200V/1200V
- Buck-boost converters
- Double boost solutions possible for UPS and solar application
- Half Bridge Rectifier
- And of course customization is possible!

Figure 2 shows the details of the current topology offered. The Type designations is explained in following chapters.

1.2.2 Low inductance design

Power terminals positive, neutral and negative are located on the same side on the module. Moreover the internal layout has been optimized to minimize internal current commutation paths between DC+, AC and Neutral (or DC-, AC, Neutral) terminals.
This generally lead to lower stray inductances and so finally lower switching losses.
Real benchmark test with competition module (form fit compatible) shows up to 20% lower E_{off} and up to 10% lower E_{on} for T-NPC configuration.

1.2.3 Excellent thermal performances

SEMiX®5 has an optimized heat spread design for optimal heat transfer resulting in lower internal thermal resistance. The maximum junction-temperature in normal operation and overload are lower than equivalent conventional layout (see Figure 1). Real benchmarks with competition modules with conventional design show up to 20% lower Rth (junction-case) and up to 30% lower Rth (case-sink).

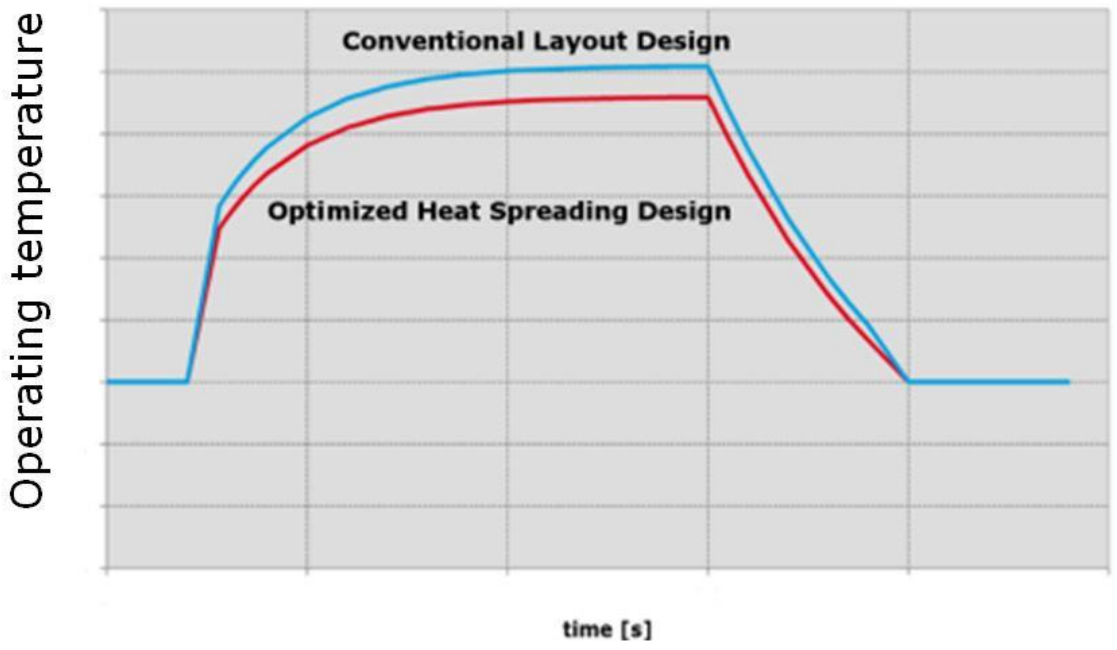
In a typical 3L TNPC application with

- V_{DC}=750V
- V_{out}=400 VAC

- cosφ=0,9
- f_{sw}=5kHz
- T_a=40°C

this leads to 10% more output power provided by SEMiX®5, or lower operating temperature with respect to modules designed conventionally.

Figure 1: Operating temperature over time comparison between conventional layout design and SEMiX®5 optimized heat spreading design



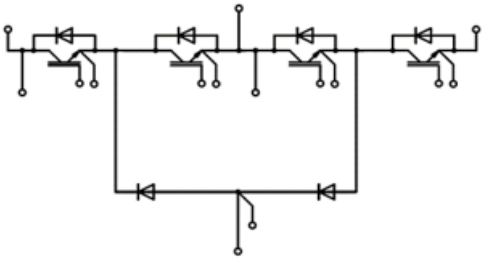
1.2.4 Housing Material

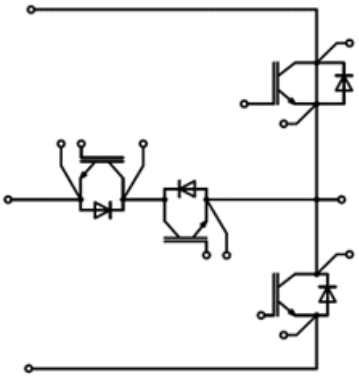
The SEMiX®5 housing material is an advanced fiberglass reinforced compound material that provides improved mechanical strength and robustness. This material is ready for upcoming chip generations and allows chip operation up to Junction Temperature T_j 175 °C as the new chip generations will be available.

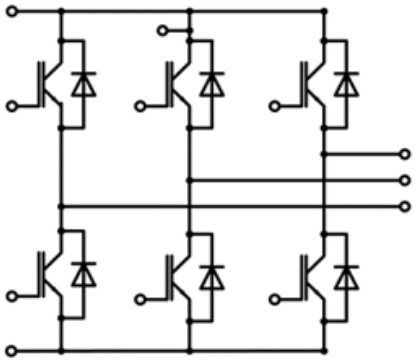
1.2.5 UL

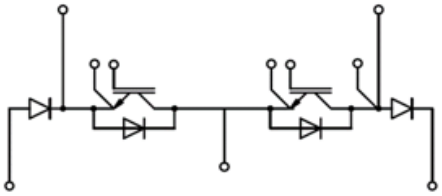
SEMiX®5 UL recognized file is E63532, Vol. 6, Section 1

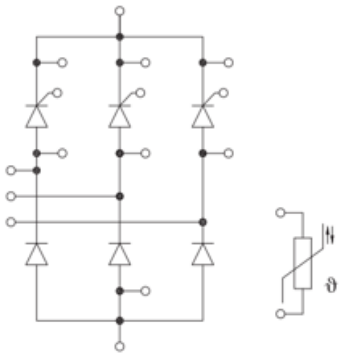
Figure 2: SEMiX®5 product portfolio (June 2021)

NPC topology			
Module Name	Inom	Blocking voltage	Circuit
SEMiX155MLI07E4	150	650	
SEMiX205MLI07E4	200	650	
SEMiX305MLI07E4	300	650	
SEMiX405MLI07E4	400	650	
SEMiX355MLI12M7	350	1200	
SEMiX305MLI12E4V2	300	1200	
SEMiX205MLI12E4V2	200	1200	

TNPC topology			
Module Name	Inom	Blocking voltage	Circuit
SEMiX205TMLI12E4B	200	1200/650	
SEMiX305TMLI12E4B	300	1200/650	
SEMiX405TMLI12E4B	400	1200/650	
SEMiX305TMLI12E4CV2	300	1700/1200	

3-Phase full bridge topology			
Module Name	Inom	Blocking voltage	Circuit
SEMiX305GD07E4	300	650	
SEMiX205GD012E4	200	1200	
SEMiX155GD12T4	150	1200	

Double Boost topology			
Module Name	Inom	Blocking voltage	Circuit
SEMiX405GARL07E3	400	650	

Half Controlled Rectifier topology			
Module Name	Inom	Blocking voltage	Circuit
SEMiX245DH16	240	1600	
SEMiX365Dh16	360	1600	

2. Technical details of SEMiX®5

Currently, the SEMiX®5 is available with IGBT and rectifier module topologies. The whole module family is based on the same design principles, which grants best efficiency in production logistic and quality chain

2.1 Mechanical and electrical design

SEMiX®5 is based on established packaging technologies. The power semiconductor devices (IGBT, diodes or thyristors) are wire bonded on top and soldered to Al_2O_3 DBC ("Direct Bonded Copper") substrates. The substrates are soldered to a solid copper base plate.
For all auxiliary contacts (gate, auxiliary emitter, temperature sensor) Press-Fit contacts are in use. Press-Fit contacts allow solder-free driver connection for fast assembly.
The construction principle of the SEMiX®5 is the visible in Figure 3.
Figure 4 shows the mechanical layout of the SEMiX®5.

Figure 3: Construction principle of SEMiX®5

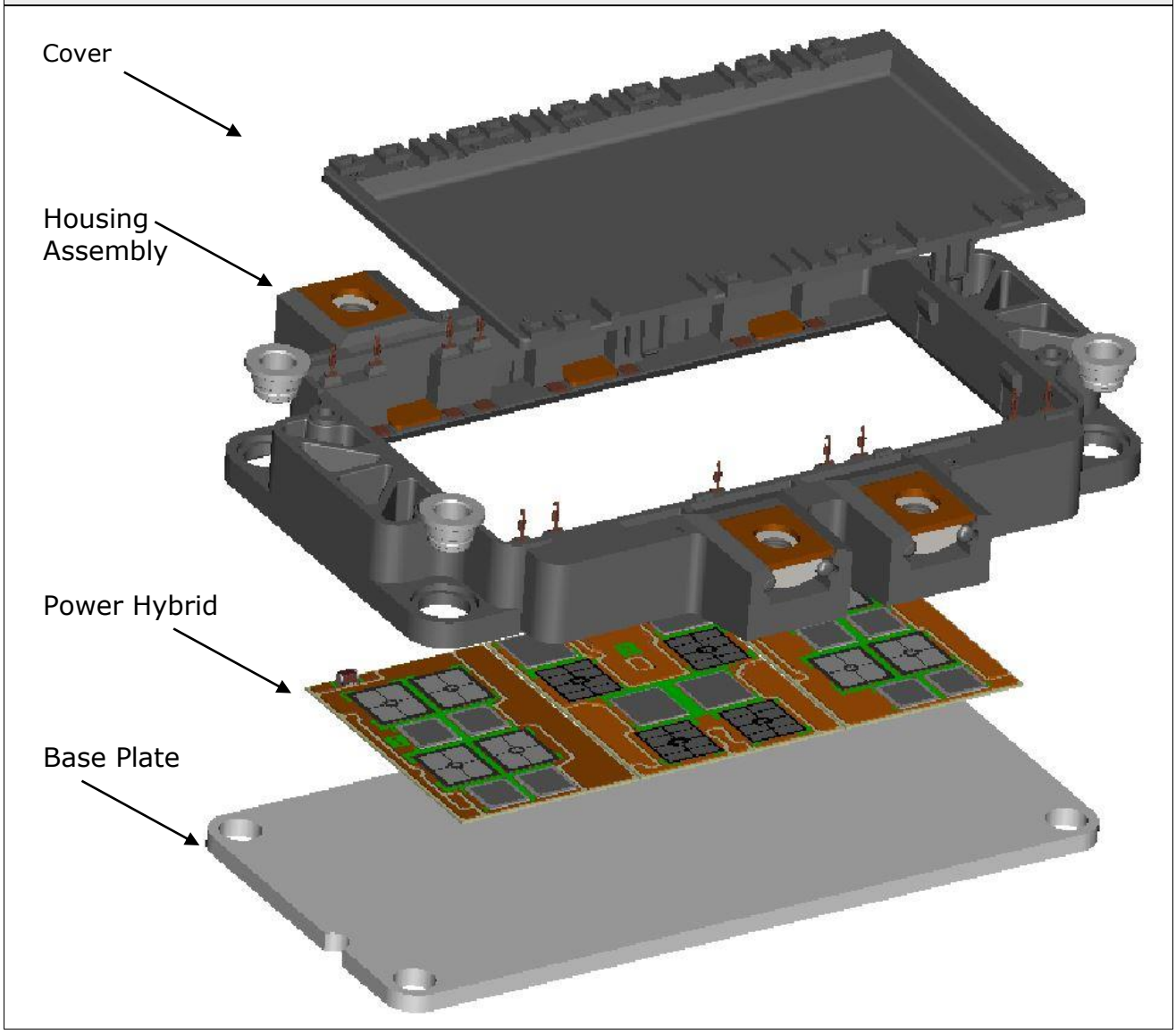
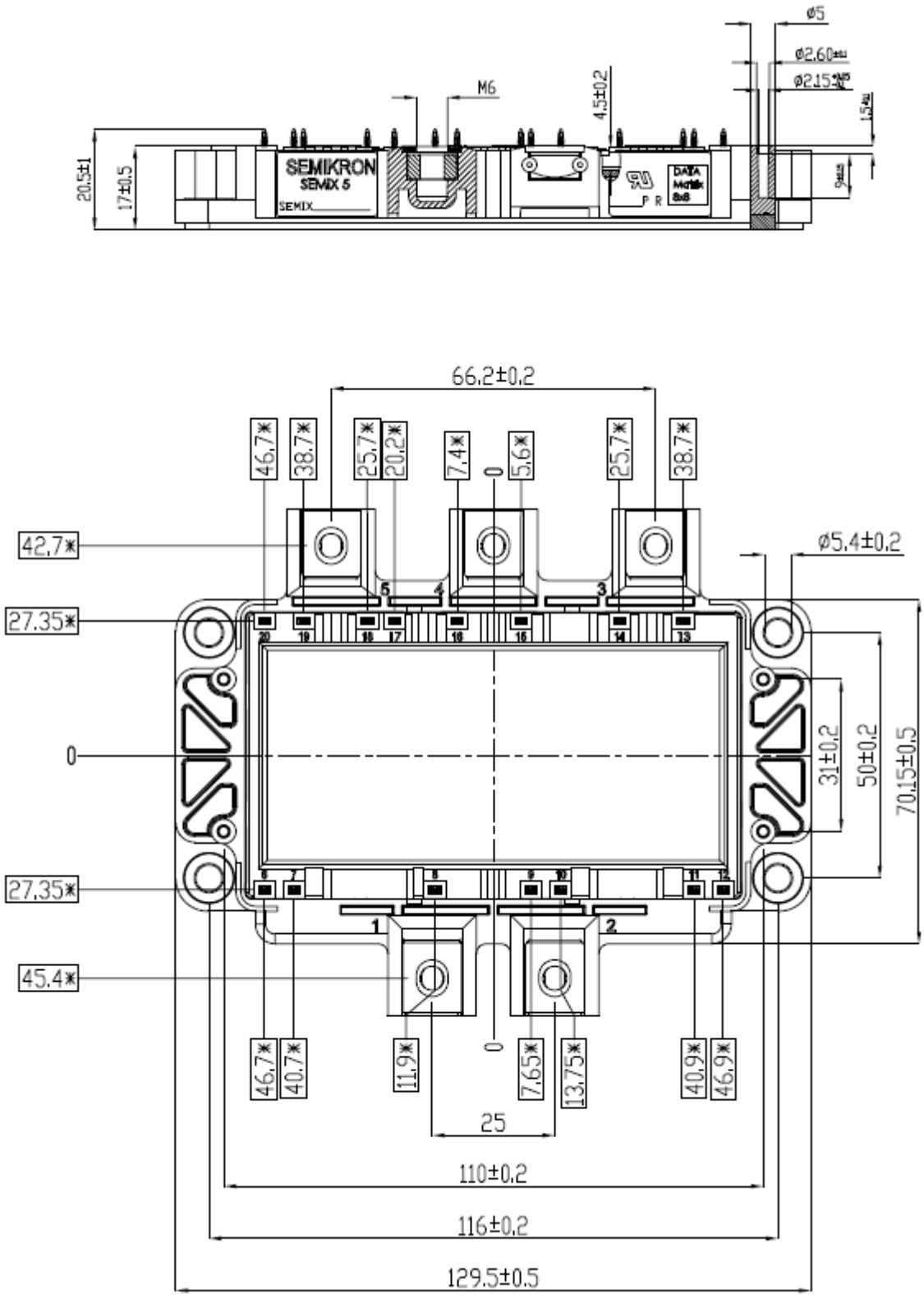


Figure 4: SEMiX®5 Mechanical layout



2.2 Electrical behaviour

We will concentrate in this chapter on the electrical behaviour of **T**-type 3-level **N**eutral **P**oint **C**lamped topology (**3L TNPC**) and **N**eutral **P**oint **C**lamped topology (**3L NPC**).

2.2.1 Current distribution

The current distribution between silicon chips is affected mainly by the parasitic stray inductance and the difference of these inductances between the commutation paths. The main design feature that influences these parasitic stray inductances is the layout of the chips on the DBC and hence the commutation behaviour between switches.

The commutation inductances are split in three different values:
In following figures D_i refers to the anti-parallel diodes and T_i to the IGBTs being "i" the switch number.

- L_{CE} This is the commutation inductance in case a TNPC module is operated as 2-level device (see the test set-up used for the measure in Figure 5). Sometimes referred also as "long" commutation path.

- L_{sCE1} This is the "short" commutation inductance of the 3-level commutation in TNPC (see the test set-up used for the measure in Figure 6), and the "short" commutation in NPC (see the test set up used for measure in Figure 8).

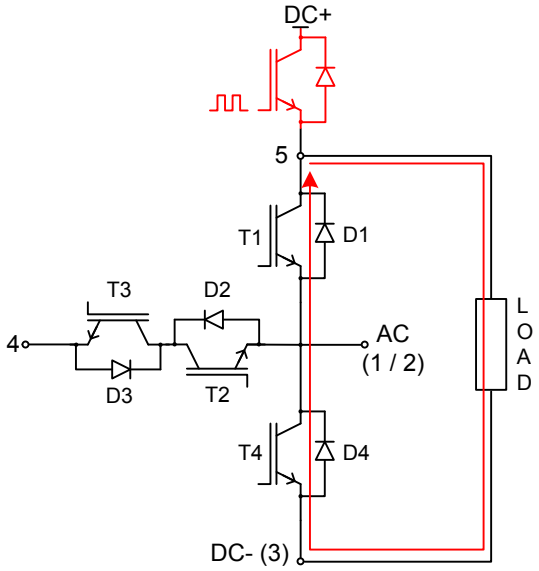
- L_{sCE2} This is the commutation inductance of the "long" commutation in NPC; it does not exist in TNPC (See the test set-up used for measure in Figure 7)

L_{sCE1} and L_{sCE2} are calculated with respect to the different commutation paths which are explained in Figure 6-9 (referred as 1st and 2nd short/long).

In SEMiX®5 datasheets for each "long" and "short" commutation path, the highest value of the measured stray inductances is given.

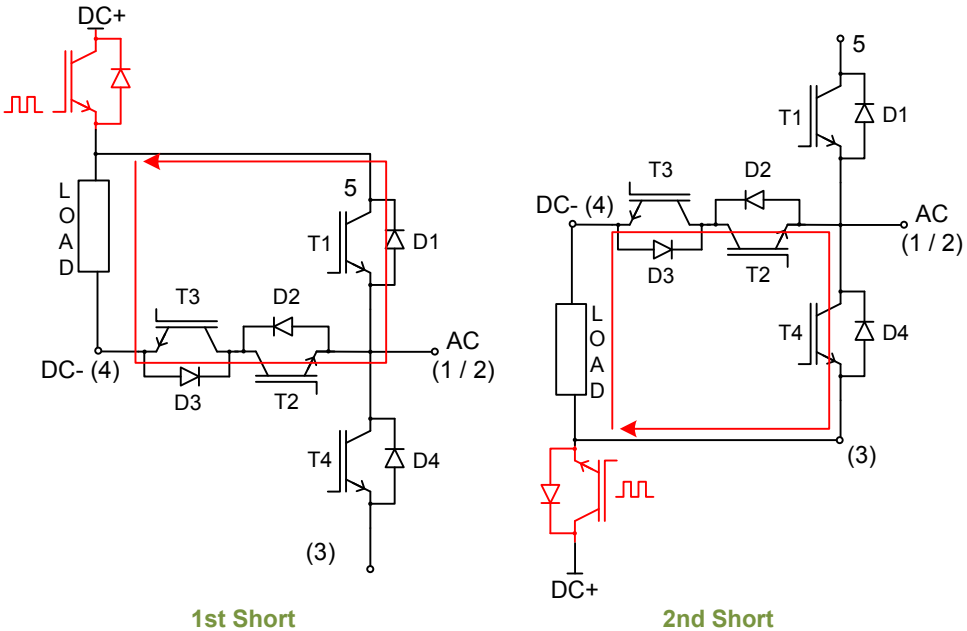
In Table 1-3 measured values for commutation inductances of MLI and TMLI modules are presented.

Figure 5: TNPC (TMLI) 2-level mode commutation loop (L_{CE}) test set up



2-Level Mode

Figure 6: TNPC (TMLI) Short commutation loops (L_{SCE1}) test set up



1st Short

2nd Short

Figure 7: NPC (MLI) long commutation loops (LsCE2) test set up

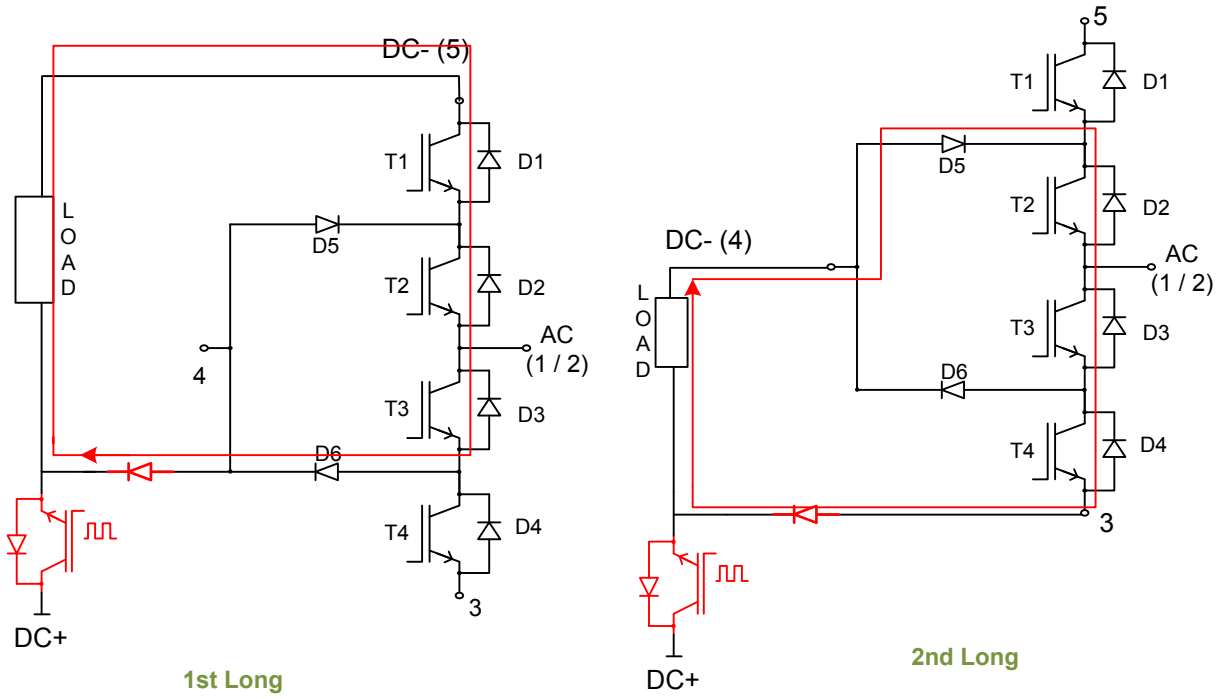


Figure 8: NPC (MLI) short commutation loops (LsCE1) test set up

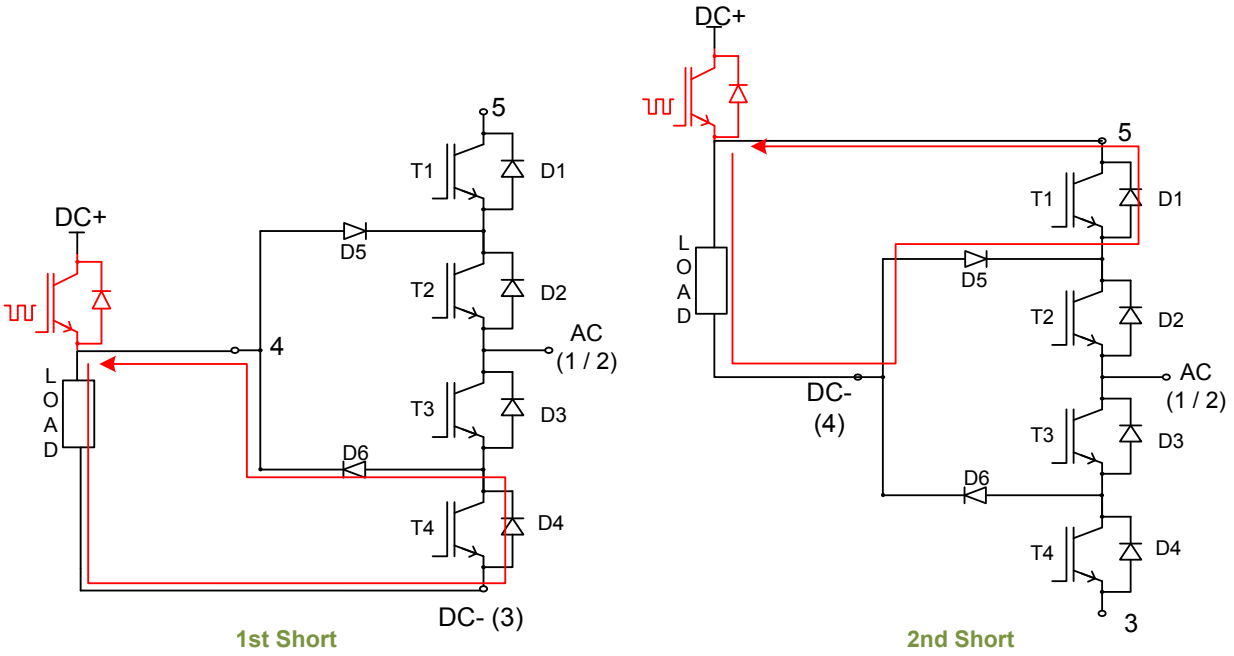


Table 1: Commutation inductances of SEMiX405TMLI12E4B and SEMiX405MLI07E4		
	SEMiX405TMLI12E4B SEMiX305TMLI12E4B SEMiX205TMLI12E4B	**SEMiX405MLI07E4**
L_{CE}	42 nH	-
L_{sCE1}	31 nH	27 nH
L_{sCE2}	-	34 nH

Table 2: Commutation inductances of SEMiX305MLI07E4 and SEMiX205MLI07E4		
	SEMiX305MLI07E4	**SEMiX205MLI07E4**
L_{CE}	-	-
L_{sCE1}	29 nH	27 nH
L_{sCE2}	38 nH	38 nH

Table 3: Commutation inductances of SEMiX205MLI12E4		
	SEMiX205MLI12E4 SEMiX205MLI12E4	
L_{CE}	-	
L_{sCE1}	30 nH	
L_{sCE2}	36 nH	

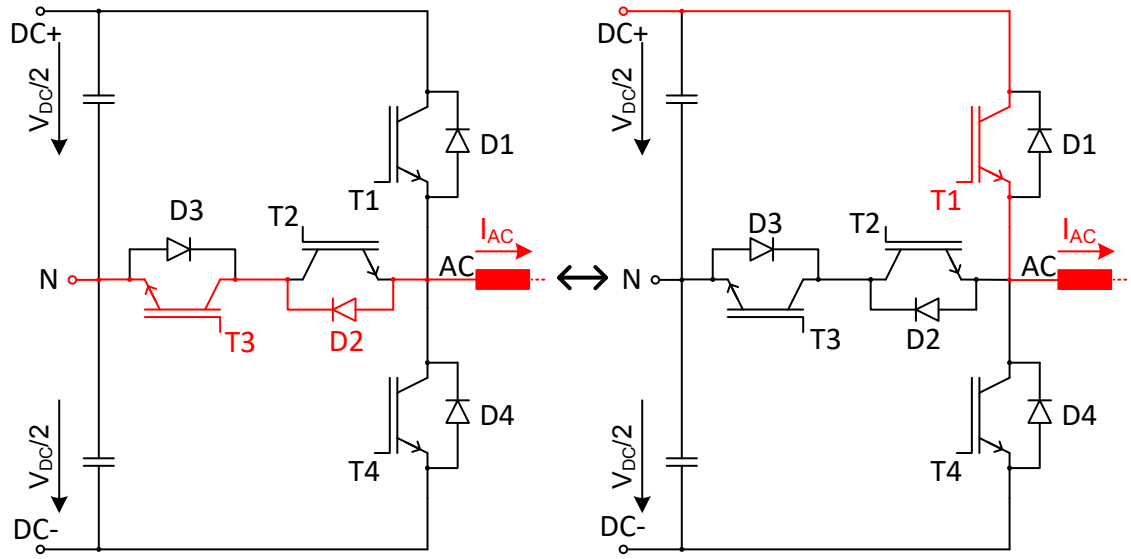
2.2.2 Dynamic losses

SEMiX®5 turn-on / turn off energy diagrams are based on different test set-ups which are explained in the following pictures.
For further details it is recommended to refer to [9].

TNPC: IGBT1 & Diode2 turn-on / -off energy

In the SEMiX®5 TNPC datasheets *IGBT1* indicates without distinction T1 or T4 and *Diode2* indicates without distinction D2 or D3 (Figure 9).

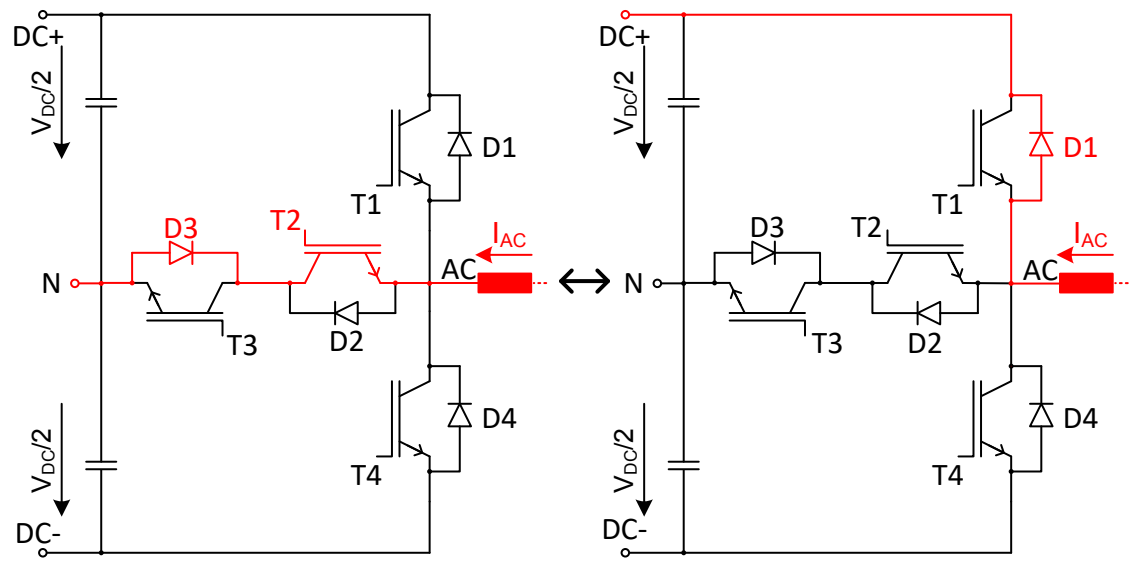
Figure 9: TNPC: IGBT1 & Diode2 turn-on / -off energy



TNPC: IGBT2 & Diode1 turn-on / -off energy

In the SEMiX®5 TNPC datasheets *IGBT2* indicates without distinction T2 or T3 and *Diode1* indicates without distinction D1 or D4 (Figure 10).

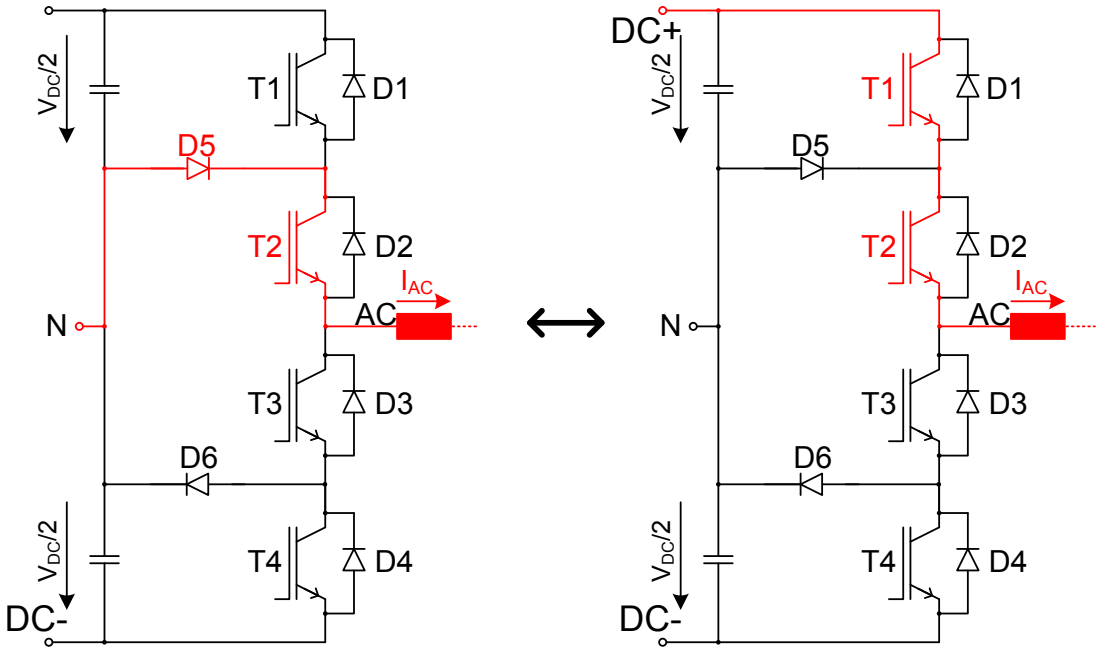
Figure 10: TNPC: IGBT2 & Diode1 turn-on / -off energy



NPC: IGBT1 & Diode5 turn-on / -off energy

In the SEMiX®5 NPC datasheets *IGBT1* indicates without distinction T1 or T4 and *Diode5* indicates without distinction D5 or D6 (Figure 11).

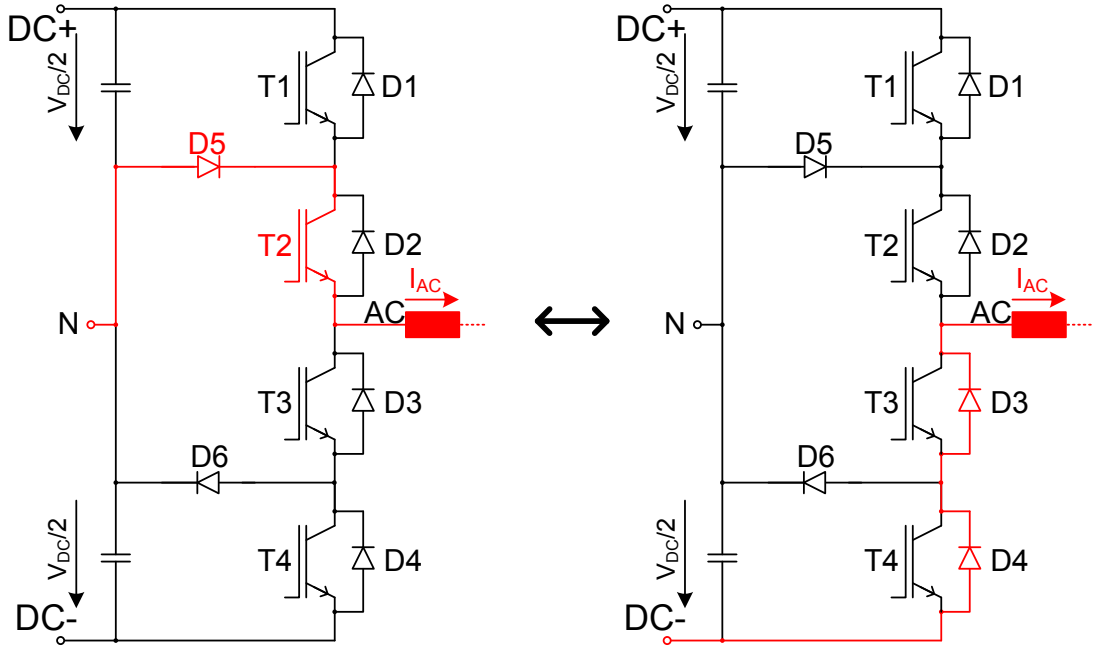
Figure 11: NPC: IGBT1 & Diode5 turn-on / -off energy



NPC: IGBT2 & Diode1 turn-on / -off energy

In the SEMiX®5 NPC datasheets *IGBT2* indicates without distinction T2 or T3and *Diode1* indicates without distinction D1 or D4 (Figure 11).

Figure 12: NPC: IGBT2 & Diode1 turn-on / -off energy



2.3 Creepage and Clearance Distances

SEMiX®5 press-fit modules comply with the creepage and clearance distances required by DIN EN 50178, EN62477-1 and EN61800-5-1 by cases, with the following boundary conditions:

- Maximum peak voltage: 1700 V
- Maximum DC-link voltage (rms): 1250 V
- Line over-voltage category: 3
- Pollution degree: 2
- Maximum height of operation above sea level: 4000 m
- Basic insulation of temperature sensor
- Comparative Tracking Index (CTI) of the housing: Class IIIb (100≤CTI<175)

Table 4: Nominal creepage and clearance distances

Creepage	Terminal to terminal	20 mm
	Terminal to base plate	17.7 mm
Clearance	Terminal to terminal	8.3 mm
	Terminal to base plate (= heat sink potential)	10.6 mm*

* A lens head screw of type ISO 7380 (M5) is necessary to achieve this clearance distance.

2.4 Insulation test

As stated in the datasheets all SEMiX®5 modules are specified for an insulation voltage V_{isol}=4kV, AC sinus 50 Hz for 1 minute.

All SEMiX5 are tested in accordance to UL 1557, by applying a potential at a frequency within the range of 40-70 Hz between live parts and accessible dead metal parts. Exception: a dc potential equal to 1.414 times the specified 40-70Hz potential may be used.

Please note that because SEMiX®5 is not equipped with security thermistor as indicated in UL 1434 the insulation test versus the NTC is not performed

The insulation test is performed as follows: All main and auxiliary terminals (including main, auxiliary emitter, gate and temperature sensors contacts) are short circuited and tested with reference to the baseplate.

2.5 Type designation system

Following type designation is used for SEMiX®5

SEMiX	40	5	TMLI	12	E4	B	Vx
①	②	③	④	⑤	⑥	⑦	⑧

1. SEMiX : Product Family Name
2. 40 : 400A nominal chip current,
3. 5 : SEMiX®5 Housing
4. TMLI : circuit electrical configuration
   - MLI = 3-level NPC
   - TMLI = 3-Level T-NPC
   - GARL = Double Boost
   - GD = 3-Phase full bridge
   - DH = Half Controlled Input Bridge
   - MH = Half Bridge with two arms consisting of MOS
   - BT = Bridge – Three Level
5. Collector-emitter voltage class of IGBT1 and Diode1 (TMLI) or all switches (MLI, GARL, GD):
   06: 600V IGBT3 trench & field stop
   07: 650V IGBT3 Medium or Low power trench & field stop
   10: 950V IGBT7
   12: 1200V IGBT4 trench & field stop
   17: 1700V IGBT4 trench & field stop
6. Chip generation of IGBT1 and Diode1 (TMLI) or all switches (MLI, GD), no value (DH, GARL):
   - E4: IGBT4 Infineon Medium Power for 1200V and 1700V.
   - E4: IGBT3 Infineon Medium Power for 650V
   - E3: IGBT3 Infineon Low Losses for 650V
   - T4: IGBT4 Infineon Low Power
   - M7: IGBT M7
7. Collector-emitter voltage class of IGBT2 and Diode2 (TMLI), no value (MLI, GARL, GD, DH):
   A: 600V IGBT3 trench & field stop
   B: 650V IGBT3 Medium Power trench & field stop
   C: 1200V IGBT4 trench & field stop
   D: 1700V IGBT4 trench & field stop
8. Vx: Variant number

2.6 Chip Locations

For detailed temperature measurements, the exact positions of the chips need to be known. To get the chip position and thermal material data of a specific SEMiX®5 module please contact your SEMIKRON representative for further support

3. Chip technologies and product Ranges

SEMiX®5 IGBT modules presently use three types of IGBTs:

- 1700V IGBT4 Trench & Field Stop technology
- 1200V IGBT4 Trench & Field Stop technology
- 650V IGBT4 Trench & Field Stop technology

3.1 Trench IGBT

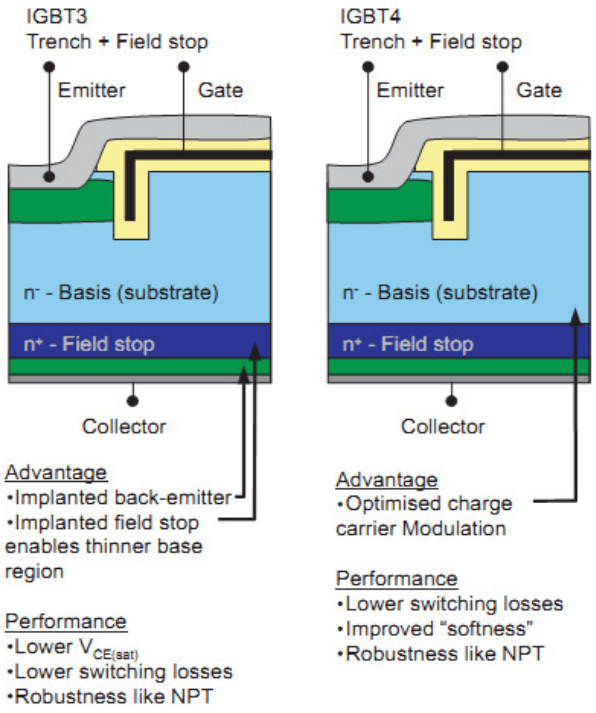
The "Trench IGBT" chip design is based on a trench-gate structure combined with a "Field Stop" n^+ buffer layer for punch through feature, as shown in Figure 13.

These type of IGBTs have a positive temperature coefficient and allow for parallel use.

With the introduction of the 4th IGBT generation, this general design was not changed, but the trade-off between the on-state losses $V_{CE(sat)}$ and the switching losses E_{on} + E_{off} was optimized for operation with switching frequencies above 4kHz. Furthermore, the 1200V "IGBT4" is able to operate with a maximum junction temperature T_{jmax} = 175°C. The increased T_{jmax} offers more flexibility in overload conditions or for applications with few temperature cycles (e.g. pumps or fans) where the junction temperature might now exceed the former limits.

For further information on "IGBT4", please refer to [3] and [4].

Figure 13: IGBT concepts, basic properties



3.2 Inverse and Free-Wheeling diodes

The free-wheeling diodes used in SEMiX®5 IGBT modules are specially optimized CAL (**C**ontrolled **A**xial **L**ifetime) diodes designed and manufactured by SEMIKRON. These fast, "super soft" planar diodes are characterised by the optimal axial profile of the charge carrier life-time.

This leads to:

- low peak reverse current lowering the inrush current load on the IGBTs in bridge circuits
- "Soft" decrease in the reverse current across the entire operating temperature range, which minimizes switching surges and interference
- robust performance even when switching at high di/dt
- very good paralleling capability thanks to the negligible negative temperature coefficient and the small forward voltage (V_f) spread

SEMIKRON's "CAL4" diode is designed specifically for use with the "IGBT4" generation, boasting low thermal losses and outstanding soft switching behaviour even at extreme commutation speeds. Furthermore, the newly developed junction termination ensures safe operation up to 175°C.

For further information on CAL4, please refer to [5].

3.3 Operating areas for IGBTs

The safe operating areas are not included in the datasheets.

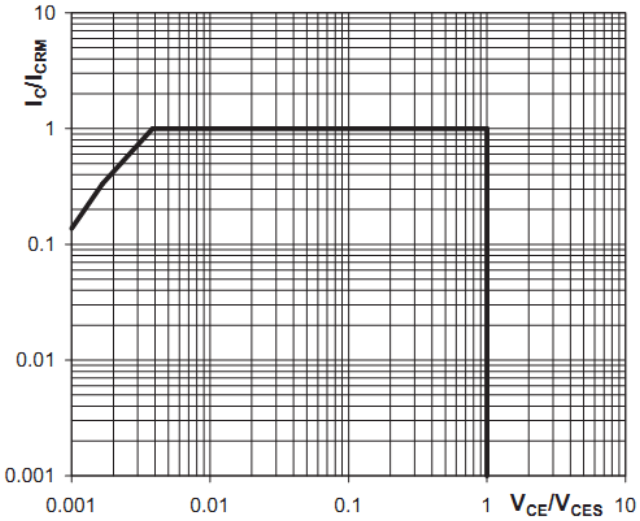
3.3.1 Safe Operating Area (SOA)

The safe operating area is defined as the voltage and current conditions for which the chip can be operated without self-damaging during switching on.
Figure 14 shows the maximum curve $I_C = f(V_{CE})$ during single-pulse operation using a double logarithmic scale. The graph in Figure 14 refers to the limiting values of V_{CES} and I_{CRM}:

- maximum collector current → horizontal limit
- maximum collector-emitter voltage → vertical limit

It is important that the maximum ratings apply to currents which do not heat the IGBT to temperatures above the maximum chip temperature T_j = 150°C or 175°C. Only during switching operation IGBT modules may touch the linear characteristic areas in the capacity of an active amplifier with $I_C = f(V_{CE})$. Analogous operation over a longer period of time is not permitted, since this would involve local overload due to the variation in the transfer characteristics among the IGBT cell or paralleled chips.

Figure 14: SOA IGBT



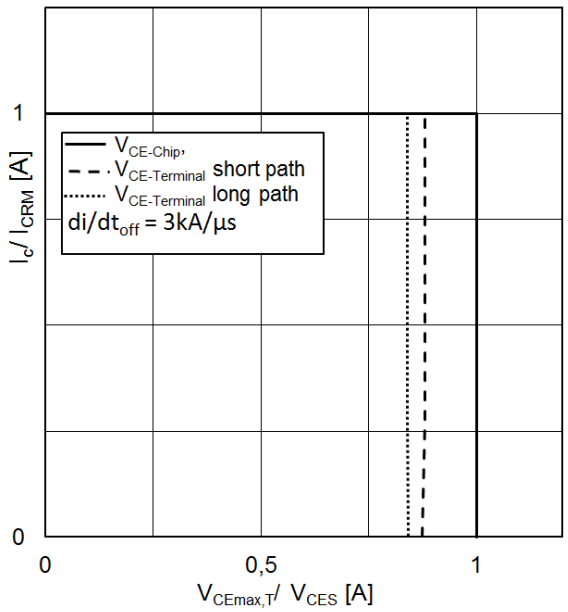
3.3.2 Reverse Bias Safe Operating Area (RBSOA)

Reverse Bias Safe Operating Area is the SOA curve during the device's turn-off state. Maximum V_{CES} must not to be exceeded during turn-off. Due to the internal stray inductance, collector-emitter voltage to terminals ($V_{CEmax,T}$) must be smaller than the collector-emitter voltage at chip level (V_{CEmax}).
The $V_{CEmax,T}$ can be calculated using the following formula

$$V_{CEmax,T} = V_{CES} - L_{CE} \cdot \frac{di}{dt_{off}} \qquad \textbf{3-1}$$

Maximum $\frac{di}{dt_{off}}$ has to be specified in the final application.
An example of RBSOA curve for SEMiX305MLI07E4 is shown in Figure 15.

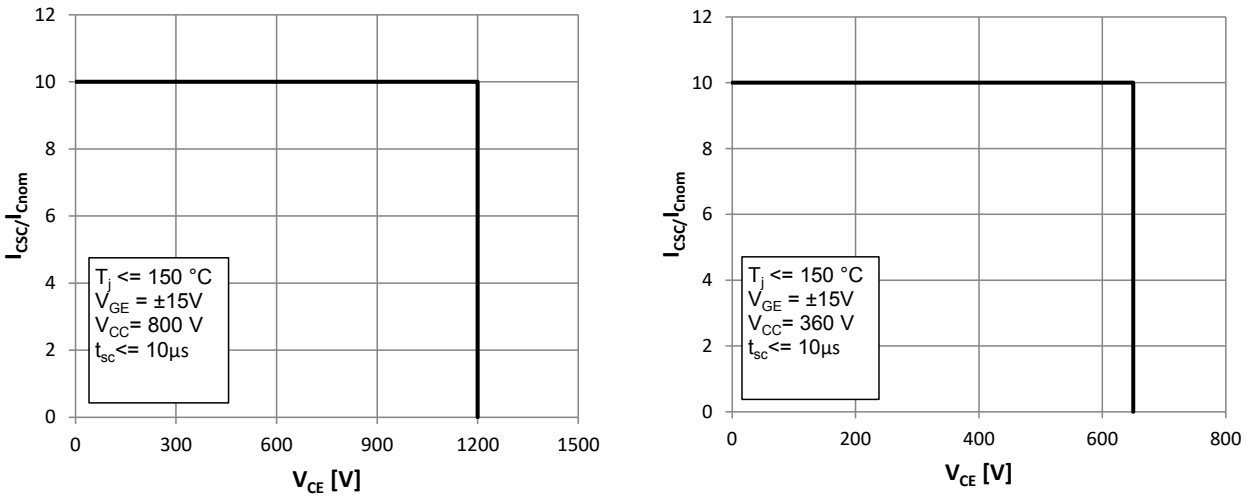
Figure 15: RBSOA IGBT for SEMiX305MLI07E4



3.3.3 Short Circuit Safe Operating Area (SCSOA)

Under certain conditions, the IGBT is essentially capable of turning off short circuits actively. In doing so, high power losses are generated by the IGBT working in the active operating area, causing a temporary increase in chip temperature far beyond $T_{j,max}$. However, the positive temperature coefficient of the collector-emitter voltage causes the circuit to stabilize and the short-circuit current is limited to 4..6 x I_{Cnom}. Figure 16 gives an example of the permissible SCSOA. Here it must be taken into consideration, that the maximum external voltage has to be reduced by the amount: $L\_s \cdot di/dt$.

Figure 16: SCSOA 1200V IGBT (left) and 650V IGBT (right)



The following boundary conditions need to be fulfilled for safe operation:

- the short circuit must be detected and turned off within max. 10µs for 1700V, 1200V and 650V IGBTs
- the time between two short circuits has to be at least 1s
- the IGBT must not be subjected to more than 1000 short circuits during its total operation time

3.3.4 Selection guide

The correct choice of the IGBT module depends very much on the application itself. A lot of different parameters and conditions need to be taken into account: V_{in}, I_{in}, V_{out}, I_{out}, f_{sw}, f_{out}, overload, load cycles, cooling conditions, etc.
Due to this variety of parameters a simplified selection guide is not seriously feasible. For this reason SEMIKRON offers the selection, calculation and simulation tool "SEMISEL" under http://semisel.semikron.com. Almost all design parameters can be edited for various input or output conditions. Different cooling conditions can be chosen and specific design needs can be effectively determined.

4. Thermal Resistances

The Thermal Resistance between two reference points is defined as given in the following equation:

$$R_{th(1-2)} = \frac{\Delta T}{P_V} = \frac{(T_1 - T_2)}{P_V} \qquad \textbf{4-1}$$

With respect to Figure 17 in the SEMiX®5 datasheets the following thermal resistances are specified

- For each IGBT- or diode
  - $R_{th(j-c)}$: Junction-to-Case thermal resistance per switch
  - $R_{th(c-s)}$: Case-to-sink thermal resistance per switch

- For the whole module
  - $R_{th(c-s)1}$: Thermal resistance of the module calculated without including thermal coupling
  - $R_{th(c-s)2}$: Thermal resistance of the module calculated with thermal coupling

Figure 17: Thermal resistances in a module with baseplate

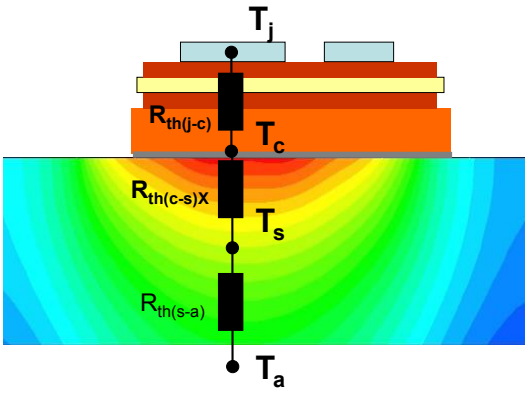
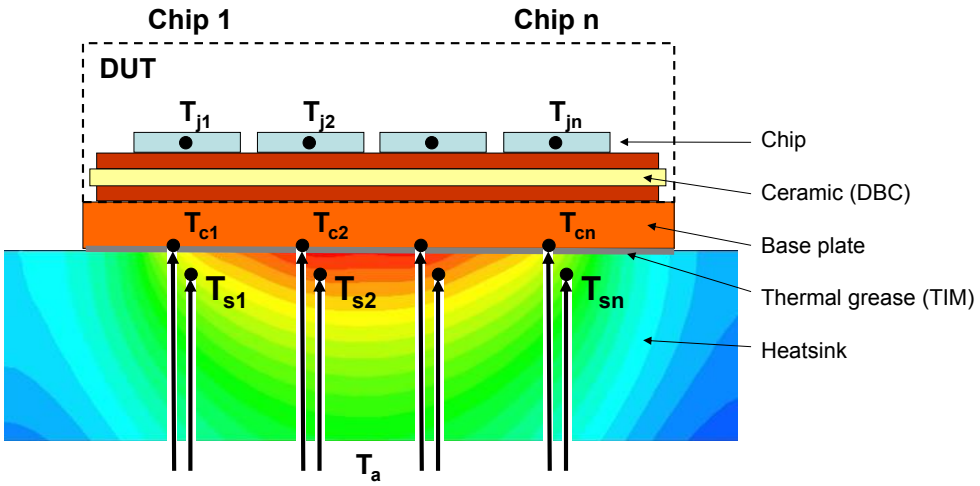


Figure 18: Reference points for temperature measurement of T_c and T_s [4]



The formulas to calculate the thermal resistances $R_{th(j-c)}$, $R_{th(c-s)}$ or $R_{th(j-s)}$ per switch or per module by using the temperature differences and power dissipation are derived by the measurements from above and are shown in Table 6. The variable X stands for IGBT or diode and is applicable to any other power semiconductor inside a module.

In all these definitions it is supposed to know the junction temperature of the chip T_j. This temperature cannot be measured in the most practical cases and can be calculated in a way proposed by IEC 60747 standard [6] called "V_0(T)-method". This method is applicable without special prepared modules When operating with a small measurement current, bipolar semiconductors show a linear dependency between the forward voltage drop and the chip temperature. A calibration curve $V_{ce}=f(T_j)$ or $V_f=f(T_j)$ is generated using this effect by passive heating and measuring the forward voltage at the measurement current and different temperatures. Then the switch device under test (IGBT or diode) is operated at a DC load current until thermal equilibrium is reached. The power dissipation is calculated by $P_X=V_X*I_{DC}$. After switching off the load current the small measurement current is applied again after few 100 µs and T_j can be derived using the measured voltage drop and the calibration curve.

Table 5 shows the definition of temperature reference points according IEC 60747-XX (for further details refers to [6] and [7])

Table 5: Definition of temperature reference points according IEC 60747-XX [6] [7]

Measured temperature	Symbol	Temperature reference point
junction temperature of chip 1 to reference point n	$T_{j1...n}$	determined for the chips by V_0(T) method for single chip IGBT- or diode. If one switch consists of 2 or more chips in parallel, then T_j represents an average temperature of the paralleled chips
case temperature below chip 1 to reference point n (e.g heat sink)	$T_{c1...n}$	The case temperature measured at a position underneath the chip in a 1…2.5 mm small hole through the heatsink
heatsink temperature below chip 1 to reference point n (e.g. ambient)	$T_{s1...n}$	T_s is taken from underneath through a 1…2.5 mm blind hole ending at 2±1 mm below the heatsink surface

Table 6: Definition of $R_{th(j-s)}$, $R_{th(j-c)}$ and $R_{th(c-s)}$	
per IGBT- or diode switch for modules with single chip switches	$R_{th(j-c)} = \frac{T_j - T_c}{P}$ $R_{th(c-s)X} = \frac{T_c - T_{s2}}{P}$
per IGBT- or diode switch of modules using n chips in parallel	$R_{th(j-c)} = \frac{T_j - \sum_{i=1}^{n} {T_{ci}}/{n}}{P}$ $R_{th(c-s)X} = \frac{\sum_{i=1}^{n} {T_{ci}}/{n} - \sum_{i=1}^{n} {T_{s2i}}/{n}}{P}$
per module M (losses $P_M=\Sigma P_m$) with n chips	$R_{th(c-s)M} = \frac{\sum_{i=1}^{n} {T_{ci}}/{n} - \sum_{i=1}^{n} {T_{s2i}}/{n}}{P_M}$

For heatsink temperature measurements the IEC 60747-15 [7] leaves two options, 1) on the heat sink surface close to the module or 2) in the heat sink from below the chip positions. For SEMiX5 the second method is used.

In IGBT modules multiple IGBT/diode chips may be used in parallel. Due to electrical and mechanical unbalances each chip has different power dissipation and its own individual temperature.

For determination of a switch-related case temperature it is necessary to measure T_{cn} under each chip and use the average T_c together with T_j to calculate the $R_{th(j-c)}$ per switch. Otherwise the thermal resistance will be position dependent and **the position underneath the hottest chip provides the smallest thermal resistance $R_{th(j-c)}$.**

It is necessary to measure case and/or heatsink temperature **underneath each chip** and use average values per switch for case and heatsink temperature. For this reason SEMIKRON uses module type specific liquid cooled heatsink with holes at each chip position

4.1 Effects of Mounting Conditions on $R_{th(j-s)}$ and $R_{th(c-s)}$

These thermal resistances depend on module assembly, e.g. screw tightening torque, heatsink performance and quality, thickness and heat conductivity of TIM. For specification of IGBT modules with baseplate the manufacturer uses not only different reference points but also different assumptions on thermal conductivity of TIM and quite different possibilities for specifying $R_{th(c-s)}$ with or without respect to thermal coupling of switches inside modules, see Table 7.

Table 7: $R_{th(c-s)}$ specifications from IGBT modules manufacturer's datasheets				
Manufacturer	**TIM thermal conductivity λ**	**Specification of $R_{th(c-s)}$ per IGBT/Diode**	**Specification of $R_{th(c-s)}$ per module**	**Including thermal coupling of switches**
SEMIKRON standard TIM	0.81 W/(m∗K)	x	x	Yes
SEMIKRON Phase Change Material	3.4 W/(m*K)	x	x	Yes
Infineon	1.0 W/(m∗K)	x	N.A	No
ABB Semiconductors	1.0 W/(m∗K)	x	N.A	No
Mitsubishi	0.9 / 1.0 W/(m∗K)	N.A	x	Yes
Fuji	no information	N.A	x	Yes

The $R_{th(c-s)}$ data sheet statement of SEMIKRON IGBT modules are valid only if the modules are mounted according to the mounting instructions using the specified thermal grease material and layer thickness. The power module should be stored a few days or a few temperature cycles should be done to reach a good distribution of the thermal grease. The values are measured at liquid cooled heatsinks, at less effective air cooled heatsinks the $R_{th(c-s)M}$ is lower due to a wider heat spreading inside the module.

Further details on the thermal resistance of IGBT modules can be found in [8].

5. Integrated Temperature Sensor Specifications

All SEMiX®5 IGBT modules feature a temperature-dependent resistor for temperature measurement. The resistor is soldered onto the same DBC ceramic substrate near IGBT and diode chips. It is necessary to evaluate the dependency between the temperatures of interest (e.g. chip temperature) and the signal from the integrated temperature sensor.

5.1 Electrical characteristics

The built-in temperature sensor in SEMiX®5 modules is a resistor with a negative temperature coefficient (NTC) and has a nominal resistance of 5kΩ at 25°C and 0.493 kΩ at 100 °C. Its characteristic is given in Figure 19 and Figure 20. The ohmic resistance values of the sensor (min., typ., max.) are given as a function of temperature in Table 8 .

A mathematical approximation (in the range from 80°C to 150°C) for the sensor resistance as a function of temperature R(T) is given by:

$$R(T) = R_{100} \cdot e^{[B_{100/125} \cdot \left(\frac{1}{T} - \frac{1}{T_{100}}\right)]}$$

With:

- R_{100} = 493Ω
- $B_{100/125}$ = 3550K
- T_{100} = 100°C = 373.15K

$$R(T) = 493\Omega \cdot e^{[3550K \cdot \left(\frac{1}{T} - \frac{1}{373.15K}\right)]}$$

Figure 19: Typical characteristic of the NTC temperature sensor included in SEMiX modules

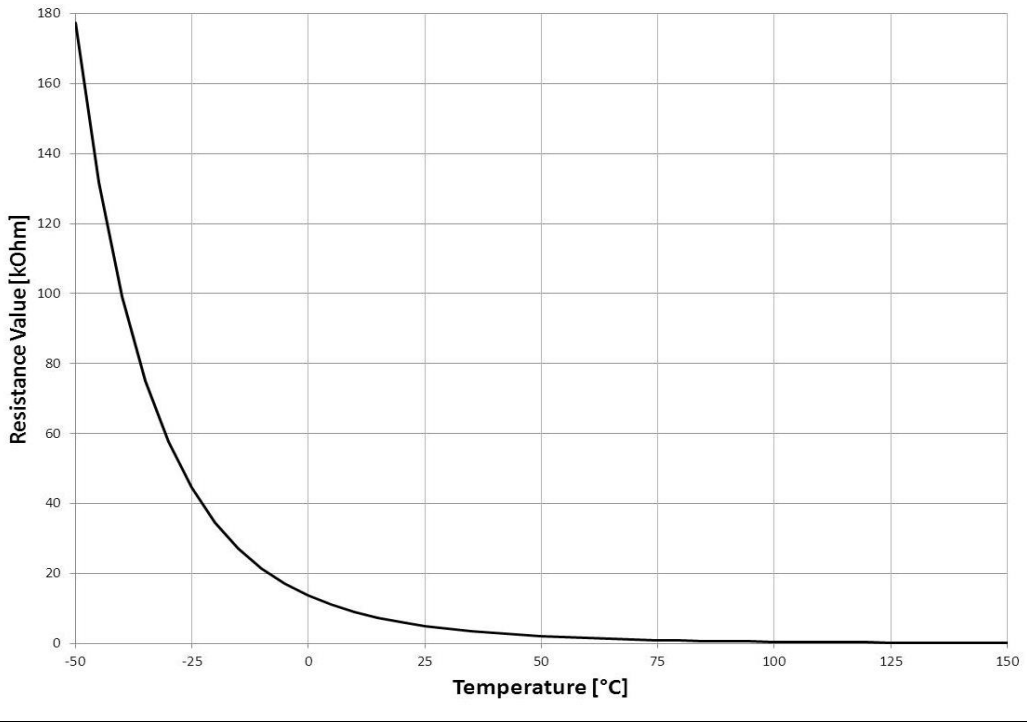


Figure 20: NTC temperature sensor characteristic including tolerances

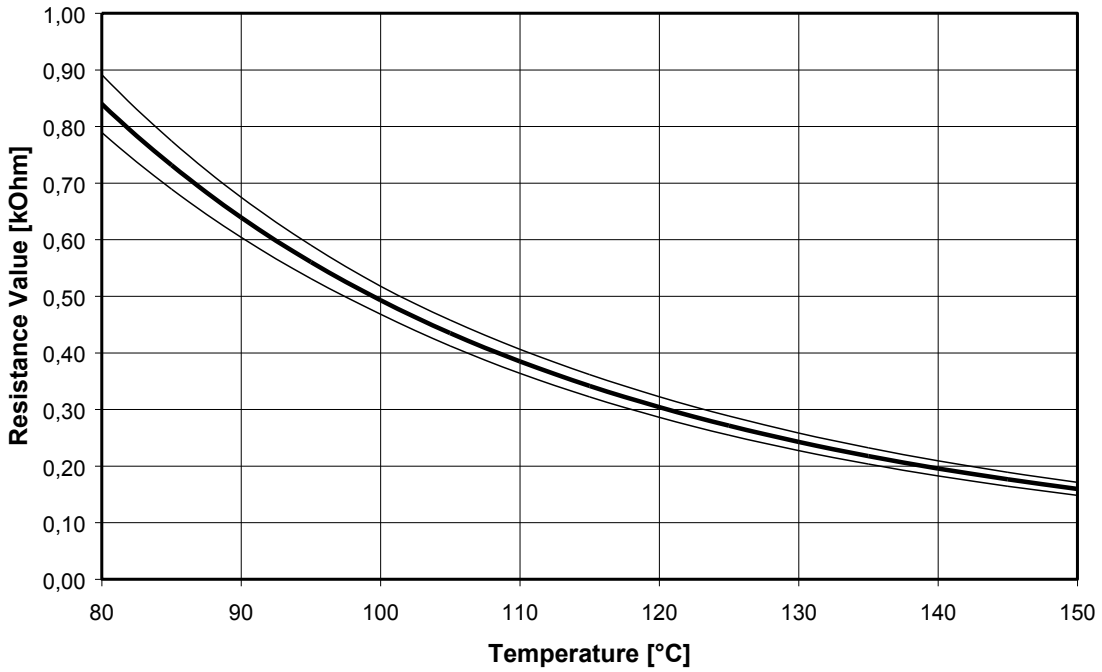
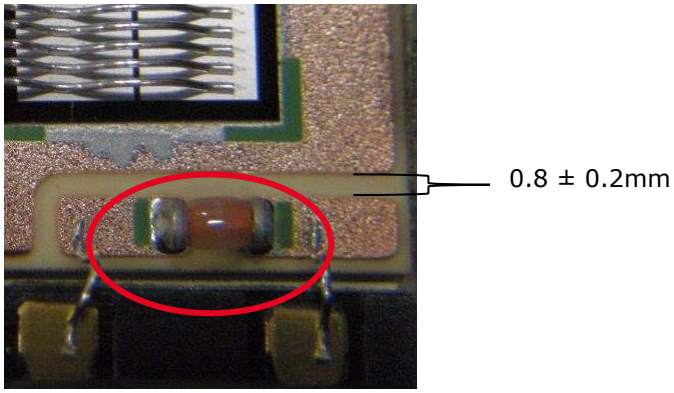


Table 8: Resistance values and tolerance as given by the supplier				
Temperature	**Resistance Value**			**Tolerance** maximum deviation [%]
[°C]	minimum [kΩ]	standard [kΩ]	maximum [kΩ]	
-50	148.183	177.265	211.525	20.2
-40	83.924	99.034	116.572	18.5
-30	49.348	57.508	66.850	16.2
-20	30.019	34.582	39.738	14.9
-10	18.832	21.465	24.404	13.7
0	12.151	13.713	15.438	12.6
10	8.044	8.995	10.034	11.6
20	5.452	6.045	6.685	10.6
30	3.776	4.153	4.557	9.7
40	2.668	2.913	3.172	8.9
50	1.920	2.082	2.251	8.1
60	1.406	1.514	1.626	7.4
70	1.046	1.119	1.195	6.8
80	0.789	0.840	0.891	6.1
90	0.604	0.639	0.675	5.6
100	0.468	0.493	0.518	5.0
110	0.364	0.385	0.406	5.5
120	0.286	0.304	0.322	6.0
130	0.227	0.243	0.258	6.5
140	0.183	0.196	0.209	7.0
150	0.148	0.159	0.171	7.4

5.2 Electrical isolation

Inside SEMiX®5 modules the temperature sensor is mounted close to the IGBT and the diode dies on the same substrate. The minimum distance between the copper conductors is 0.80 ± 0.2mm (Figure 21)

Figure 21: SEMiX®5 NTC temperature sensor position

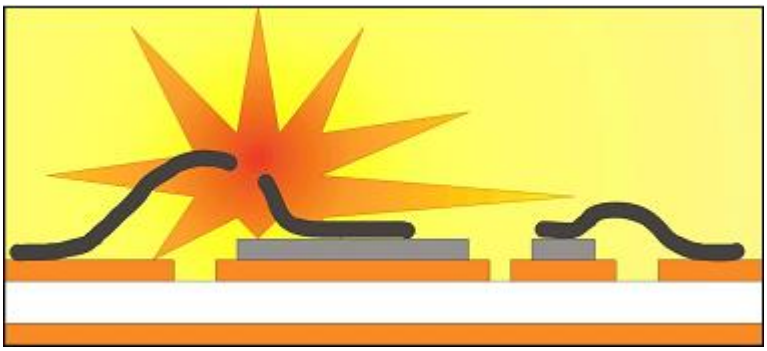


SEMiX®5 module is filled with silicone gel for isolation purpose, so the requirement for the specified isolation voltage (AC 4 kV for 1 min) are met and 100% tested,

According to EN 62477-1, this design does not provide "Safe Electrical Insulation", because the temperature sensor inside the SEMiX®5 module might be exposed to high voltages during semiconductor short-circuit failure mode. After electrical overstress the bond wires could melt off, producing an arc with high-energy plasma in the process (as shown in Figure 22). In this case the direction of plasma expansion is unpredictable and the temperature sensor might come into contact with the plasma and be exposed to high voltage level.

The safety grade "Safe Electrical Insulation" in accordance with EN 62477-1can be achieved by different additional means, which are described in this EN standard in more detail.

Figure 22: Sketch of high energy plasma caused by bond wire melting



6. Reliability

6.1 Standard tests for the qualification of SEMiX®5 platform

The objectives of the test program are:

1. Ensure the general product quality and reliability
2. Evaluate design limits by stressing under a variety of testing conditions
3. Ensure the consistency and predictability of the production processes
4. Appraise process and design changes regarding their effect on reliability

Table 9: SEMIKRON qualification tests for SEMiX®5

Test Description	Conditions
High Temperature Reverse Bias (HTRB) IEC 60747-9:2007	1000h
	95% $V_{CE\ max}$
	$T_{j\ max}$
High Temperature Reverse Bias (HTRB) * IEC 60747-2:2016	1000h
	66% V_{RRM}
	$T_s = T_{j\ max} - 20K$
High Temperature Gate Stress (HTGS) IEC 60747-9:2007	1000h
	$\pm V_{GES\ max}$
	$T_{j\ max}$
High Humidity High Temperature Reverse Bias (H3TRB) EN 60749-5:2018, EN 60068-2-67:1996	1000h
	T_a = 85°C, RH = 85%
	V_{CE} = max. 80V
High Voltage - High Humidity High Temperature Reverse Bias (HV-H3TRB) ** EN 60749-5:2018	168h
	T_a = 85°C, R_H = 85%
	80% $V_{CE\ max}$
High Temperature Storage (HTS) *** EN 60068-2-2:2008, IEC 60749-6:2002	1000h
	$T_{stg\ max}$
Low Temperature Storage (LTS) *** EN 60068-2-1:1993 + A1:1993 + A2:1994	1000h
	$T_{stg\ min}$
Thermal Cycling (TC) EN 60068-2-14:2010	100 cycles
	$T_{stg\ max}$ - $T_{stg\ min}$
Vibration IEC 60068-2-6:2008	20Hz … 500Hz Sinusoidal sweep
	5g
	2h per axis (x, y, z)
Mechanical Shock IEC 60068-2-27:2010	Half sine pulse 18ms
	30g
	3 times each direction (±x, ±y, ±z)
Power Cycling (PC)	20k cycles at ΔT= 100K

EN 60749-34:2010	
Power Cycling * (PC) EN 60749-34:2010	10k cycles at ΔT= 100K

*) Valid for standard glass passivated rectifier diodes and thyristors.
**) Valid for IGBT "M7" generation.
***) Module without TIM
SEMiX®5 modules can be subjected on demand to additional tests, as follows.

- Salt Spray Test according mil-std-810F method 509.4 +JESD22-a107-a
- Corrosive Atmosphere test according to DIN EN 60068-2-60Ke method 3 including SO_2 in addition to H_2S, NO_2 and Cl_2.

Test level may vary, depending on module layout and technology.

6.2 Lifetime calculation

Lifetime of power modules is limited by mechanical stress that occurs among the different materials of the package during operation. These mechanical stress is due to the different CTEs (Coefficients of thermal expansion) of such materials. This means that in the course of heating (power on) and cooling (power off) = temperature swing (power cycle), the materials try to expand differently on account of their different CTEs. A cross section view of SEMiX®5 package, including the coefficients of thermal expansion at 20°C is provided in Figure 23.
Since the materials are mechanically joined thermally induced mechanical stress occurs.

Result is that after a certain number of power cycles the module fails. One of the typical failure modes is the wire bond "lift off", that means contact between chip (or DBC copper) and wire bonds is lost (Figure 24).

In the 90's intensive investigations were carried in this area including a research project known as "LESIT study". This study puts in evidence the relationship between the number of load cycles Nf, the junction temperature difference DT and the medium temperature Tm. (For better understanding see also Figure 25 and Figure 26).

$$N_f = A \cdot \Delta T_j^{\alpha} \cdot e^{\left(\frac{E_a}{k_B \cdot T_m}\right)} \qquad \textbf{6-1}$$

with:
N_f = number of load cycles til failure
k_B = Boltzmann-constant ($1.380 \cdot 10^{-23}$J/K)
E_a = activation energy ($9.891 \cdot 10^{-20}$J)
A = constant (648000 $K^{-\alpha}$)
α = constant (-5.039)
T_{jm} = medium junction temperature [K]

Figure 23: Cross sectional view of SEMiX package, including the coefficients of thermal expansion (at 20 °C)

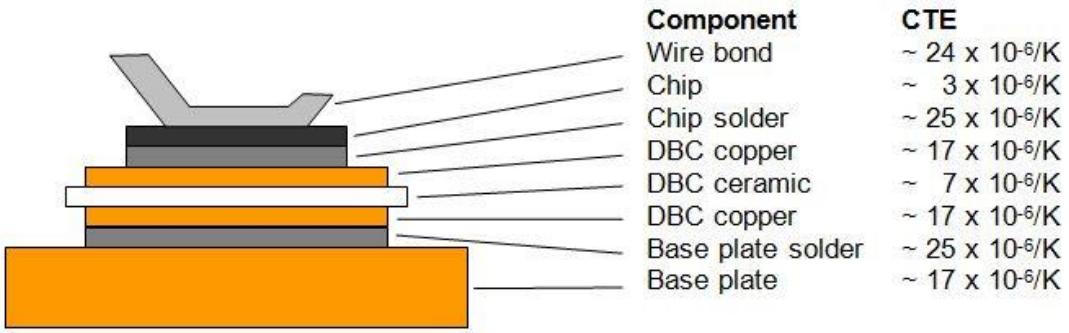


Figure 24: Typical wire bonding lift-off observed by an electron microscope

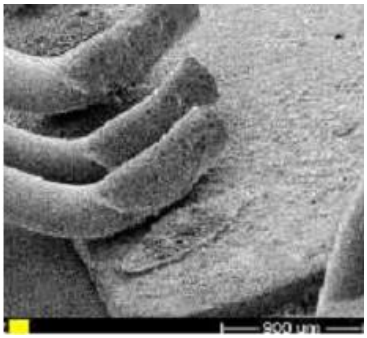
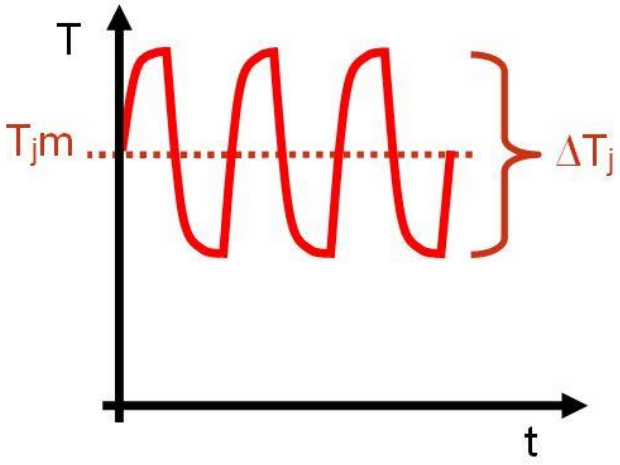


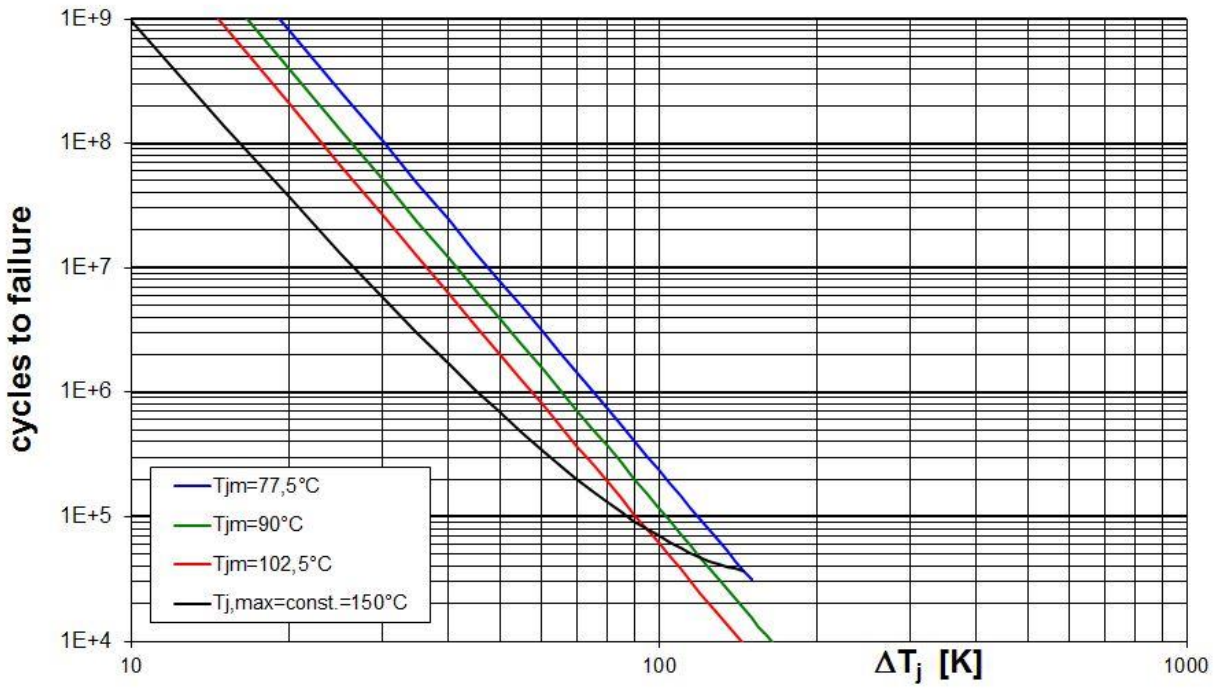
Figure 25: Example of $T_j m$ and ΔT_j



SEMiX® modules are based on the same design principles as the modules which were investigated in the course of the LESIT study. For this reason equation 6-1 may be used for life time estimations. Note that the reliability of power modules has improved since the LESIT study was concluded and thus the coefficients in equation 6-1 have been adjusted.

The power cycling diagram in Figure 26 shows the number of load cycles til failure as a function of the junction temperature swing with the average temperature T_{jm} as additional parameter. The given number of cycles represents a 1% failure probability.

Figure 26: Power cycling lifetime as a function of ΔT_j and T_{jm}



7. Marking

7.1 Laser Data Matrix code marking of modules

All SEMIKRON modules are lasered with a Data Matrix Code. The Data Matrix Code type EEC 200 according to ISO/IEC 16022 with a cell size of 0.46mm and a field size of 24x24 is used. The code has a size of 11x11mm and a guard zone of 1mm. Code structure provided 53 digits (which is common to all SEMIKRON standard modules). The contents is left- justified and missing characters are filled with blanks.

SEMIKRON recommends to use as Data Matrix Code Reader the Lynx D302 from DATALOGIC. This device works in reading distances between 45 and 165 mm.

An example of SEMiX405TMLI12E4B datamatrix code is provided in Figure 30.
The 5 digits data code indicates

- YY: Production Year
- WW: Production Week
- Lot of same type per week (counting starts from 0)

The data code might be followed by

- "R" to indicate that the module complies with the RoHS directive

SEMiX®5 has two adhesive tags which are shown in **Errore. L'origine riferimento non è stata trovata.**

Adhesive Tag 1 contains SEMIKRON logo, SEMiX®5 family name and Product Type Name (Figure 29 left)

Adhesive Tag 2 contains the 5 digits data code (described previously) and UL logo (Figure 29 right).

The Data Matrix of SEMiX®5 is indicated in Figure 30 and it is defined as follows:

- Lines: 26
- Capacity: 53 characters
- Datamatrix size = 8.0x8.0 mm^2
- Dot size: 0.30mm
- Dot number: 26 x 26

- Total size = 8.0x8.0 mm^2

7.1.1 Samples

Evaluation, engineering and application samples are marked "ES" on the module (see Figure 31). For the type of sample please refer to the accompanying documents.

Figure 27: SEMiX405TMLI12E4B Data Matrix Code

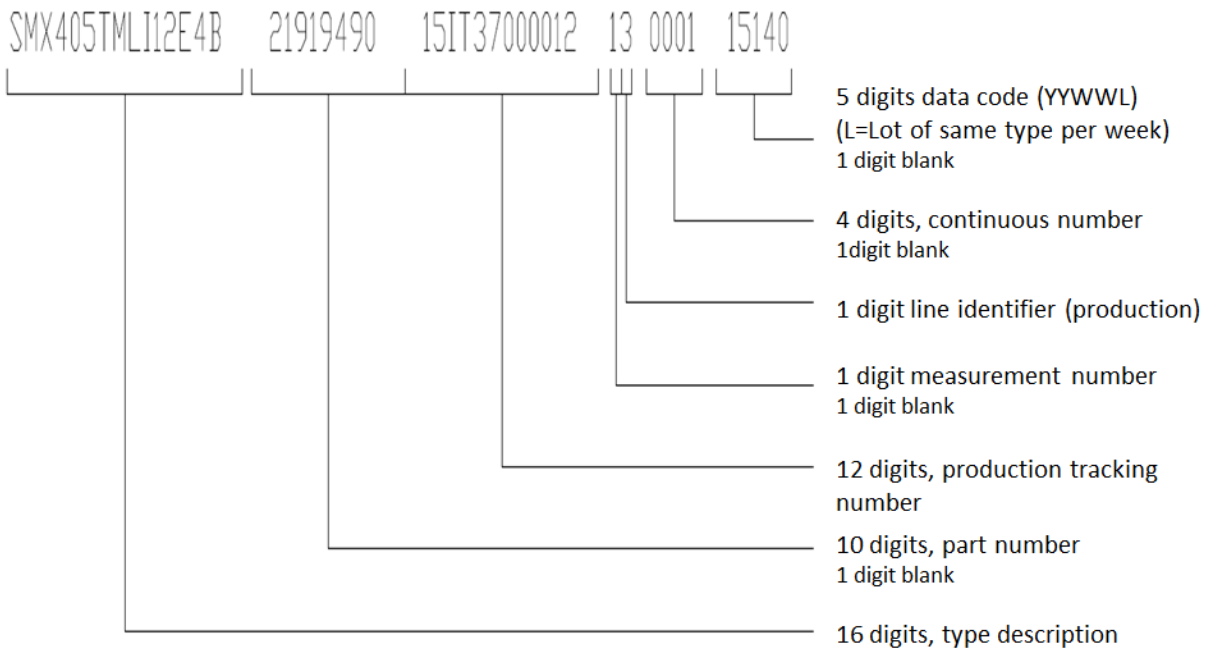


Figure 28: Positioning of adhesive tags 1 and 2

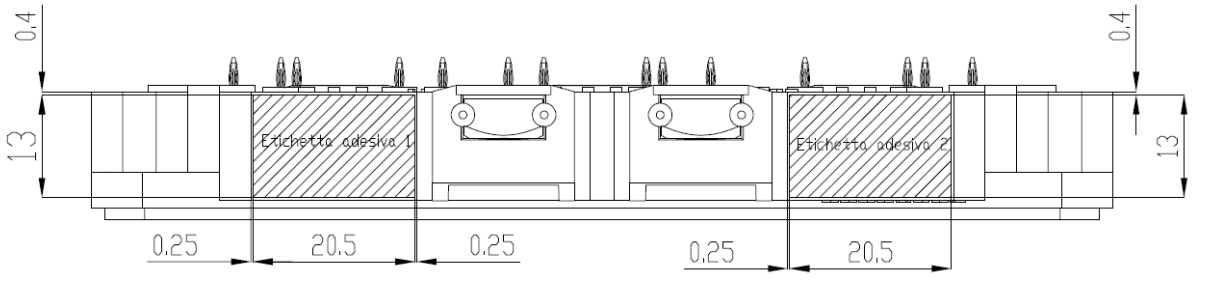


Figure 29: Details Tag1 and Tag2

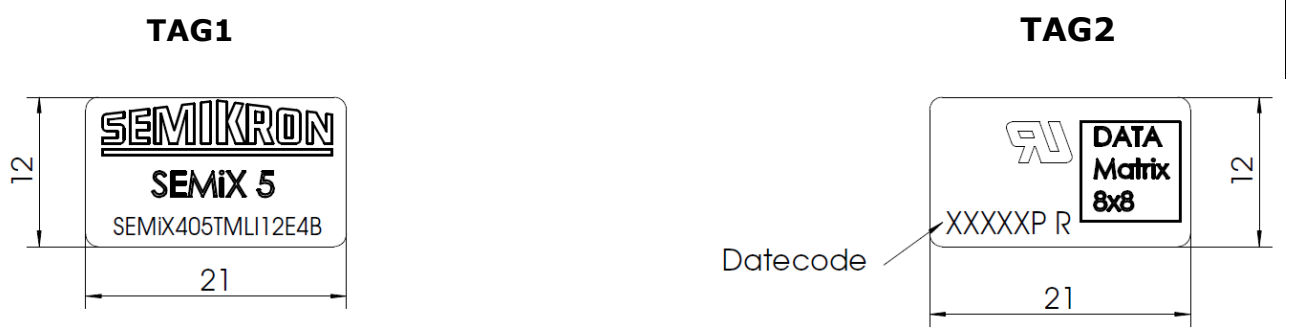


Figure 30: SEMiX®5 Data Matrix

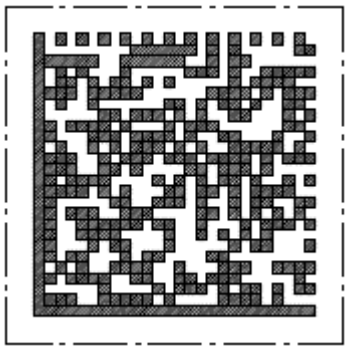


Figure 31: SEMiX®5 Example of Evaluation or Engineering or Application Sample

8. Packaging Specifications

8.1 Packaging box and blister/ ESD cover

Please see SEMiX®5 Mounting Instructions

8.2 Marking of packaging boxes

8.2.1 Description label

Two labels can be found on paper box

- **White label**: information about product. Details about label content can be found here:
  - Labeling of SEMIKRON product packaging

8.2.2 Date code example

Example Datecode IT210300
IT: italia
21: 2021 (year)
03: week 03
00 : lot number in progressive
P: Pomezia (Factory)
R: Rohs

8.2.3 ESD Label

- **Yellow label**: warning for electrostatic sensitive devices.

In Figure 32 is indicated ESD label with its size

Figure 32: ESD label on SEMiX®5 box

dimension: 105 x 26 mm^2

8.3 Storage Conditions

SEMiX®5 products are qualified according to IEC 60721-3-1 and can therefore be stored in original package for maximum 2 years starting from date code under climatic class 1K2. So the following frame conditions apply

Table 10: Storage conditions	
Storage temperature	5°C … 40°C
Relative humidity	5% … 85%
Duration	2 years
Climatic class	1K2 (IEC 60721-3-1)
Condensation	Not allowed at any time

SEMiX®5 products have been tested for climatic conditions in their original packaging. Packaging is very often limiting the allowed climatic conditions. So there are less restrictive conditions for the products itself. Due to our experience the temperature range mentioned in IEC 60721-3-1 for 1K2 can be enlarged for transportation and storage. So the following conditions are possible [1] :

Table 11: Shelf life conditions	
Relative humidity	Max. 85%
Storage temperature	-25°C … +60°C
Condensation	Not allowed at any time
Storage time	Max. 2 years

Please note that a higher temperature load can decrease storage time, in extreme cases down to half a year.

More restrictive storage conditions for products with pre-applied thermal interface material may apply and are mentioned in the dedicated documentation.

9. Material Content Data Sheet (MCDS)

A detailed MCDS is available for SEMiX®5 in SEMIKRON web site.

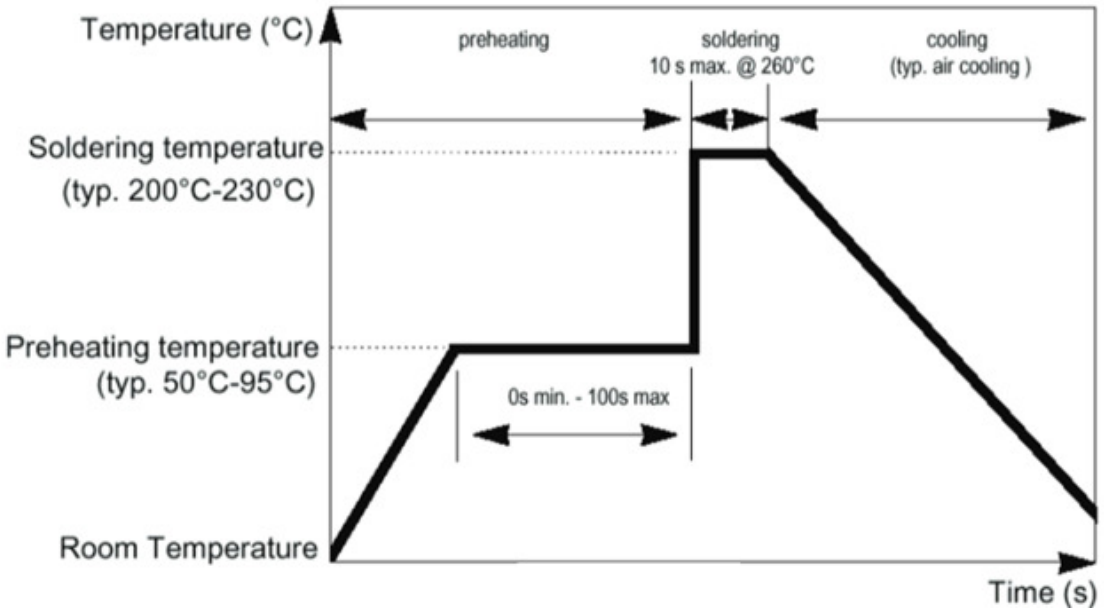
[1] These conditions have not explicit been tested by Semikron

10. Soldering pins

Despite the press-FIT technology SEMiX®5 press-FIT pins can be soldered to.

SEMIKRON recommends to use wave soldering. Soldering temperature, please refer below curve in the following figure, the temperature measured at modules' pins

Figure 33: Wave Soldering Temperature Profile for SEMIKRON power module



If use Iron soldering, please see refer below recommendations

- Soldering iron: 90W antistatic thermostat soldering iron;
- Solder wire: KESTER245 clean-safe solder wire, diameter is 1 mm;
- Solder temperature: 390±10 ,maximum 400 ;
- Solder time: 4±1s for one welding spot; 8±2s for welding spot with connected double pins; =40s for welding spot with three pins.
- Amount of solder wire: no exceeding 10mm for one welding spot (exclude the Solder adsorbing at the head of iron)
- Welding quality: good welding surface wetting for repair welding, no solder penetration onto the surface of IGBT.

To judge if the soldering effect is good please refer to norm **IPC-A-610E** – Acceptability of Electronic Assemblies (2010), chapter ref: **4.3.2.1 Press Fit Pins Soldering**

11. Environmental conditions

11.1 Climatic conditions, air humidity limits

Climatic conditions include air temperature, absolute and relative air humidity, condensation rate of temperature change, barometric pressure, solar and thermal radiation, air movement, wind driven rain, water (except for rainfall) and ice formation.

Most of SEMIKRON power modules, including SEMiX®5, conform to climate class 3K3 as per EN 60721-3-3 in compliance with the 62477-1 and, with regard to clearance and creepage distances, may be operated under pollution degree 2 conditions stipulated by 62477-1 and EN 61800-5-1

We remind the 3K3 climate classes as defined: Closed locations, with air temperature regulation, non-regulated air humidity, condensation ruled out.

Silicone-based single-layer coating and encapsulation system provide protection against humidity level but does not provide a sealed barrier. The speed of diffusion of water ions in the silicone gel is not zero and depend by the environmental condition. For instance amounts to 0.04 mm/s at 18°C, increasing up to 1 mm/s at 100°C. For silicon layers of approx. 5 mm in thickness, the saturation state is reached within 5 hours.

Accordingly, operation is not permitted in places of operation or installation where dripping or condensation water impacts on the power modules for example. Condensation is admissible occasionally only, and on provision that the system is not under voltage. Under no circumstances may condensation residue resulting from occasional condensation be allowed to accumulate due to frequent condensation/drying cycles.

To prevent power semiconductors failure due to condensation, applications must comply with the component-specific climatic requirements. For operation, additional anti-condensation measures such as standstill heating, air conditioning, continuous duty, cooling water temperature etc. must be taken.
According to climate class 3K3, operation must take in place in shielded locations which must not be exposed to weather and which have a maximum relative humidity of 85% and absolute air humidity of 26 g/m^3 . At 40°C, for example, the relative air humidity must not exceed 50%. Further details can be founded in [2].

Please contact your local Semikron representative to get support in case you have further questions on this topic.

12. Figure captions in the Datasheets

12.1 SEMiX®5 TMLI

Table 12: Figure captions in the datasheet of SKiM4 TMLI	
Fig. 1	Typical IGBT1 output characteristic, incl $R_{CC'+EE'}$
Fig. 2	IGBT1 rated current vs. temperature $I_C = f(T_c)$
Fig. 3	Typical IGBT1 & Diode2 turn-on/-off energy = $f(I_C)$
Fig. 4	Typical IGBT1 & Diode2 turn-on/-off energy = $f(R_G)$
Fig. 5	Typical IGBT1 transfer characteristic
Fig. 6	Typical IGBT1 gate charge characteristic
Fig. 7	Typical IGBT1 switching times vs. I_C
Fig. 8	Typical IGBT1 switching times vs. gate resistor R_G
Fig. 9	Transient thermal impedance of IGBT1 & Diode2
Fig. 10	Diode2 forward characteristic, incl $R_{CC'+EE'}$
Fig. 11	Typ. Diode2 peak reverse recovery current
Fig. 12	Typ. Diode2 recovery charge
Fig. 13	Typical IGBT2 output characteristic
Fig. 14	IGBT2 rated current vs. temperature $I_C = f(T_c)$
Fig. 15	Typical IGBT2 & Diode1 turn-on/-off energy = $f(I_C)$
Fig. 16	Typical IGBT2 & Diode1 turn-on/-off energy = $f(R_G)$
Fig. 17	Typical IGBT2 transfer characteristic
Fig. 18	Typical IGBT2 gate charge characteristic
Fig. 19	Typical IGBT2 switching times vs. I_C
Fig. 20	Typical IGBT2 switching times vs. gate resistor R_G
Fig. 21	Transient thermal impedance of IGBT2 & Diode1
Fig. 22	Diode1 forward characteristic, incl $R_{CC'+EE'}$
Fig. 23	Typ. Diode1 peak reverse recovery current (if present)
Fig. 24	-

12.2 SEMiX®5 MLI

Table 13: Figure captions in the datasheet of SKiM4 MLI	
Fig. 1	Typical IGBT1 output characteristic, incl $R_{CC'+EE'}$
Fig. 2	IGBT1 rated current vs. temperature $I_C = f(T_c)$
Fig. 3	Typical IGBT1 & Diode5 turn-on/-off energy = $f(I_C)$
Fig. 4	Typical IGBT1 & Diode5 turn-on/-off energy = $f(R_G)$
Fig. 5	Typical IGBT1 transfer characteristic
Fig. 6	Typical IGBT1 gate charge characteristic
Fig. 7	Typical IGBT1 switching times vs. I_C
Fig. 8	Typical IGBT1 switching times vs. gate resistor R_G
Fig. 9	Transient thermal impedance of IGBT1 & Diode5
Fig. 10	Diode5 forward characteristic, incl $R_{CC'+EE'}$
Fig. 11	*Typ. Diode5 peak reverse recovery current (under request)*
Fig. 12	*Typ. Diode5 recovery charge (under request)*
Fig. 13	Typical IGBT2 output characteristic, incl $R_{CC'+EE'}$
Fig. 14	IGBT2 rated current vs. temperature $I_C = f(T_c)$
Fig. 15	Typical IGBT2 & Diode1 turn-on/-off energy = $f(I_C)$
Fig. 16	Typical IGBT2 & Diode1 turn-on/-off energy = $f(R_G)$
Fig. 17	Typical IGBT2 transfer characteristic
Fig. 18	Typical IGBT2 gate charge characteristic
Fig. 19	Typical IGBT2 switching times vs. I_C
Fig. 20	Typical IGBT2 switching times vs. gate resistor R_G
Fig. 21	Transient thermal impedance of IGBT2 & Diode1 and Diode2
Fig. 22	Diode1 & Diode 2 forward characteristic, incl $R_{CC'+EE'}$
Fig. 23	*Typ. Diode1 peak reverse recovery current (under request)*
Fig. 24	*Typ. Diode5 recovery charge (under request)*

Symbols and Terms

Letter Symbol	Term

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors" [2]

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HISTORY

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