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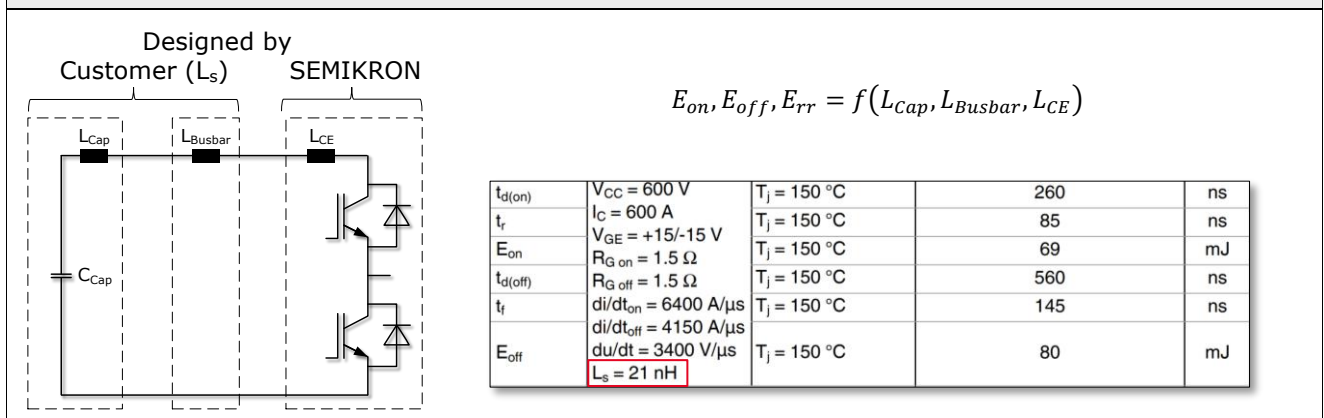
Influence of DC-Link Inductance on Switching Performance and Power Losses

1. Introduction.....	1
2. Device Under Test and Test Setup	2
3. Influence of L_s on Switching Performance and Power Losses	3
3.1 Overview.....	3
3.2 Influence of L_s on power losses	3
3.2.1 Influence of L_s on IGBT turn-on losses E_{on}	3
3.2.2 Influence of L_s on IGBT turn-off losses E_{off}	4
3.2.3 Influence of L_s on IGBT total losses E_{sw}	4
3.2.4 Influence of L_s on diode turn-off losses E_{rr}	5
3.3 Influence of L_s on overvoltage.....	5
3.3.1 Influence of L_s on IGBT overvoltage during Turn-off	5
3.3.2 Influence of L_s on diode overvoltage during turn-off	6
3.4 Influence of L_s on delay times	6
3.4.1 Influence of L_s on turn-on delay time $t_{d,on}$	6
3.4.2 Influence of L_s on turn-off delay time $t_{d,off}$	7
3.5 Influence of L_s on diode reverse recovery behavior	7
3.5.1 Influence of L_s on maximum reverse recovery peak current I_{rrm}	7
4. 3-Level Topologies based on Standard Half-Bridge Modules	8
4.1 NPC topology based on SEMiX3p	8
4.2 Commutation loops	8
4.2.1 Commutation loops at power factor = 1	8
4.2.2 Commutation loops at power factor = -1.....	9
5. Summary	10

1. Introduction

The power dissipation E_{on}/E_{off} of the IGBT and E_{rr} of the diode specified in the data sheets are measured under certain parameters. In addition to parameters such as the DC-Link voltage, current, junction temperature, gate resistance and gate-emitter voltage, the losses also depend on the inductance of the commutation loop. Figure 1 shows the three main inductive parameters of the commutation loop as centered elements using a simplified inductive equivalent circuit diagram. The power module shown as a half-bridge has an internal module inductance L_{CE} . The DC-Link inductance L_s consists of the internal inductance of the DC-Link capacitors L_{Cap} and the busbar inductance L_{Busbar} . These two quantities are determined by the type of capacitor, the number of capacitors connected in series and in parallel and the busbar design. This inevitably leads to different DC-Link inductances L_s used at Semikron Danfoss and at the customer. The aim of this Application Note is to illustrate the influence of the DC-Link inductance L_s on the power losses and the switching behavior. Furthermore, measures to reduce overvoltage when using standard half-bridge modules to build a NPC 3-level topology are presented.

Figure 1: Definition of L_s



2. Device Under Test and Test Setup

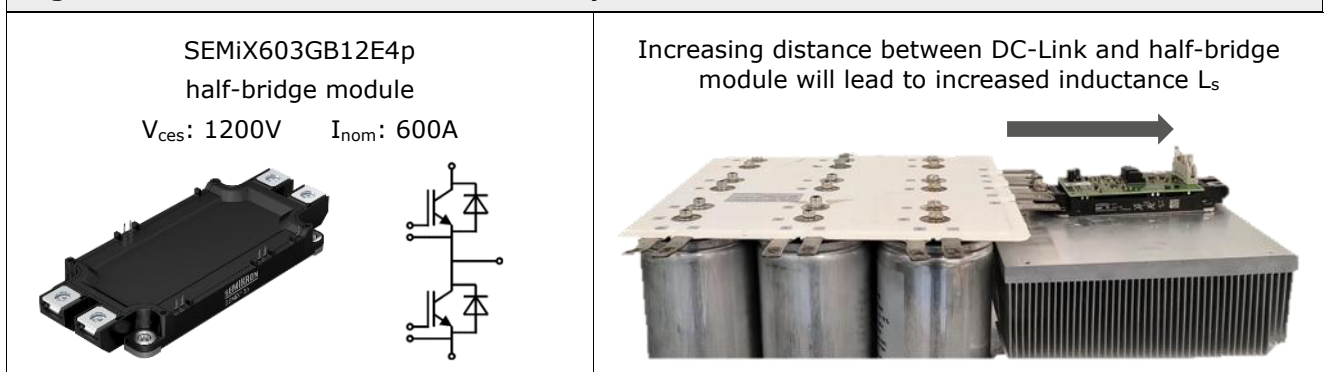
As shown in Figure 2, the device under test is a 600A/1200V rated power module SEMIX603GB12E4p [2] that belongs to the SEMIX3p product family. It is a standard half-bridge module consisting of a TOP and BOT IGBT/Diode. It uses IGBT E4 and Diode CAL4F technology.

For the test setup 12 capacitors (type: EPCOS 420uF B2520-B1227-A101) are connected in parallel that form together with the laminated busbar the DC-Link. The power module is mounted on a heatsink and screwed to the DC-Link. The DC-Link inductance L_s is increased by increasing the distance between the DC-Link and the power module. This Application Note examines the switching behavior and losses for the following DC-Link inductances: $L_s=35/60/85\text{ nH}$

The investigations at very high DC-Link inductances ($L_s=85\text{ nH}$) are mainly used to illustrate the challenges of overvoltage issues of 3-level topologies based on standard half-bridge modules.

The statements on DC-Link inductances can be transferred to other current ratings if the inductance per ampere is considered. Thus, a 60nH inductance for a 600A rated module would be comparable to 120nH inductance for a 300A rated module.

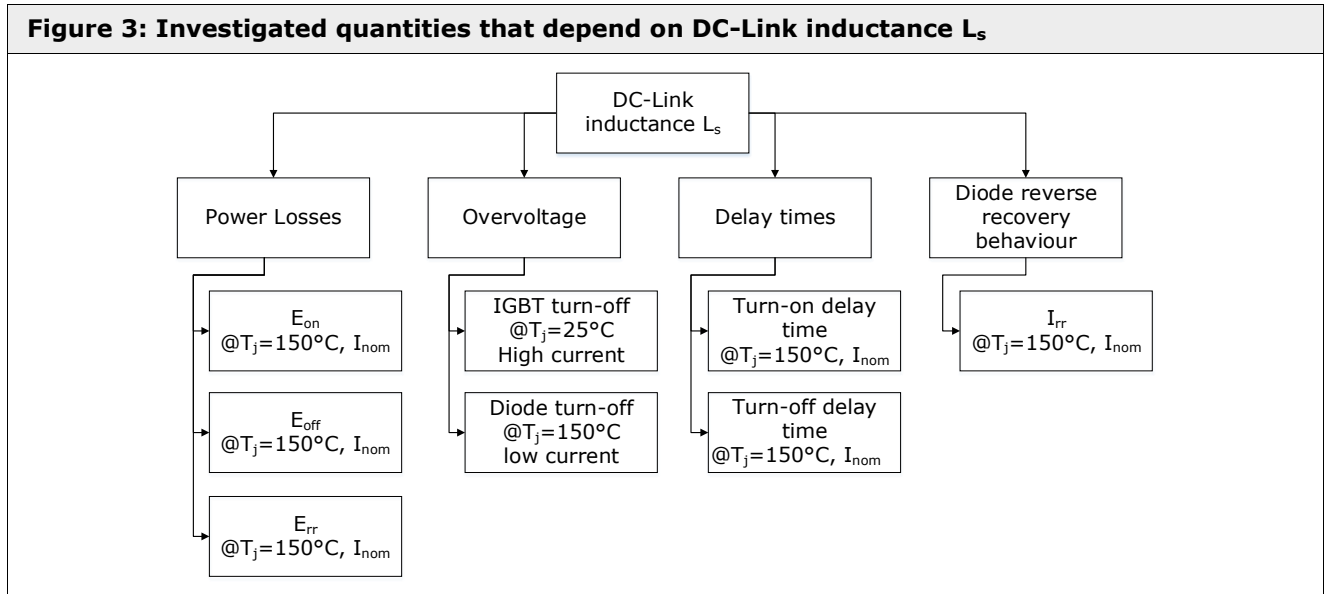
Figure 2: Device Under Test and Test setup



3. Influence of L_s on Switching Performance and Power Losses

3.1 Overview

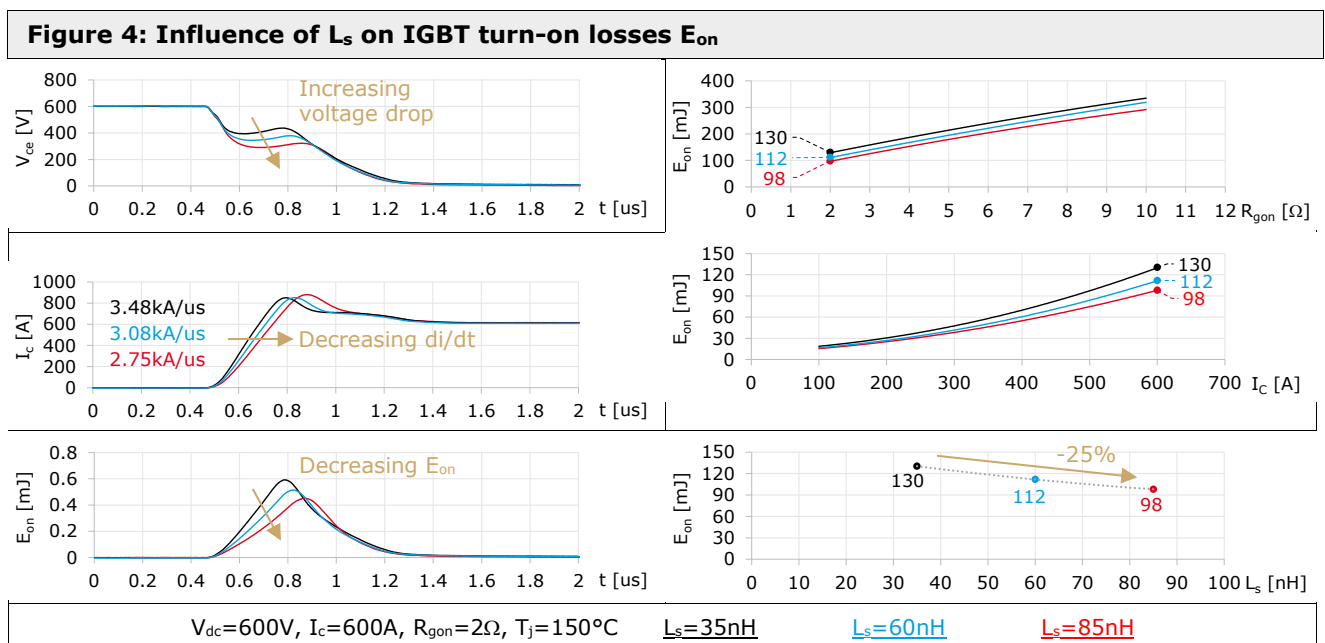
Figure 3 shows the quantities whose dependence on L_s is discussed in this Application Note.



3.2 Influence of L_s on power losses

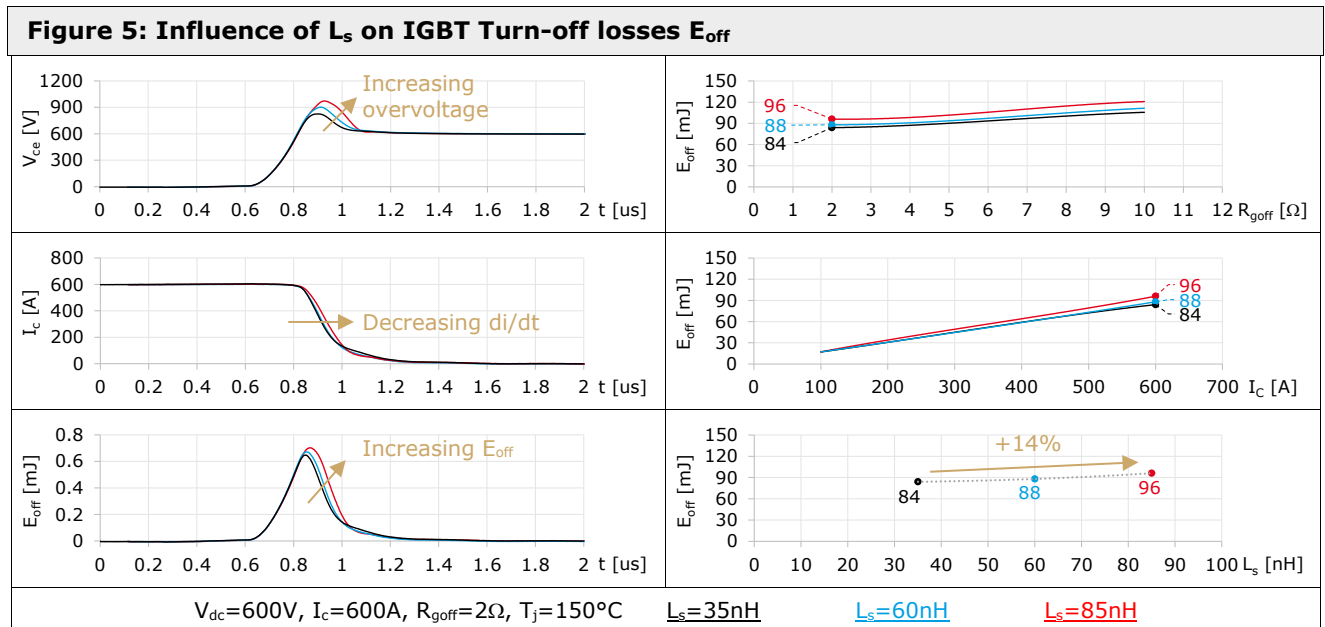
3.2.1 Influence of L_s on IGBT turn-on losses E_{on}

Figure 4 shows the influence of L_s on the IGBT turn-on losses E_{on} . With increasing inductance the voltage drop of the V_{ce} voltage increases. In this case one speaks of inductive voltage drop. Due to the constant DC-Link voltage, the di/dt decreases with increasing inductance, which is visible from the turn-on current I_c . The multiplication of V_{ce} and I_c results in the turn-on losses E_{on} for the three DC-Link inductances. As the turn-on resistance R_{gon} increases, the L_s caused difference in turn-on losses remains almost constant. Only towards low turn-on currents the differences decrease, because the inductive voltage drop disappears more and more. At 600V, 600A, 2Ω, 150°C the turn-on losses decrease by 25% in the range of $L_s=35$ to 85nH.



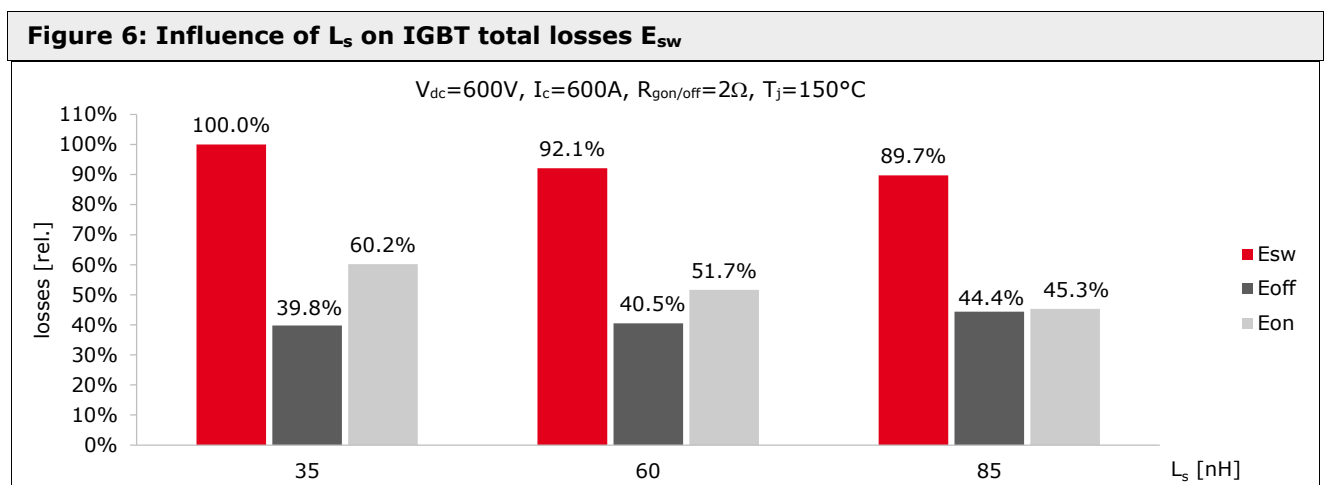
3.2.2 Influence of L_s on IGBT turn-off losses E_{off}

Figure 5 shows the influence of L_s on the IGBT turn-off losses E_{off} . With increasing inductance the overvoltage across the IGBT increases. Due to the increasing overvoltage and the decreasing di/dt , the switching losses increase with increasing DC-Link inductance. With increasing turn-off resistance R_{goff} the difference in turn-off losses remains almost constant. Only towards small turn-off currents do the differences decrease. At 600V, 600A, 2Ω, 150°C the turn-off losses increase by 14% in the range of $L_s=35$ to 85nH.



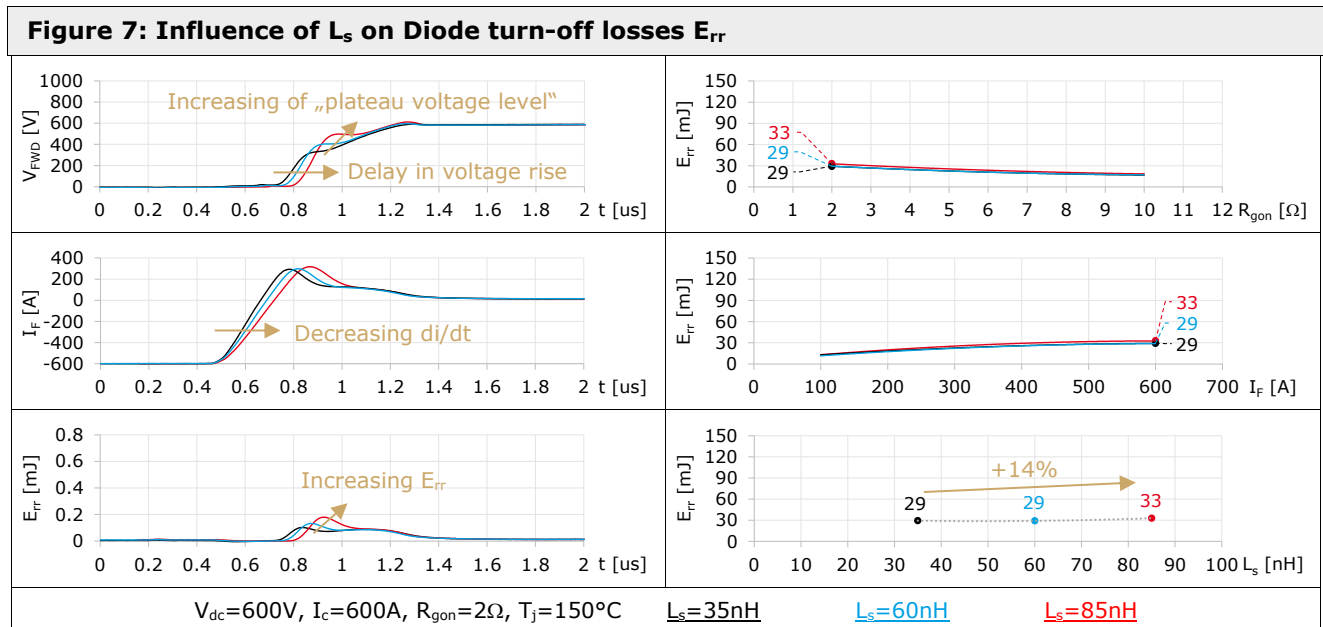
3.2.3 Influence of L_s on IGBT total losses E_{sw}

Figure 6 shows E_{on} , E_{off} and the sum of both E_{sw} as relative values over the DC-Link inductance L_s . The total switching losses E_{sw} refer to the reference value at $L_s=35$ nH. E_{on} , E_{off} refer to the respective total losses E_{sw} at the corresponding DC-Link inductance. At 600V, 600A, 2Ω, 150°C, the total switching losses decrease by about 10% in the range of $L_s=35$ to 85nH.



3.2.4 Influence of L_s on diode turn-off losses E_{rr}

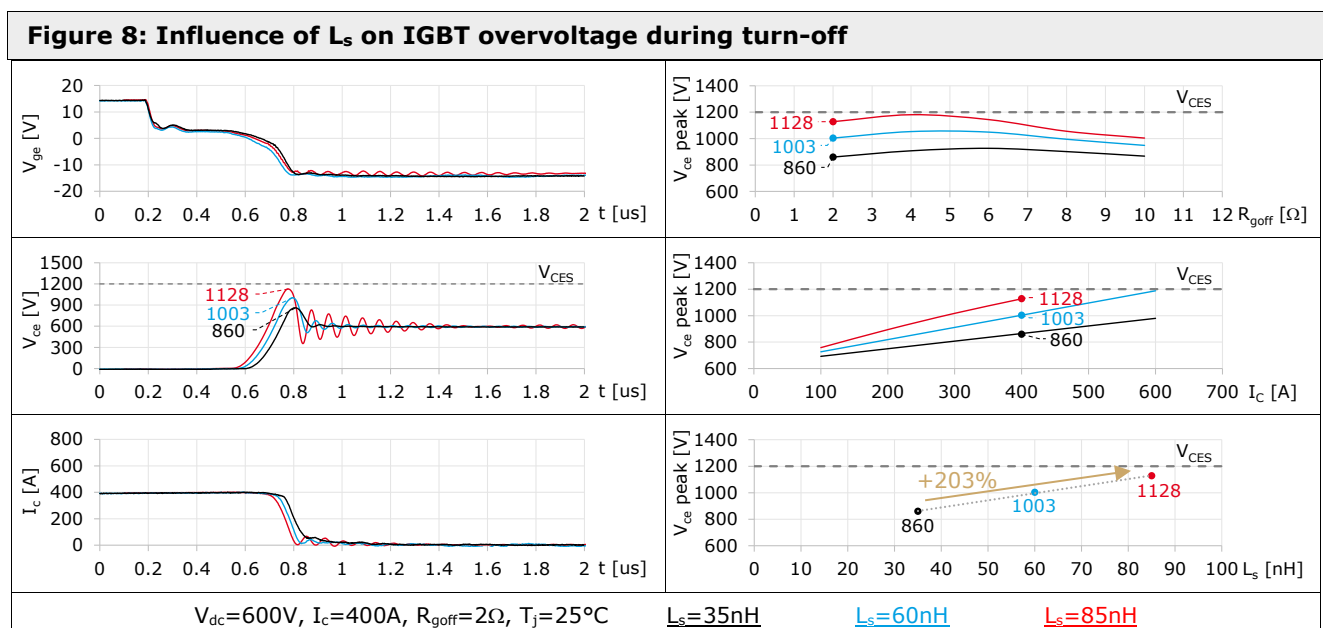
Figure 7 shows the influence of L_s on the diode turn-off losses E_{rr} . With increasing inductance the course of the voltage rise over the diode changes, the di/dt decreases and the losses increase. With increasing turn-on resistance R_{gon} the difference in turn-off losses remains almost constant. Only towards small turn-off currents do the differences decrease. At 600V, 600A, 2Ω , 150°C the turn-off losses increase by 14% in the range of $L_s=35$ to 85nH .



3.3 Influence of L_s on overvoltage

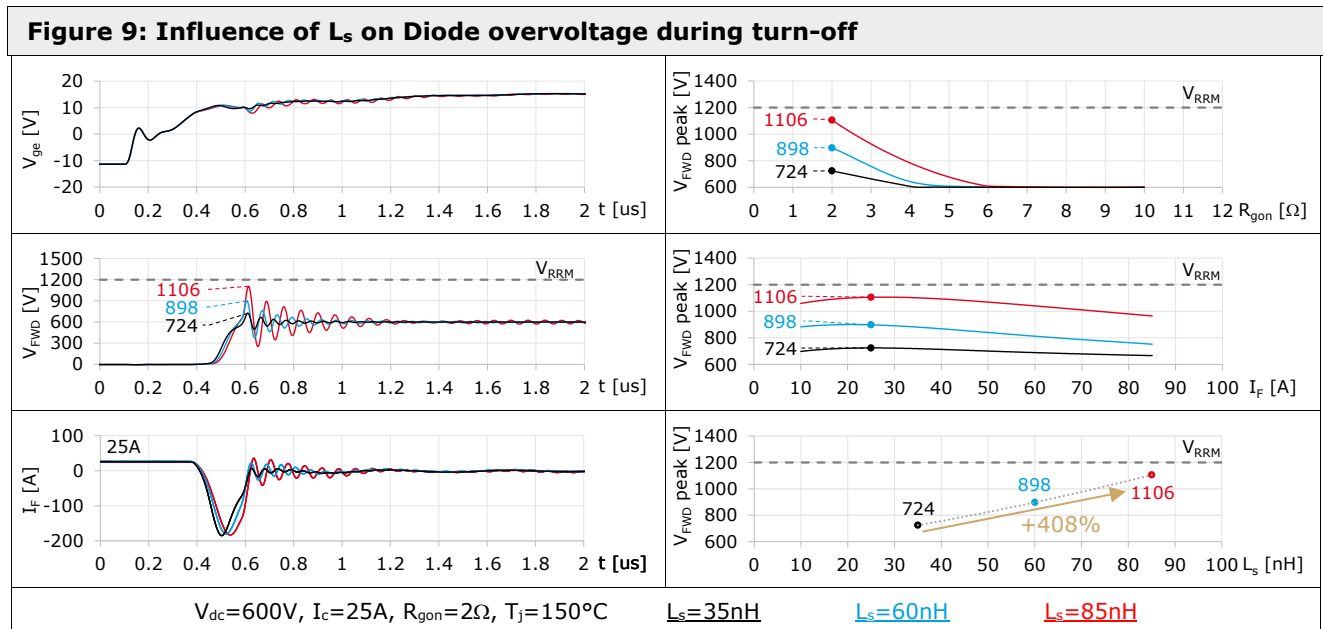
3.3.1 Influence of L_s on IGBT overvoltage during Turn-off

Figure 8 shows the influence of L_s on IGBT overvoltage during turn-off. All curves are synchronized with each other at the gate-emitter voltage V_{ge} . With increasing inductance the overvoltage and the oscillations increase. The oscillations are visible in the V_{ge} , V_{ce} voltage and the switched current. The overvoltage as a function of R_{goff} shows a typical IGBT4 behavior. It first increases with increasing resistance and then decreases again. At 600V, 400A, 2Ω , 25°C the overvoltage related to V_{dc} doubles (528V overvoltage compared to 260V) in the range of $L_s=35$ to 85nH .



3.3.2 Influence of L_s on diode overvoltage during turn-off

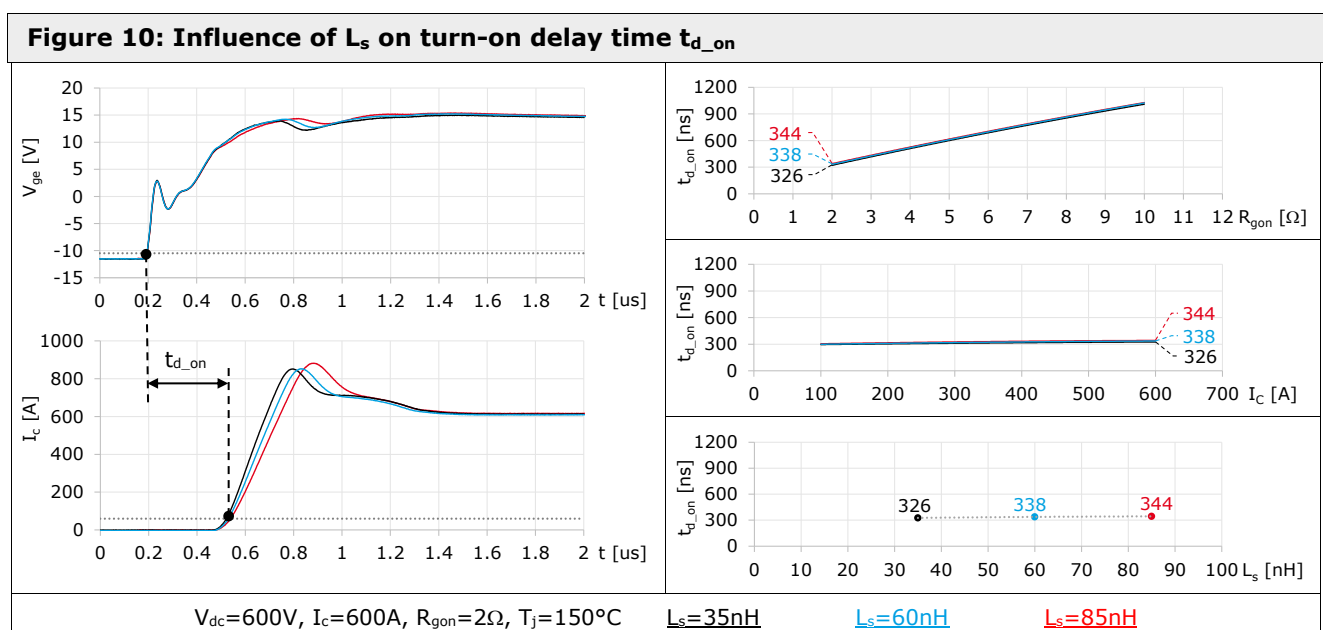
Figure 9 shows the influence of L_s on Diode overvoltage during turn-off. All curves are synchronized with each other at the gate-emitter voltage V_{ge} . With increasing inductance the overvoltage and the oscillations increase. The oscillations are visible in the V_{ge} , V_{ce} voltage and the switched current. The overvoltage as a function of R_{gon} shows that from a gate resistance of 4 or 6 Ω no overvoltage occurs anymore. However, this is accompanied by an increase in the IGBT turn-on losses E_{on} (refer to Figure 4). At 600V, 25A, 2 Ω , 25°C the overvoltage related to V_{dc} quadruples in the range of $L_s=35$ to 85nH.



3.4 Influence of L_s on delay times

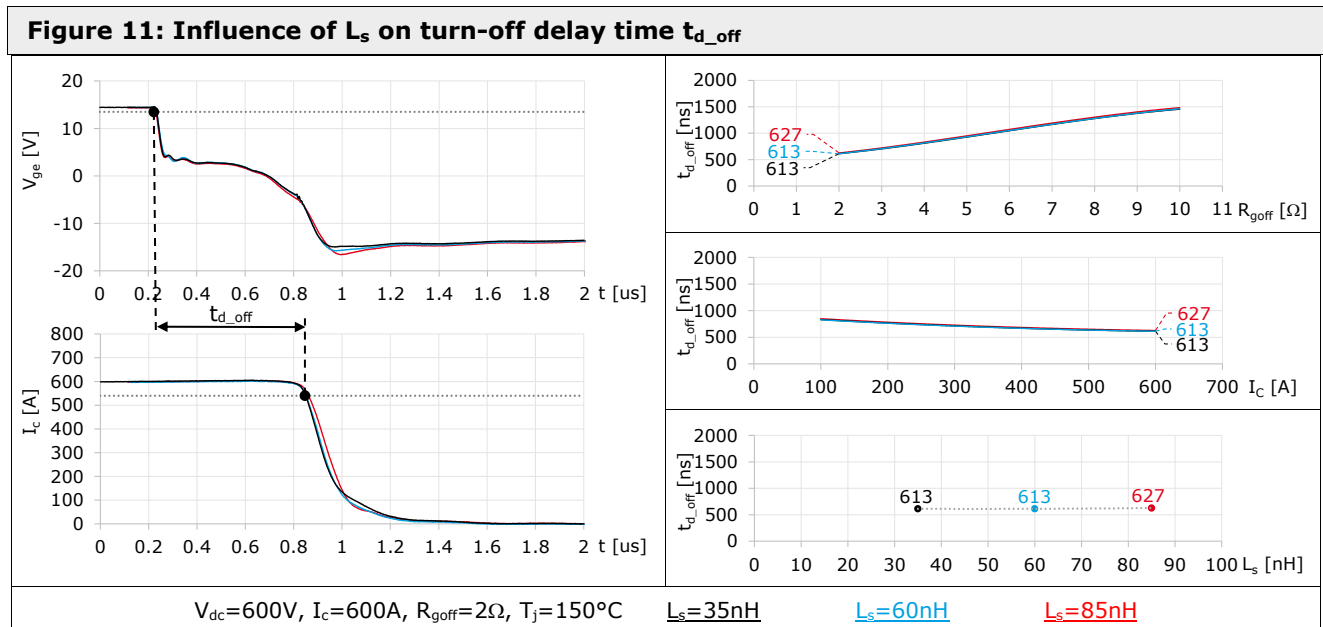
3.4.1 Influence of L_s on turn-on delay time $t_{d_{on}}$

Figure 10 shows the influence of L_s on turn-on delay time $t_{d_{on}}$. All curves are synchronized with each other at the gate-emitter voltage V_{ge} . With increasing inductance the di/dt changes what causes the turn-on delay time only slightly to change. At 600V, 600A, 2 Ω , 150°C the influence on the turn-on delay time can be neglected in the range of $L_s=35$ to 85nH.



3.4.2 Influence of L_s on turn-off delay time t_{d_off}

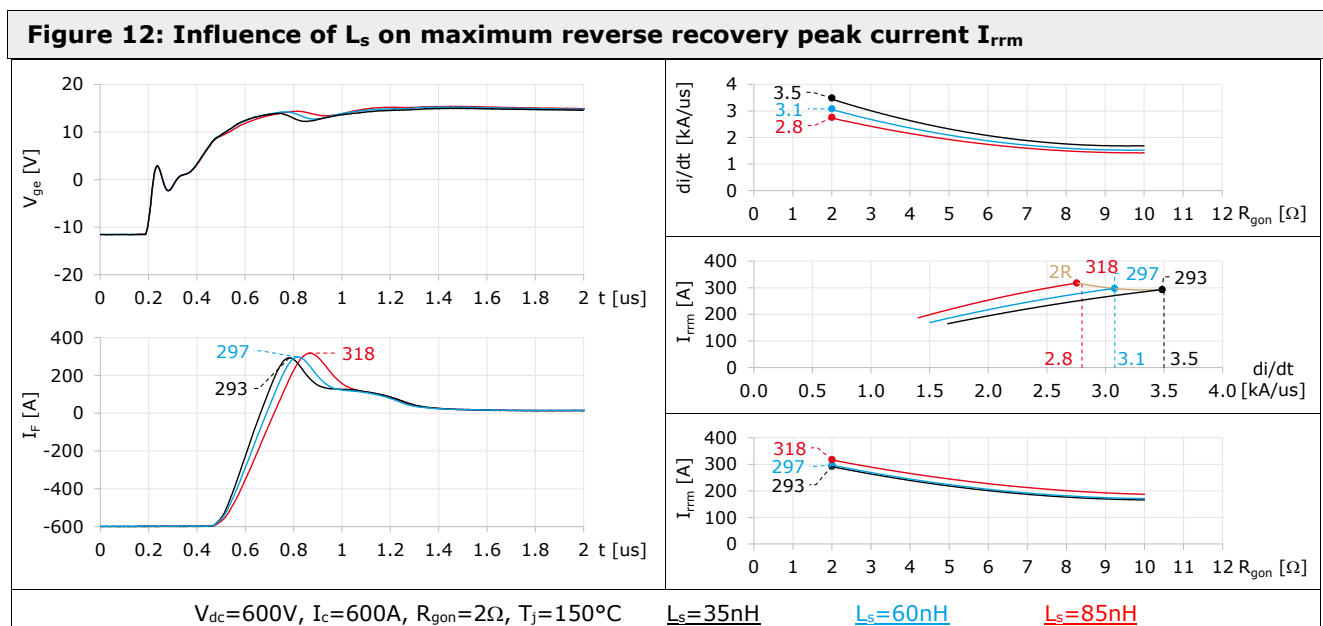
Figure 11 shows the influence of L_s on turn-off delay time t_{d_off} . All curves are synchronized with each other at the gate-emitter voltage V_{ge} . With increasing inductance the di/dt changes what causes the turn-off delay time on slightly to change. At 600V, 600A, 2Ω , 150°C the influence on the turn-on delay time can be neglected in the range of $L_s=35$ to 85nH .



3.5 Influence of L_s on diode reverse recovery behavior

3.5.1 Influence of L_s on maximum reverse recovery peak current I_{rrm}

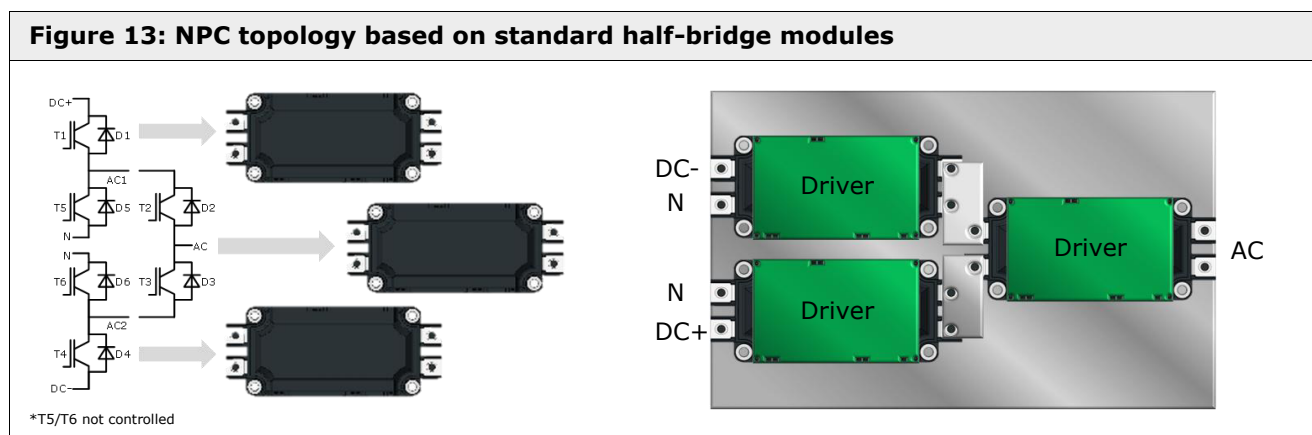
Figure 12 shows the influence of L_s on the maximum reverse recovery peak current I_{rrm} . All curves are synchronized with each other at the gate-emitter voltage V_{ge} . With increasing inductance the I_{rrm} changes only slightly. The differences in I_{rrm} keep constant also at higher R_{gon} .



4. 3-Level Topologies based on Standard Half-Bridge Modules

4.1 NPC topology based on SEMiX3p

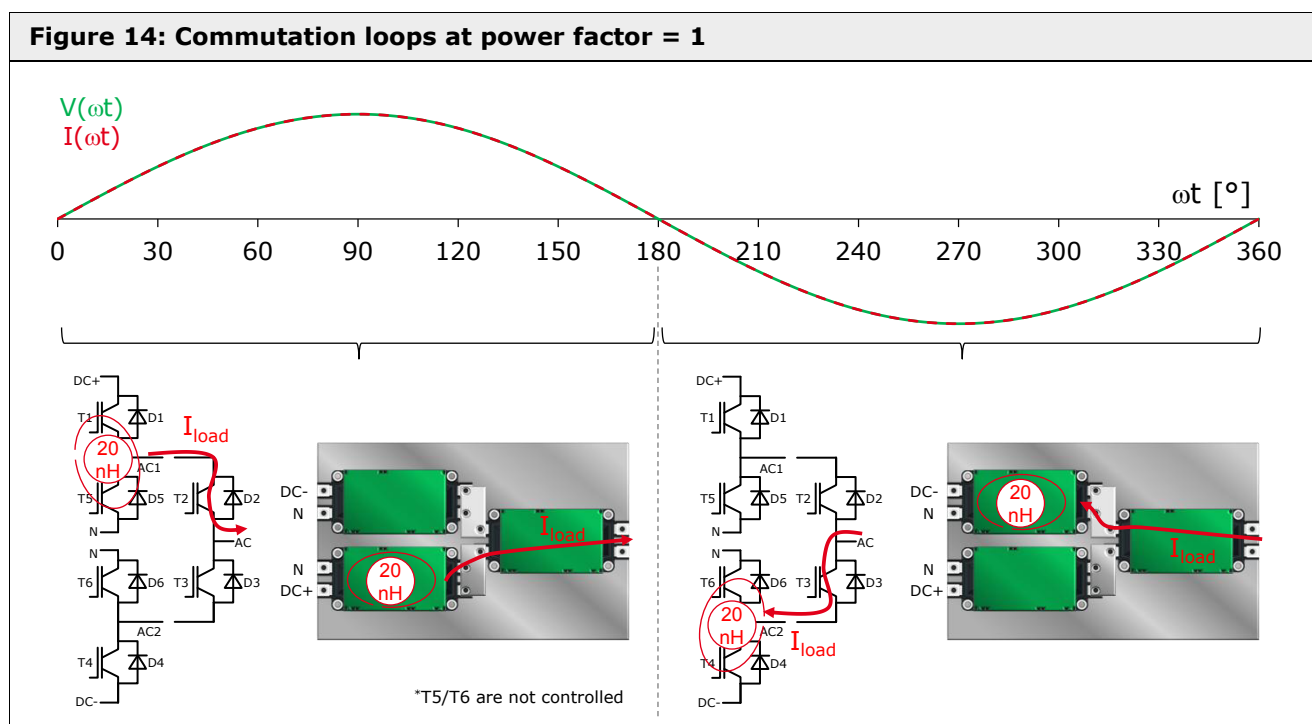
3-level topologies are state of the art and are used in grid tie inverters mainly in wind, solar and UPS applications. In Figure 13 a Neutral Point Clamp (NPC) topology is shown, which is constructed from three standard half-bridge modules. Due to the terminal connections for DC+/DC-/N and AC, the DC-Link cannot be designed in such a way that the potentials overlap completely. This leads to an increased DC-Link inductance, which differs significantly from that specified in the data sheet of the module.



4.2 Commutation loops

4.2.1 Commutation loops at power factor = 1

The commutation loops over an output period are shown for the power factor = 1 in Figure 14. The phase angle between the idealized output voltage and current is 0° . For positive and negative output current, fast commutation takes place exclusively within a half-bridge module. The commutation inductance is of the same order of magnitude as that specified in the module data sheet. From the point of view of overvoltage limitation, the voltage zero crossing must be considered here when fast commutation changes from DC+/N to N/DC- or vice versa. In this commutation case all three modules are involved. Due to the single switching event within an output period, the gate resistances for T2/T3 can be chosen large, however, so that the switching losses can be neglected.



4.2.2 Commutation loops at power factor = -1

The commutation loops over an output period are shown for the power factor = -1 in Figure 15. The phase angle between the idealized output voltage and current is 180°. For positive and negative output current, all three half-bridge modules are always involved in the fast commutation. The commutation inductance is much higher than the values given in the data sheet and can reach values of 100nH or even more.

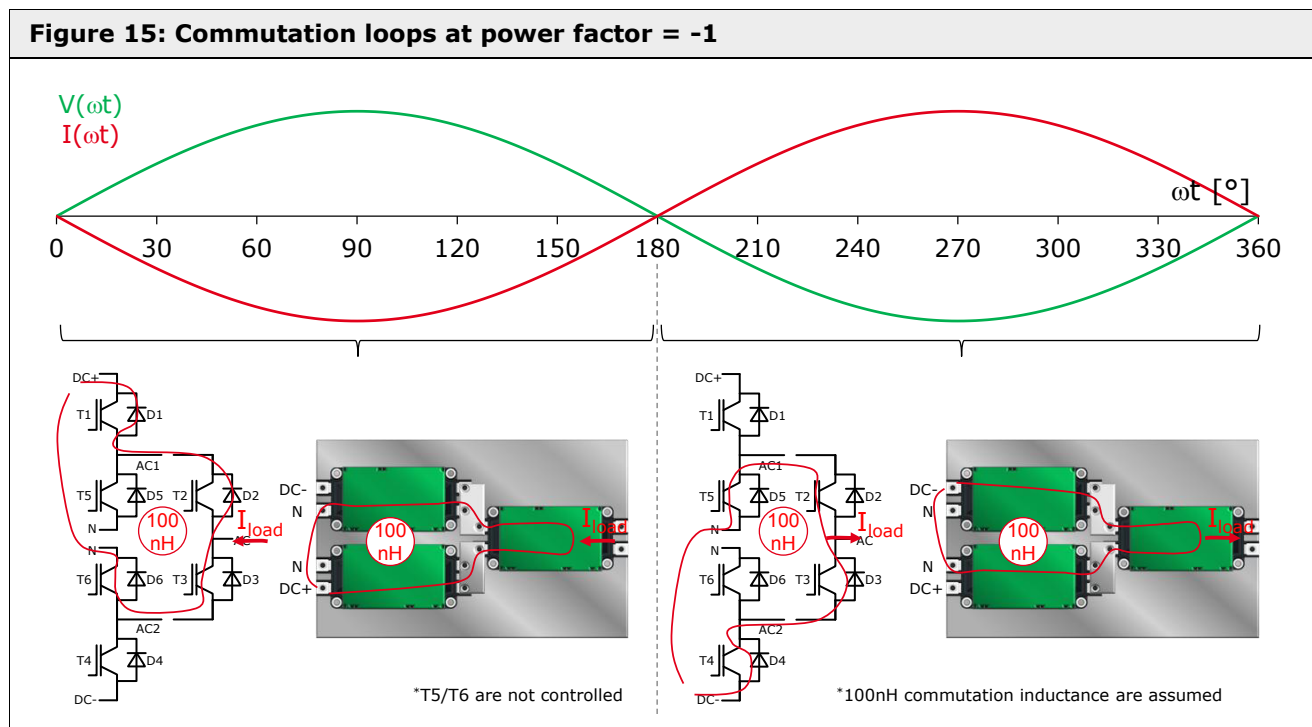


Figure 16 shows the overvoltage curves to be expected when switching off the IGBT T2/T3 and the diodes D1/4 as a function of the commutation inductance (see Figure 8/Figure 9). For the IGBT, the overvoltage increases with falling temperature and rising turn-off currents. In this example, an overvoltage of 1128V at 400A/ $L_s=85\text{nH}$ occurs at the IGBT. For the diode, low currents and high temperatures are critical. Here an overvoltage of 1106V at 25A/ $L_s=85\text{nH}$ occurs. In both cases the maximum overvoltage of approx. 70V or 90V is only slightly below the maximum permissible blocking voltage of 1200V.

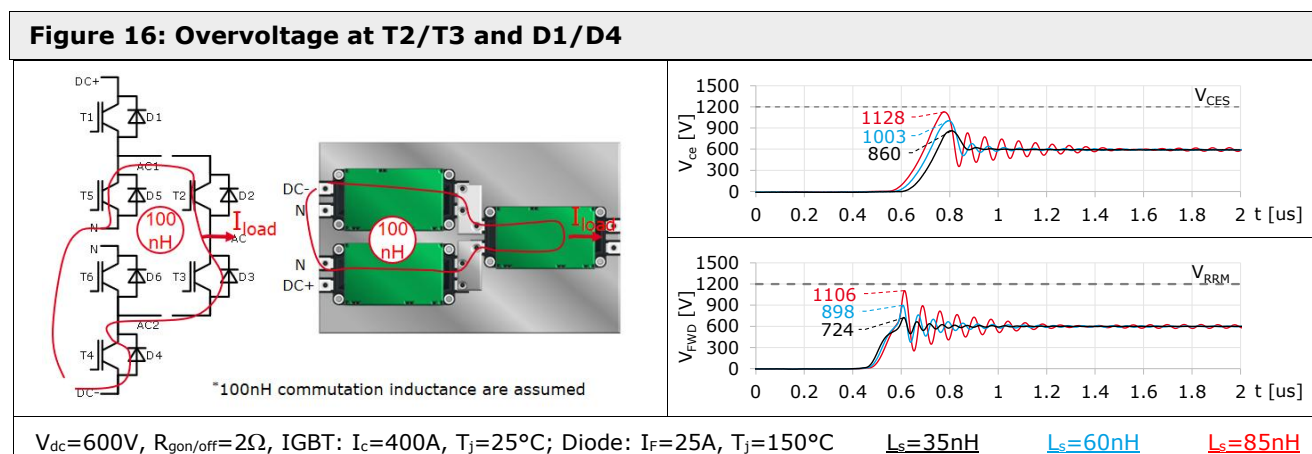
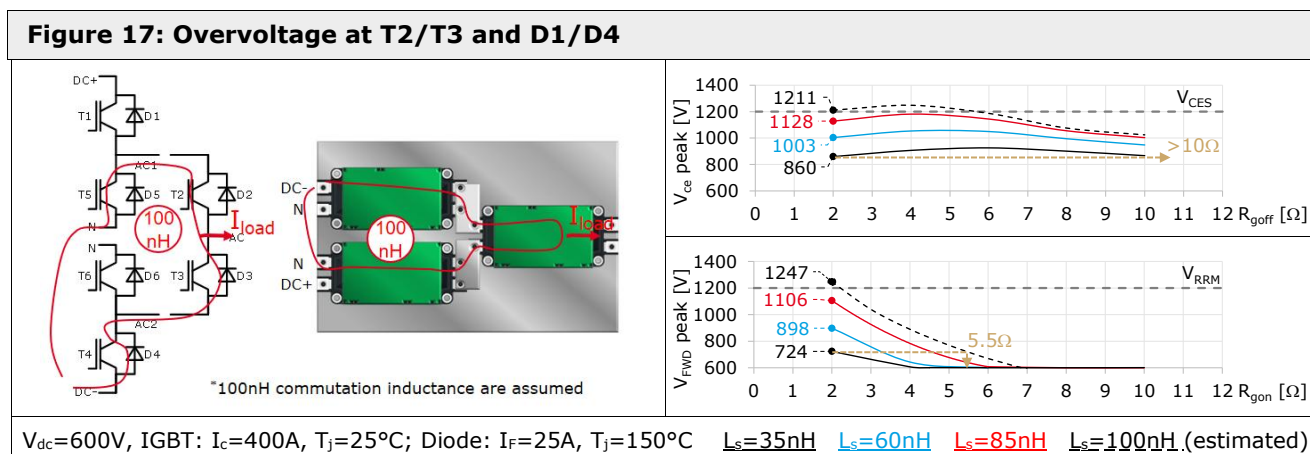


Figure 17 shows the overvoltage characteristics of the IGBT and diode as a function of the gate resistance. The characteristic of $L_s=100\text{nH}$ is estimated and symbolized by a dotted line. Corresponding to the maximum turn-off current, the R_{goff} must be increased for a given DC-Link design to remain below the maximum blocking voltage. In this example, the IGBT overvoltage exceeds the maximum blocking voltage of 1200V at an inductance of 100nH. To achieve the same 860V overvoltage at $L_s=100\text{nH}$ as at 35nH would require to increase R_{goff} from 2Ω to well more than 10Ω, if it is achieved at all. With increasing R_{goff} the losses increase (see Figure 5).

It can be seen from Figure 9 that the maximum overvoltage of the diode occurs at approx. 25A, which is in the range of 5% of the nominal chip current. This current value always occurs near the current zero crossing regardless of the maximum output power. To generate the same overvoltage at the diode at $L_s=100\text{nH}$ as at 35nH , the R_{gon} would have to be increased from 2 to 5.5Ω . Referring to Figure 4, the turn-on losses are almost doubled if the R_{gon} is increased from 2 to 5.5Ω .



5. Summary

In this Application Note, the influence of the DC-Link inductance on the switching behavior and the power losses was examined. It was shown that with increasing DC-Link inductance L_s , the IGBT turn-on losses decrease, whereas IGBT and diode turn-off losses increase. E_{on} in particular is reduced more than E_{off} and E_{rr} increase. This is the reason why L_s is given in the data sheet, otherwise the losses can be assumed too optimistically.

Furthermore, the overvoltage and the tendency to oscillate increase with increasing inductance for both the IGBT and the diode. This makes it necessary to increase the gate resistance with increasing stray inductance, which leads to higher losses.

The influence on the turn-on and turn-off delay time can be neglected.

Even though increased DC-Link inductance results in reduced E_{on} , a low-inductance DC-Link design should still be aimed for, since low overvoltage peaks are essential for reliable operation. In addition, a low-inductance DC-Link design is necessary in order to turn-off high output currents even in the event of a short circuit and to limit the overvoltage and oscillations on the IGBT and the diode during turn-off (EMI).

In the case of 3-level NPC topologies based on standard half-bridge modules, other gate resistances than those specified in the data sheet must be used, as in this case the commutation inductance can be much higher than that specified in the data sheet.

Furthermore, when comparing power dissipation in different data sheets, it is important to note at which inductance they were measured.

Figure 1: Definition of L_s	2
Figure 2: Device Under Test and Test setup	2
Figure 3: Investigated quantities that depend on DC-Link inductance L_s	3
Figure 4: Influence of L_s on IGBT turn-on losses E_{on}	3
Figure 5: Influence of L_s on IGBT Turn-off losses E_{off}	4
Figure 6: Influence of L_s on IGBT total losses E_{sw}	4
Figure 7: Influence of L_s on Diode turn-off losses E_{rr}	5
Figure 8: Influence of L_s on IGBT overvoltage during turn-off	5
Figure 9: Influence of L_s on Diode overvoltage during turn-off	6
Figure 10: Influence of L_s on turn-on delay time $t_{\text{d, on}}$	6
Figure 11: Influence of L_s on turn-off delay time $t_{\text{d, off}}$	7
Figure 12: Influence of L_s on maximum reverse recovery peak current I_{rrm}	7
Figure 13: NPC topology based on standard half-bridge modules	8
Figure 14: Commutation loops at power factor = 1	8
Figure 15: Commutation loops at power factor = -1	9
Figure 16: Overvoltage at T2/T3 and D1/D4.....	9
Figure 17: Overvoltage at T2/T3 and D1/D4.....	10

Es konnten keine Einträge für ein Abbildungsverzeichnis gefunden werden. **Symbols and Terms**

Letter Symbol	Term
AC	Output terminal
DC+	Positive potential (terminal) of a direct voltage source
DC-	Negative potential (terminal) of a direct voltage source
di/dt	change of current per time
DUT	Device Under Test
dv/dt	change of voltage per time
E_{off}	Energy dissipation during IGBT turn-off time
E_{on}	Energy dissipation during IGBT turn-on time
E_{rr}	Energy dissipation during reverse recovery (diode)
E_{sw}	Energy dissipation during IGBT turn-off and turn-on time
I_c	Continuous collector current
I_F	Diode forward current
IGBT	Insulated Gate Bipolar Transistor
I_{nom}	Nominal current
I_{rrm}	Peak reverse recovery current
L_{CE}	Parasitic collector-emitter inductance
L_s	DC-Link stray inductance
N	Neutral potential (terminal) of a direct voltage source; midpoint between DC+ and DC
R_{gon}	Gate turn-on resistor
R_{goff}	Gate turn-off resistor
t	Time
t_{d_off}	Turn-off delay time
t_{d_on}	Turn-on delay time
t_f	Fall time
t_r	Rise time
V_{ce}	Collector-emitter voltage
V_{ces}	Collector-emitter voltage with gate-emitter short circuited
V_{dc}	Total supply voltage (DC+ to DC-)
V_{FWD}	Voltage across free-wheeling diode
V_{ge}	Gate-Emitter voltage
V_{RRM}	Repetitive peak reverse voltage (Diode)
T_j	Junction temperature
ωt	Conduction angle

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors" [3].

References

- [1] www.semikron-danfoss.com
- [2] SEMiX603GB12E4p, data sheet, Rev. 2.0 – 25.01.2017
- [3] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, "Application Manual Power Semiconductors", 2nd edition, ISLE Verlag 2015, ISBN 978-3-938843-83-3

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