Application Note
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SEMIKRON DANFOSS

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Power Cycle Model for IGBT Product Lines

1. Introduction

Semikron Danfoss introduces with this Application Note new power cycle (PC) figures for power semiconductor modules with wire bonded chips. The failure modes covered by this Application Note are chip solder fatigue, bond wire heel crack or lift-off and in combination of later also degradation of top side metallization. The presented curves do not cover active and passive temperature cycling which rather stresses and degrades the baseplate soldering. The revision 02 introduces an additional thickness factor for rectifier devices only.

1.1 Failure modes in Power Cycling

Power cycling failure is an End of Life (EOL) failure. Power cycling happens, when a semiconductor chip inside a package is loaded by current and is heated up by the losses caused by the current flow. During the heating phase a temperature gradient arises inside the package. After switching off the current the chip cools down and the temperature gradient disappears. The up and down in combination with different CTE's of the used materials stresses the interconnection between the materials and leads to a wear out of the semiconductor package. Which failure mode (chip solder or bond wire) is triggered first depends on the temperature gradient and the duration of the cycle. More details about the failure mechanisms can be found for example in [2].

1.2 Test procedure, failure criteria and statistic

The tests to trigger these failures are Fast Power Cycling (also referred as PC_{sec}) with t_{on} in the low second range and Slow Power Cycling (also referred as PC_{min}) with t_{on} >15s up to minutes. Typically, these tests are DC tests where a constant current is applied to the device under test (DUT) for a certain time t_{on} and the conduction losses heat up the device. In addition to this Semikron Danfoss has carried out inverter tests, where conduction and switching losses are used to heat up the semiconductors in short times.

The test strategy for Semikron Danfoss products is chosen to be as close as possible to real application conditions. That means the temperature swing is initially set by time t_{on} and load current I_L and then these parameters are kept constant during the whole test independent from the evolution of the temperature swing. Ageing of the DUT like "solder fatigue → higher R_{th} → higher ΔT_j" or alternative "bond wire lift-off → higher forward voltage → higher losses → higher ΔT_j" increases the stress and accelerates the ageing effect. The reason to keep the load parameters constant is that in real applications, no reduction in performance is applied to keep the temperature swing constant. In [5] it was shown that this strategy is most stressful for the DUT. The failure criteria to reach EOL is an increase either of the forward voltage (V_f, V_{CE} or V_{DS}) by 20%, of the R_{th} by 20% or of the temperature swing ΔT by 20%, each compared to its initial value. Weibull statistics is applied to test results to calculate a failure probability. The PC figures shown in this paper represent a 15% failure probability.

1.3 History of PC lifetime modelling

The most popular model in the past from the late 90s was published by the LESIT [3] study and introduced a dependency of the cycle number from the medium junction temperature $T_{jm} = \frac{T_{j(max)}+T_{j(min)}}{2}$ additional to the junction temperature swing. The curves in the application manual [2] have been derived from this model by an adapted technology factor A. In 2008 a model was published at the CIPS conference [4], which considered additional parameters like current density, pulse duration, voltage class (related to chip thickness) and bond wire diameter.
At the PCIM conference in 2013 [6] and ESREF conference 2017 [7] results of a test series have been published which allowed to separate failure modes for solder fatigue and bond wire lift-off/heel crack. This is important for the improvement of power modules and is the base for the SKiM63-Model used for backside Ag-sintered chips and front side contact with Al bond wire. Furthermore, the model provides a function of time dependency for a much wider range of on-times used here as well.

1.4 Base for PC lifetime models

The PC lifetime models provided in the following text combine the investigation results published by researchers of Semikron Danfoss and other affiliations with the extensive data base generated by Semikron Danfoss during product qualifications and lifetime model validations. This data base comprises:

- About 1000 DUT stressed in power cycles tests over the last years are considered
- More than 60% of these are tested until EOL. The other 40% of DUT did not fail during the test time but had to be stopped due to failing of one of the 60% group in the setup
- Test of modules with and without baseplate
- Voltage classes from 600V to 1700V
- IGBT, CAL Diode, Rectifier and SiC devices like MOSFETs or Schottky diodes
- Chip thickness from 70µm to 310µm
- t_{on} times from 0.07s to 60s in DC-test and 0.04s to 0.5s in Inverter test (AC with switching losses)
- ΔT_j from 50K to 120K (DC-Test) and 30K to 63K (Inverter test)
- Medium temperature between T_{jm} = 333K … 400K (32°C … 127°C)

1.5 Validity

The models presented here are valid for Semikron Danfoss Product Lines used mainly for transistors (IGBT, MOSFET) and in some cases also for rectifiers but all with Al bond wire connection on the front side and solder or Ag sinter connection on the backside of the chips. Power cycle curves previously published are herewith obsolete, especially the curves presented in the application manual [2]. The curves in the 2nd edition (2015) represented the state of knowledge in the early 2000er. In the meanwhile, a lot of investigations and publications provide a much better understanding of influencing parameters and interaction of different operating conditions.

2. Power Cycling Lifetime Models

2.1 Lifetime Model Equations

The model equations use terms of long time established power cycle models like Arrhenius Term and Coffin-Manson Law [3] as well as the time dependency and the chip thickness [6] [7]. The formula is extended by two terms with an exponent β which results in an additional increase of N_f at low ΔTj [10].

$$N_f = A_0 \cdot A_1{}^{\beta} \cdot \Delta T_j{}^{-\beta} \cdot \Delta T_j{}^{\alpha} \cdot e^{\left(\frac{E_a}{k_B \cdot T_{jm}}\right)} \cdot \frac{C + t_{on}{}^{\gamma}}{C + 2^{\gamma}} \cdot k_{thickness}$$

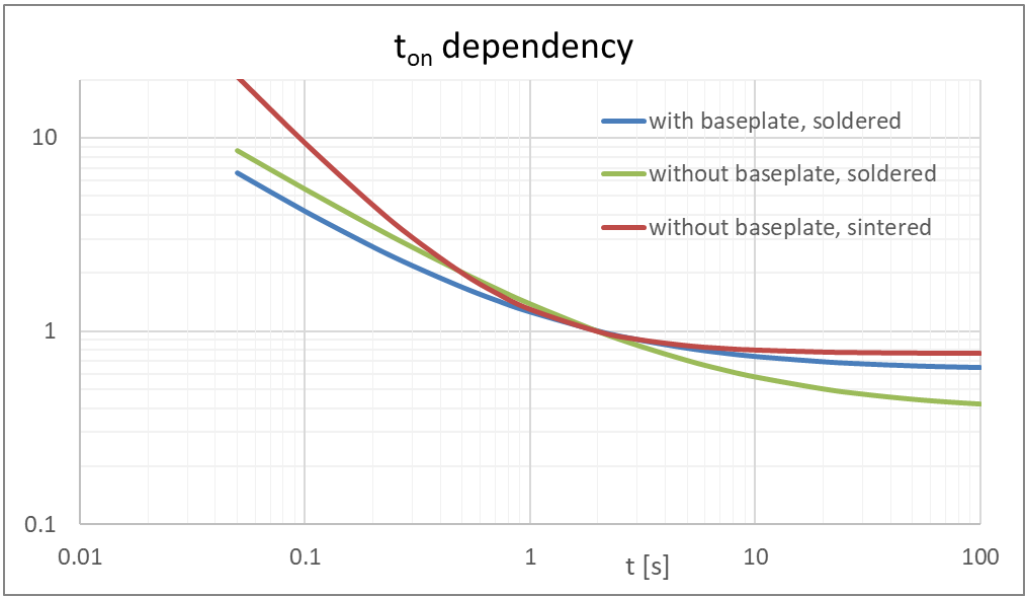
$$\text{with} \quad \beta = e^{\left(\frac{-\left(\Delta T_j - T_0\right)}{\lambda}\right)}$$

The model equation can be used for all types of Semikron Danfoss power modules with slightly adapted set of parameters.

2.2 Time dependency t_{on}

The term in the model equation related to t_{on} in seconds was introduced in the SKiM63 lifetime model [6] for sintered and wire bonded power modules. It has been adapted to the test results here for other assembly technologies using the parameter C and γ. It is a time dependent scaling factor, normalized to a pulse duration (heating time) of t_{on}=2s. For modules with copper baseplate a different dependency was found compared to modules without baseplate, even though the front and back side chip contacts are the same. A reason might be the different temperature gradient inside the module in Y and X direction as well as a different micro-mechanical bending behavior depending on the construction of the power module (with or without baseplate). Furthermore, in modules without baseplate smaller chips are used while in baseplate modules typically larger chips are built-in.
Nevertheless, higher numbers of cycles are achievable in all cases for short cycles, while for longer durations the power cycling capability is lower. The function approaches a minimum value for times 30…60s and in [8] it is mentioned that for time < 40ms no further increase of cycle numbers can be expected.
Fatigue of the baseplate solder is an additional failure mode for modules with baseplate. This ageing process is not the relevant failure mode in the tests considered here for the PC models, but can lead to a lower number of cycles, especially with long cycle durations (blue curve in Figure 1).

Figure 1: Time dependency of power cycle numbers for modules with and without baseplate

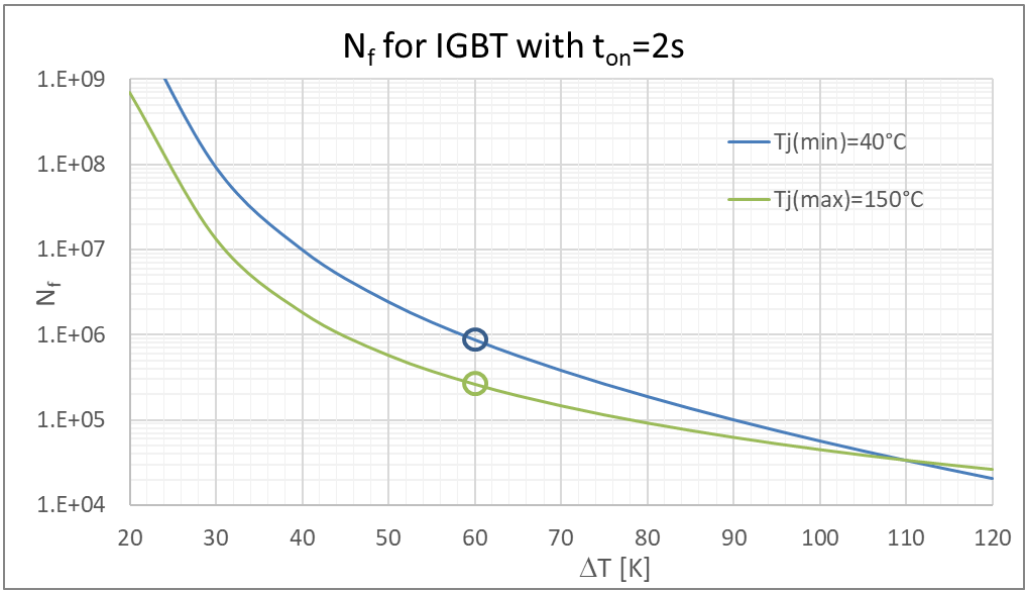


2.3 Dependency from medium temperature T_{jm}

The medium temperature is defined as $T_{jm} = \frac{T_{j(max)} + T_{j(min)}}{2}$ and is used as an absolute value in Kelvin. It is not the average temperature over time. The influence of the medium temperature is much lower as it was

predicted for example in [3] and used in [2]. This can lead to the situation that the old models predict much higher cycle numbers than today's models, especially at low temperature levels.
For example, if an IGBT is stressed by a temperature swing of ΔTj=60K in the application, it can withstand about 880k cycles at a lower turning point of $T_{j(min)}$=40°C (40°C↔100°C). On the other hand the expected number of cycles is only about 260k at the same ΔT=60K but at an upper turning point of $T_{j(max)}$=150°C (90°C↔150°C) (see Figure 2).

Figure 2: Power cycle number in dependency of medium temperature for soldered chips



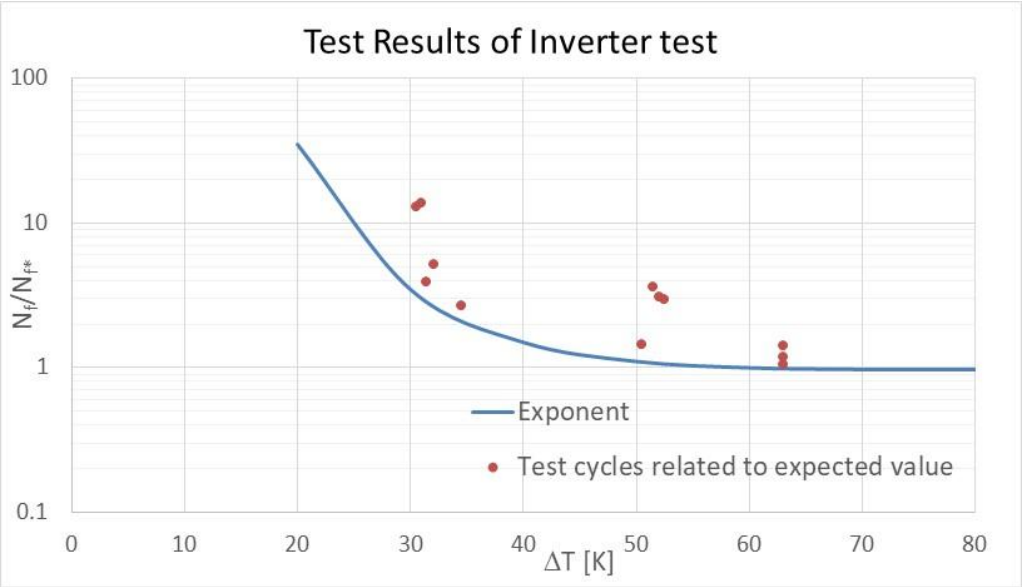
2.4 Low ΔT_j behaviour described by exponent β

In several papers and studies the topic "What happens at low ΔT_j?" has been investigated [8]. Depending on the test conditions and the triggered failure mode (solder fatigue) an increase of N_f was reported. Furthermore there appears to be a discrepancy between the predicted numbers of formerly used PC models and the field experience of inverter operating for years at low frequencies and low ΔT_j for example at ΔT_j=30K. These considerations lead to the theory for a stronger increase of the cycle numbers towards low ΔT_j.
One problem is, that the models are derived from accelerated tests at ΔT_j=70K and ΔT_j=110K where plastic deformation dominates. They are applied to the low ΔT_j in the real applications where more and more elastic deformation takes place [9]. Test under conditions like in the application are not possible for product qualification as they would need years of testing time.
To provide evidence for this theory inverter tests have been performed with a back-to-back inverter to stress the IGBT on the inverter side and the diodes on the rectifier side. The current amplitude of the sine wave function was set to 80% nominal current and with additional switching losses the desired ΔT_j was achieved within sufficiently short times. The inverter output frequency was modulated between 2Hz and 10.5Hz to set the exact ΔT_j. The overall test duration was 1.5 years.
The test results in Figure 3 are set in relation to an expected value N_{f*} without low ΔT_j effect. N_{f*} was calculated with the power cycle model from chapter 2.1 without the low ΔT_j extension ($A_1{}^{\beta} \cdot \Delta T_j{}^{-\beta}$) but with the thickness factor and the time dependency:

$$N_{f*} = A_0 \cdot \Delta T_j{}^{\alpha} \cdot e^{\left(\frac{E_a}{k_B \cdot T_{jm}}\right)} \cdot \frac{C + t_{on}{}^{\gamma}}{C + 2^{\gamma}} \cdot k_{thickness}$$

A clear increase towards low ΔT_j can be seen (factor >1). The parameters A_1, T_0 and λ used in combination with the exponent β were derived from the blue curve in Figure 3.
The root cause of failure in the inverter test was solder fatigue beginning at the chip center. In [7] was shown that the effect is related to the short cycle times. This is in contrast to high ΔT_j DC tests in which the solder fatigue starts in the corners and the edges of the chips. When the devices failed, the bond wire contact was still there, but was already seriously damaged.

Figure 3: Inverter test results of IGBT and Diodes at low ΔT related to the expected value



2.5 Chip thickness $k_{thickness}$

An influence of the chip thickness was observed too as it was indirectly introduced by the voltage class in [4] (IGBT of higher voltage class are thicker than low voltage IGBT). Thicker chips are stiffer and generate higher stress on the interconnections and fail earlier.
The thickness of the different chip generations and from different suppliers are not known to the user of the power modules. Furthermore, there was only a very small dependency between 650V and 1200V IGBT observed, much smaller than the standard deviation considering the total number of test results under one test condition. Therefore, the thickness is clustered here to make the model more user friendly. It is implemented into the model by constant factors. For SiC devices the factor represents not only the thickness which contributes to the stiffness but also different material properties like Young's modulus (modulus of elasticity) which is about factor 3 higher for SiC compared to Si.

- Factor = 1 is used for IGBT with a blocking voltage <=1200V
- Factor = 0.65 for 1700V IGBT, CAL diodes
- Factor = 0.5 is used for rectifier (thyristor, mains diodes) inside IGBT module housings
- Factor = 0.33 is used for SiC devices with a blocking voltage <=1200V

2.6 Chip size and rate of module area utilization

The power cycle capability is not heavily influenced by the area of the single chip. That means a large 150A chip can achieve the same number of cycles at a given ΔT_j as a small 25A chip. The same applies for the utilization of the internal available module area. A module completely equipped with silicon chips achieves nearly the same number of cycles as the same type of module only partially equipped (see the results in [11]). Therefore, it is feasible to apply the same formula for a whole product family and it is not necessary to distinguish between modules with lower and higher nominal currents.

3. Power Cycle Figures

Three partially different sets of parameters are used for the different types of assembly technologies.

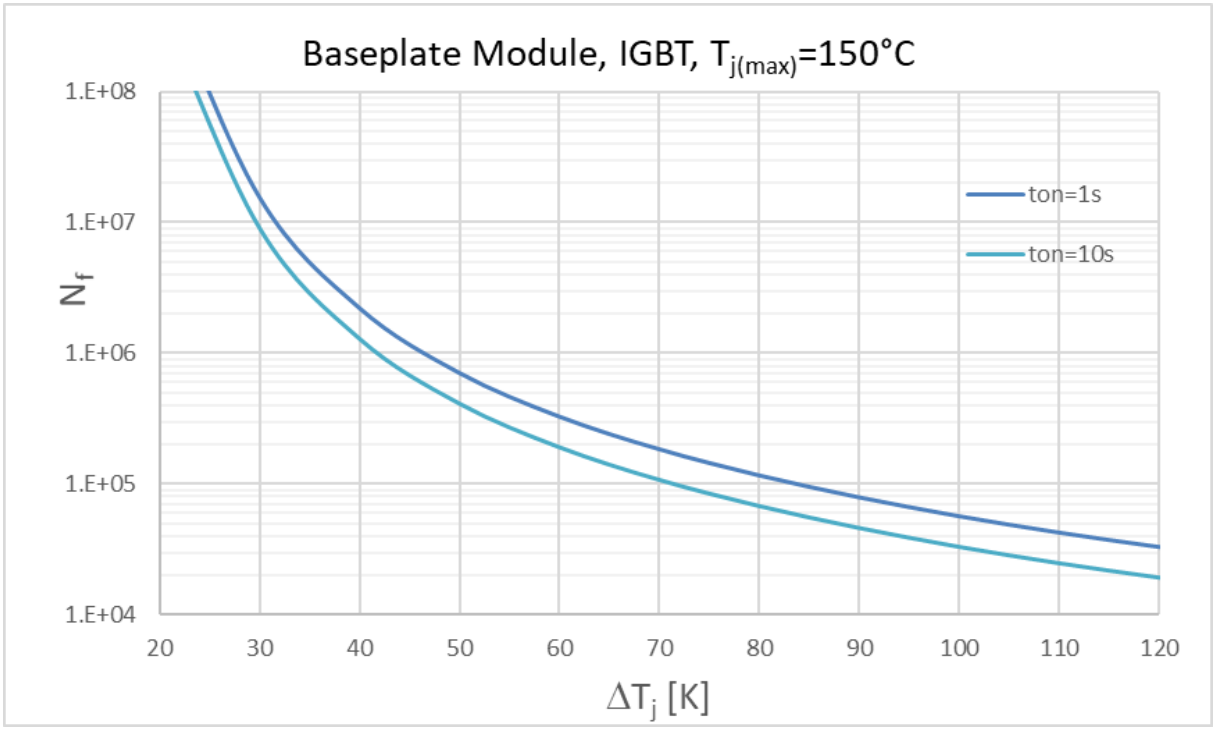
3.1 Modules with copper baseplate, soldered chips and aluminum bond wires

The model is valid for the product families SEMITRANS and SEMiX

Table 1: Parameter for power cycle model "Baseplate Modules"

Parameter	Value	Explanation
A_0	2.9E+09	Technology Coefficient
A_1	60	Factor of Low ΔT Extension
T_0 [K]	40	Initial Temperature for Low ΔT Extension
λ [K]	17	Drop Constant of Low ΔT Extension
α	-4.3	Coffin-Manson Exponent
E_a [J]	4.50E-20	Activation Energy
k_B [J/K]	1.38E-23	Boltzmann Constant
C	1	Time Coefficient
γ	-0.75	Time Exponent
$k_{thickness}$	1 | 0.65| 0.5 | 0.33	Chip Thickness Factor (see 2.5)

Figure 4: N_f for IGBT in modules with baseplate with t_{on}=1s, t_{on}=10s and $T_{j(max)}$=150°C



$$N_f = A_0 \cdot A_1^{e^{\left(\frac{-(\Delta T_j - T_0)}{\lambda}\right)}} \cdot \Delta T_j^{\alpha - e^{\left(\frac{-(\Delta T_j - T_0)}{\lambda}\right)}} \cdot e^{\left(\frac{E_a}{k_B \cdot T_{jm}}\right)} \cdot \frac{C + t_{on}^{\gamma}}{C + 2^{\gamma}} \cdot k_{thickness}$$

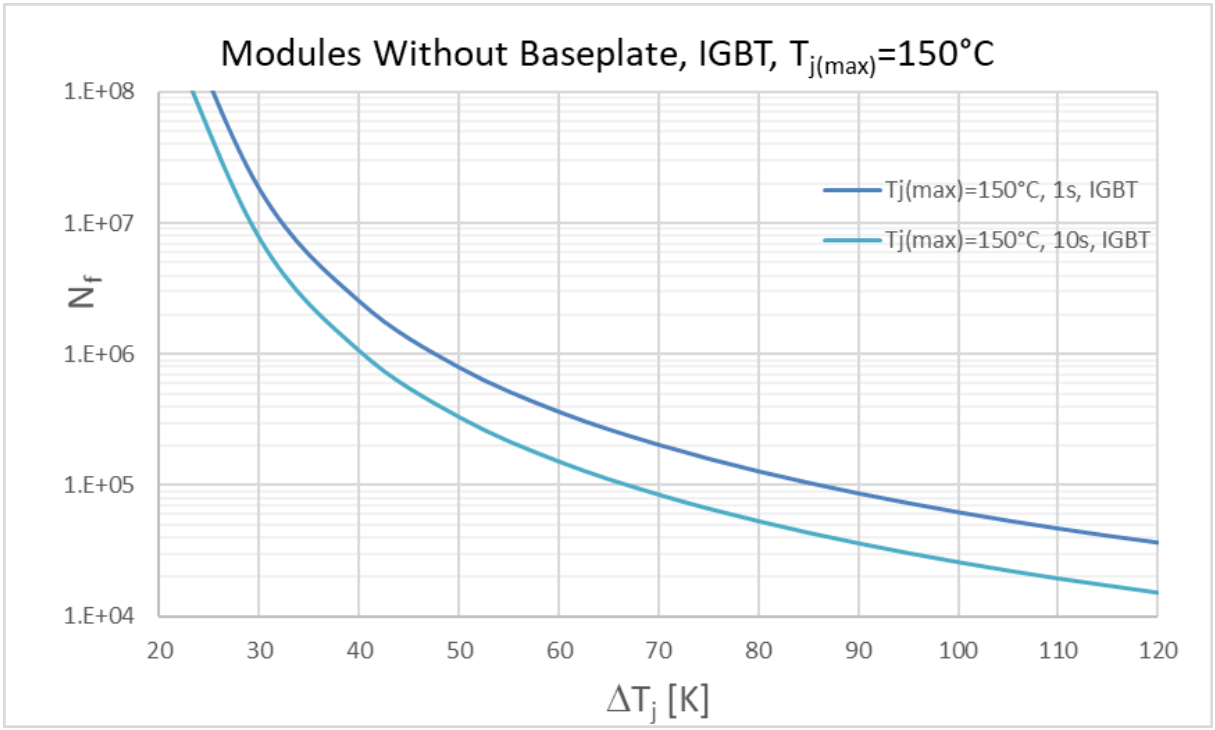
3.2 Modules without baseplate, soldered chips and aluminum bond wires

The model is valid for the product families MiniSKiiP, SEMITOP, SKiiP3, SKiM4/5

Table 2: Parameter for power cycle model "Modules without Baseplate"

Parameter	Value	Explanation
A_0	2.90E+09	Technology Coefficient
A_1	60	Factor of Low ΔT Extension
T_0 [K]	40	Initial Temperature for Low ΔT Extension
λ [K]	17	Drop Constant of Low ΔT Extension
α	-4.3	Coffin-Manson Exponent
E_a [J]	4.50E-20	Activation Energy
k_B [J/K]	1.38E-23	Boltzmann Constant
C	0.38	Time Coefficient
γ	-0.7	Time Exponent
$k_{thickness}$	1 | 0.65| 0.5 | 0.33	Chip Thickness Factor (see 2.5)

Figure 5: N_f for IGBT in modules without baseplate with t_{on}=1s, t_{on}=10s and $T_{j(max)}$=150°C



$$N_f = A_0 \cdot A_1^{e\left(\frac{-(\Delta T_j - T_0)}{\lambda}\right)} \cdot \Delta T_j^{\alpha - e\left(\frac{-(\Delta T_j - T_0)}{\lambda}\right)} \cdot e^{\left(\frac{E_a}{k_B \cdot T_{jm}}\right)} \cdot \frac{C + t_{on}^{\gamma}}{C + 2^{\gamma}} \cdot k_{thickness}$$

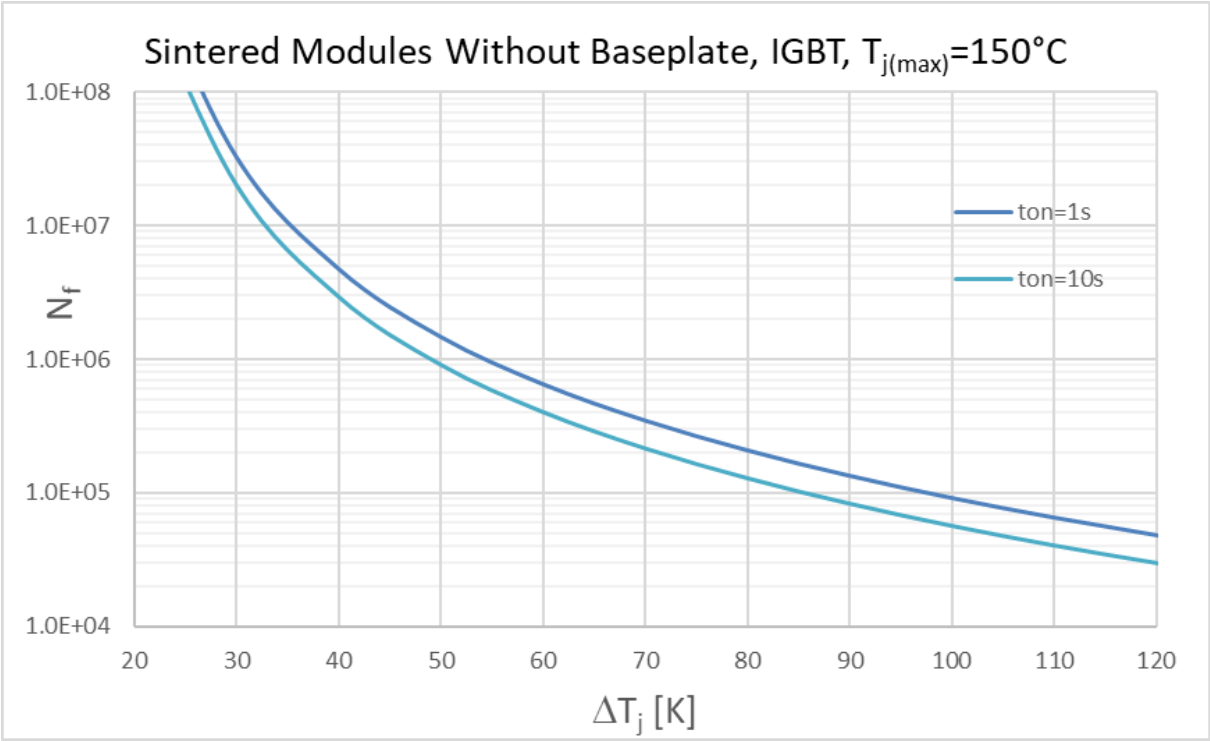
3.3 Modules without baseplate, single side sintered chips and aluminum bond wires

The model is valid for the product families SKiM63/93 and SKiiP4

Table 3: Parameter for power cycle model "Modules with Sintered Chips"

Parameter	Value	Explanation
A_0	2.05E+11	Technology Coefficient
A_1	60	Factor of Low ΔT Extension
T_0 [K]	38	Initial Temperature for Low ΔT Extension
λ [K]	17	Drop Constant of Low ΔT Extension
α	-4.3	Coffin-Manson Exponent
E_a [J]	2.54E-20	Activation Energy
k_B [J/K]	1.38E-23	Boltzmann Constant
C	1.44	Time Coefficient
γ	-1.21	Time Exponent
$k_{thickness}$	1 | 0.65| 0.5 | 0.33	Chip Thickness Factor (see 2.5)

Figure 6: N_f for IGBT in modules without baseplate and single side sintered chips with t_{on}=1s, t_{on}=10s and $T_{j(max)}$=150°C



$$N_f = A_0 \cdot A_1^{e^{\left(\frac{-(\Delta T_j - T_0)}{\lambda}\right)}} \cdot \Delta T_j^{\alpha - e^{\left(\frac{-(\Delta T_j - T_0)}{\lambda}\right)}} \cdot e^{\left(\frac{E_a}{k_B \cdot T_{jm}}\right)} \cdot \frac{C + t_{on}^{\gamma}}{C + 2^{\gamma}} \cdot k_{thickness}$$

Symbols and Terms

Letter Symbol	Term
CTE [ppm/K]	Coefficient of thermal expansion
EOL	End of Life
ΔTj [K]	Temperature swing of a chip
T_j	Virtual junction temperature
T_{jm} [K]	Medium temperature of ΔT (absolute temperature)
t_{on} [s]	Pulse duration, heating time of a power cycle in seconds
V_f, V_{CE}, V_{DS}	Forward voltage of a semiconductor (Diode, IGBT, MOSFET)

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors" [2].

References

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