Application Note
AN 11-001

SEMIKRON DANFOSS

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3L NPC, TNPC & ANPC Topology

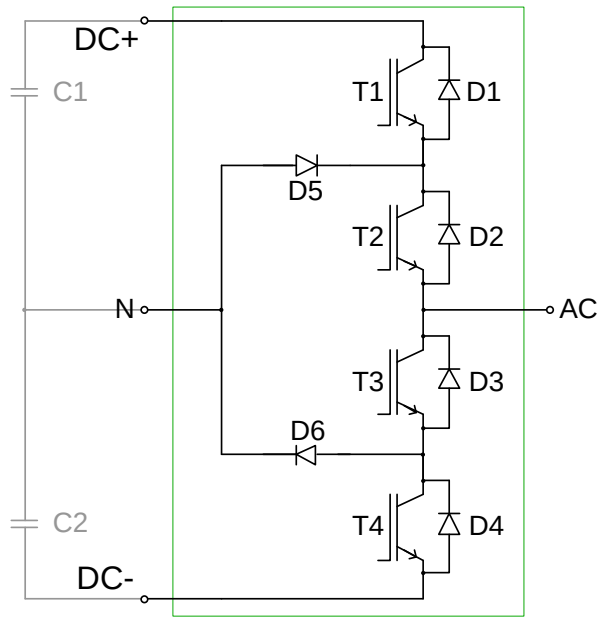
1. Introduction

This Application Note provides information on two three level topologies: the three level NPC (3L NPC; **N**eutral **P**oint **C**lamped), the three level TNPC (3L TNPC; **T**-type **N**eutral **P**oint **C**lamped), and the three level ANPC (3L ANPC; **A**ctive **N**eutral **P**oint **C**lamped). The reader will gain insight in elementary thoughts of how these 3L devices work; where advantages and disadvantages are. Some hints concerning the layout/setup of 3L modules are given as well. However, the information given is not exhaustive and the responsibility for a proper design remains with the user.

2. General

One benefit of using 3L NPC, 3L TNPC, or 3L ANPC topology is the lower current THD; that reduces the filtering effort (less copper needed, lower losses in the filter).
A major advantage of 3L NPC and 3L ANPC is the possibility to use IGBTs and diodes with breakdown voltages that are lower than the actual DC-link voltage. The lower blocking devices produce lower losses and so the efficiency can be increased. By using the same blocking voltage as in a 2L applications higher DC-link voltages can be realized.
Compared to a 2L phase leg module one phase leg of a 3L NPC module consists of 10 instead of 4 semiconductors (Figure 1): 4 **IGBT**s (T1 - T4), 4 antiparallel **F**ree-**W**heeling **D**iodes (FWD; D1 - D4) and 2 **C**lamping **D**iodes (CD; D5 and D6).

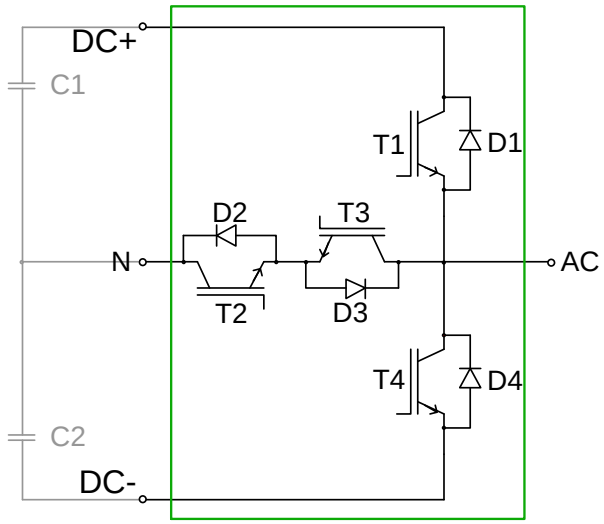
Figure 1: Green box: content of a 3L NPC phase leg



Four power terminals connect the module to AC and to the DC-link: DC+, DC- and N (neutral). The DC-link is split in two symmetric halves connected in series: the upper half connecting DC+ and N and the lower half connecting N and DC-.
In this 3L topology every conduction path consists of two semiconductors in series, and it can either handle higher DC-link voltages or the blocking voltage of the switches can be reduced in comparison to a 2L topology.

The benefit of 3L TNPC is the 3L output voltage waveform while there are no restrictions to the switching scheme as in 3L NPC (especially in emergency shut-down).

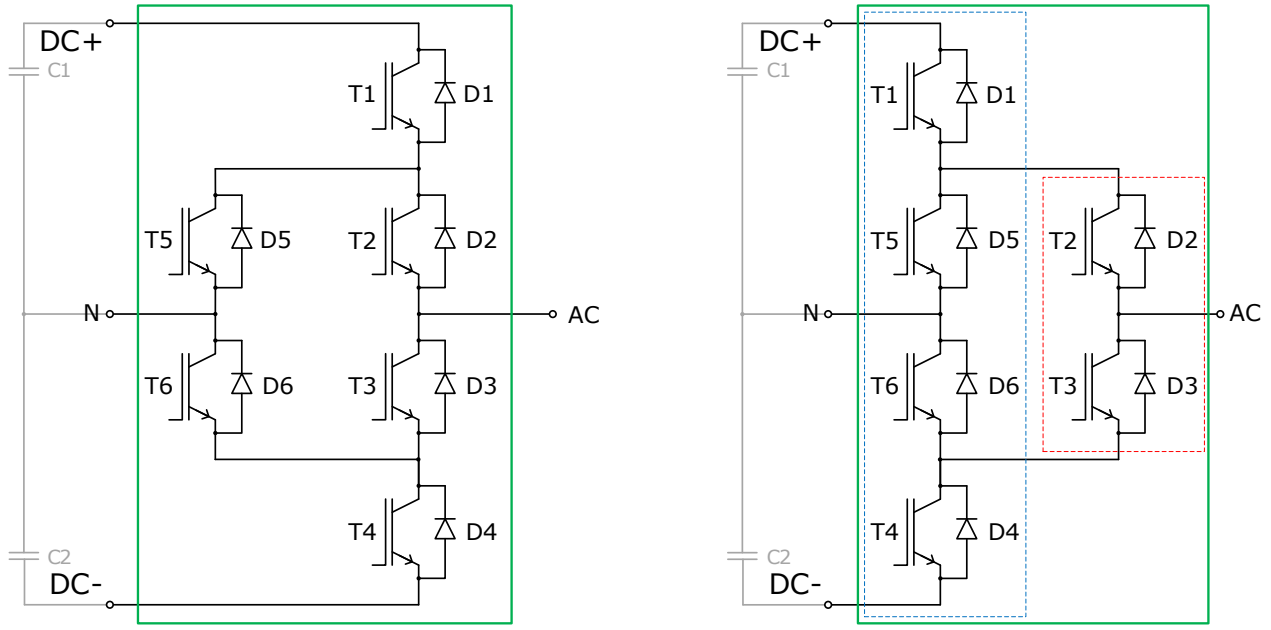
Figure 2: Green box: content of a 3L TNPC phase leg



A 3L TNPC phase leg (Figure 2) consists of only 8 semiconductors: 4 **IGBT**s (T1 - T4) and 4 antiparallel **F**ree-**W**heeling **D**iodes (FWD; D1 - D4). As a 3L NPC the TNPC is connected to the split DC-link at DC+, N, and DC-. The fourth power terminal provides the AC output.
In 3L TNPC topology semiconductors with different breakdown voltages are used: T1 and T4 (which are referred to as outer switches) need to withstand the full DC-link voltage. The inner switches (indices 2 and 3) connect AC to Neutral and must be able to block half of the DC-link voltage.
In 3L TNPC topology the conduction paths are either through one higher blocking semiconductors (outer switch) or two lower blocking devices in series (inner switches).
Naming the semiconductors as shown in Figure 1 and Figure 2 inherits the advantage that the exact same switching pattern can be used for both 3L NPC and 3L TNPC topology.

3L ANPC combines the benefits of 3L NPC and 3L TNPC topologies. As TNPC, it offers a 3L output voltage waveform without restrictions to the switching scheme (especially in emergency shut-down). At the same time it offers the opportunity to use semiconductor devices with breakdown voltages that are lower than the actual DC-link voltage. The lower blocking devices produce lower losses and so the efficiency can be increased.
A 3L ANPC phase leg (Figure 3) consists of 12 semiconductors: 6 **IGBT**s (T1 – T6) and 6 antiparallel **F**ree-**W**heeling-**D**iodes (FWD; D1 – D6). The ANPC is again connected to the split DC-link at DC+, N, and DC-. A fourth power terminal provides the AC connection.
In 3L ANPC topology, as in NPC, every conduction path consists of two semiconductors in series, and it can either handle higher DC-link voltages or the blocking voltage of the switches can be reduced in comparison to a 2L topology.
The ANPC topology consists of an input stage (switches T1, T5, T6, and T4) and an output stage (switches T2 and T3). Due to this allocation to input and output stage, the drawing schematic is slightly shifted in comparison to NPC. The numbering of the input stage has not been adjusted in order to stay consistent with the naming in NPC and TNPC.
In contrast to NPC and ANPC a completely different switching pattern is required for 3L ANPC.
ANPC can be further differentiated in ANPC HF/LF and ANPC LF/HF, where LF stands for "low frequency" (i.e. line frequency, e.g. 50Hz, 60Hz) and HF stands for "high frequency" (i.e. the switching frequency of the inverter, e.g. 10kHz). In ANPC HF/LF the input stage (T1, T5, T6, and T4) are operated at switching frequency ("HF"), while the output stage is operated at line frequency ("LF").

Figure 3: Green box: content of a 3L ANPC phase leg



3. Difference 2L ⇔ 3L

The difference between 2L and 3L topology is not only the number of semiconductor devices. While the well-known 2L converter switches either DC+ or DC- to the AC terminal (Figure 4), the 3L versions connect the AC either to DC+, DC- or N. N(eutral) is the midpoint voltage between DC+ and DC- and forms the third voltage level where the three level topology has its name from.

Figure 4: Voltage and current waveforms of 2L

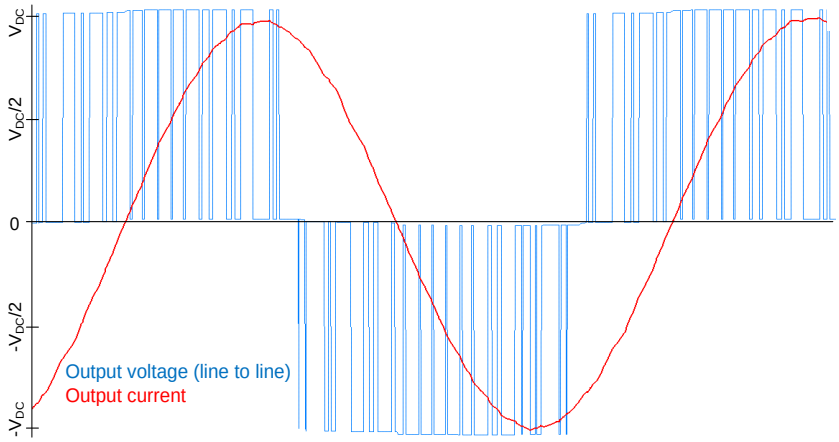
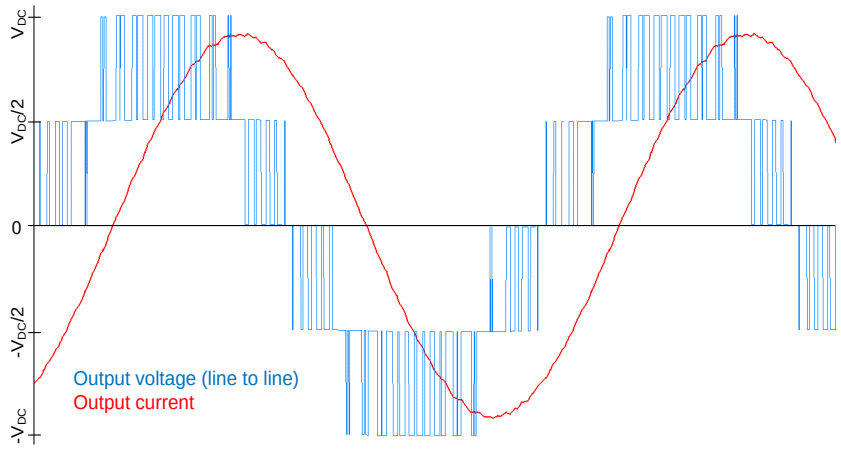


Figure 5: Voltage and current waveforms of 3L



By introducing a third voltage level the waveform of the output voltage is approximated closer to the desired sine waveform (Figure 5) and the current THD can be reduced. Thus, strong requirements concerning grid quality (when feeding to the grid) can be met more easily.

3.1 Comparison of 2L ⇔ 3L NPC/TNPC

3.1.1 NPC, TNPC, ANPC

- For reaching the same current THD value with 3L topology the switching frequency can be reduced leading to reduced switching power losses.
- Subsequently operation at a working point producing the same switching frequency as in 2L topology the current THD can be reduced in 3L topology.
- In 3L applications the switching frequency can be reduced compared to 2L applications, still improving the THD and reducing the filtering effort.
- As the number of IGBTs has increased also the number of gate drivers increases. The auxiliary power consumption grows as well as the control effort.

3.1.2 NPC

- The number of switches in the active current path in 3L NPC topology is doubled; that increases the conduction power losses.
- In 3L NPC applications semiconductors with a lower blocking voltage capability may be used; example: DC-link voltage of 750V can be handled with 1200V 2L or 650V 3L modules (each switch only needs to block 375V). The lower losses of the lower blocking devices compensate the additional losses due to the increased number of devices in the current path.
- The maximum DC-link voltages are $800V_{DC}$ using 650V semiconductors, $1500V_{DC}$ using 1200V semiconductors and $2400V_{DC}$ using 1700V semiconductors.

3.1.3 TNPC

- The number of switches in the active current path in 3L TNPC topology is either similar to 2L (outer switches) producing the same losses or doubled (with lower blocking voltage; inner switches) leading to higher conduction but lower switching losses.
- The maximum DC-link voltages are as for a 2L module: $400V_{DC}$ using 650V semiconductors, $800V_{DC}$ using 1200V semiconductors and $1200V_{DC}$ using 1700V semiconductors.

3.1.4 ANPC

- The number of switches in the active current path in 3L ANPC topology is doubled; that increases the conduction power losses.
- In 3L ANPC applications semiconductors with a lower blocking voltage capability may be used; example: DC-link voltage of 750V can be handled with 1200V 2L or 650V 3L modules (each switch only needs to block 375V). The lower losses of the lower blocking devices compensate the additional losses due to the increased number of devices in the current path.

- The maximum DC-link voltages are $800V_{DC}$ using 650V semiconductors, $1500V_{DC}$ using 1200V semiconductors and 2400VDC using 1700V semiconductors.
- An additional optimization can be achieved by using different semiconductors for input stage and output stage, depending on the chosen PWM pattern (HF/LF or LF/HF; e.g. SiC semiconductors for the HF part).
- ANPC HF/LF can be set up from 2L power modules, while ANPC LF/HF can play its advantages when the whole topology can be integrated into one housing with optimized stray inductances.

4. Switching Pattern of a 3L Converter

The control of 3L applications is more sophisticated than 2L. While the 2L switching pattern is pretty simple (TOP and BOT IGBTs always switch inversely) it gets more complicated at 3L as certain switches (namely T2 and T3 in NPC, TNPC, and ANPC HF/LF) are switched on for quite a while depending on the value of cos φ (up to a half period for cos φ = 1). The number of possible switching states increases from 4 in 2L topology (TOP/BOT: 0/0, 0/1, 1/0, 1/1) to 16 in NPC and TNPC and 64 in ANPC.

4.1 NPC switching states

At 3L NPC a distinction is drawn between allowed, potentially destructive and destructive states (Figure 6).

Figure 6: Switching states NPC

T1	0	0	0	1	0	0	1	0	1	1	0	1	1	1	0	1
T2	0	1	0	1	1	0	0	0	0	0	1	1	1	0	1	1
T3	0	0	1	0	1	1	0	0	0	1	0	1	0	1	1	1
T4	0	0	0	0	0	1	0	1	1	0	1	0	1	1	1	1
state	allowed						potentially destructive					destructive				

Allowed states

- All IGBTs are in off-state; the converter is switched off.
- Either T2 or T3 may be switched on solely.
- Each state where two adjacent IGBTs are switched on (T1/T2, T2/T3, T3/T4).

Potentially destructive states

- Either T1 or T4 is switched on solely or together.
- Two not adjacent IGBTs are switched on (T1/T3 or T2/T4).

The consequences depend on the switching pattern applied to the modules of the other phase legs.

Destructive states

- Three adjacent IGBTs are switched on (T1/T2/T3 → shorting upper half of DC-link; T2/T3/T4 → shorting lower half of DC-link)
- Three not adjacent IGBTs are switched on (T1/T2/T4 → full DC-link voltage applies to T3; T1/T3/T4 → full DC-link voltage applies to T2)
- Four IGBTs switched on → DC+, DC- and N shorted.

4.2 TNPC switching states

At 3L TNPC the distinction is drawn only between allowed and destructive states (Figure 7).

Figure 7: Switching states TNPC

T1	0	1	0	0	0	1	0	0	1	0	1	0	1	1	1	1
T2	0	0	1	0	0	1	1	0	0	1	0	1	0	1	1	1
T3	0	0	0	1	0	0	1	1	1	0	0	1	1	0	1	1
T4	0	0	0	0	1	0	0	1	0	1	1	1	1	1	0	1
state	allowed								destructive							

Allowed states

- All IGBTs are in off-state; the converter is switched off.
- Any one of the IGBTs may be switched on solely.
- Each state where two adjacent IGBTs are switched on (T1/T2, T2/T3 or T3/T4).

Destructive states

- Two not adjacent IGBTs are switched on (T1/T3 → shorting upper half of DC-link; T2/T4 → shorting lower half of DC-link; T1/T4 → shorting DC+ and DC-).
- Three not adjacent IGBTs are switched on (same consequences as above: shorting either upper half or lower half or the full DC-link)
- Four IGBTs switched on → DC+, DC- and N shorted

(TOP/BOT: 0/0, 0/1, 1/0, 1/1) to 16 in NPC and TNPC and 64 in ANPC.

4.3 ANPC switching states

Allowed states

- All IGBTs are in off-state; the converter is switched off.
- Either T2, T3, T5, or T6 may be switched on solely or T5/T6 together.
- Any combination of T1/T6 or T5/T4 together (not adjacent switches in the input stage), additionally either T2 or T3.

Potentially destructive states

- Either T1 or T4 is switched on solely or together.

The consequences depend on the switching pattern applied to the modules of the other phase legs.

- T2 and T3 are switched on together

The consequences depend on the symmetry of the voltage sharing of T1 and T4.

Destructive states

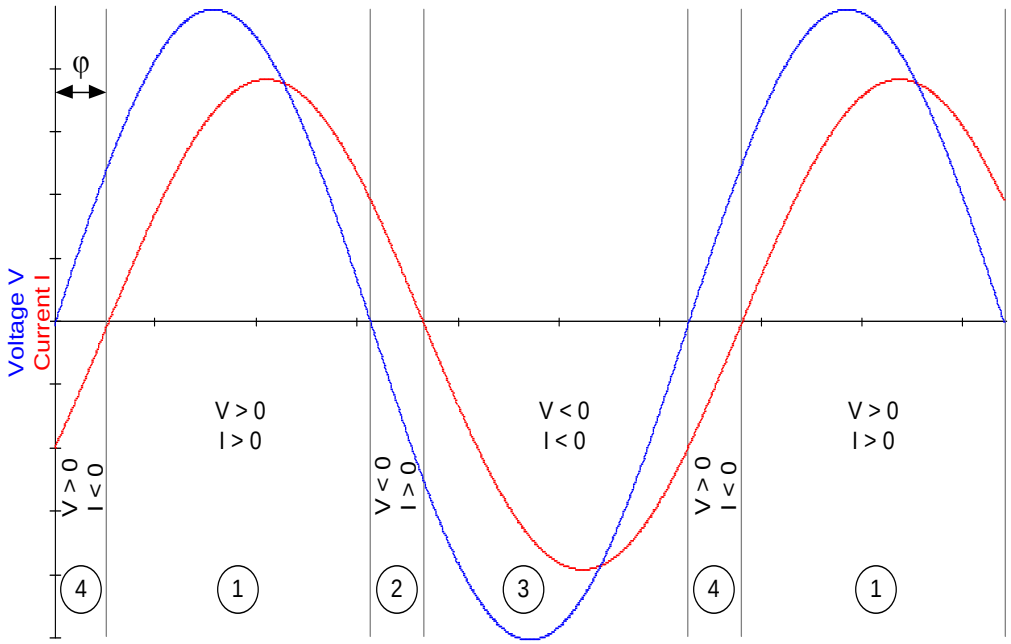
- Two adjacent IGBTs are switched on (T1/T5 → shorting upper half of DC-link; T6/T4 → shorting lower half of DC-link)
- Three adjacent IGBTs are switched on (T1/T2/T3 → shorting upper half of DC-link and T4 exposed to dull DC-link voltage; T2/T3/T4 → shorting lower half of DC-link and T1 exposed to full DC-link voltage)
- Three not adjacent IGBTs are switched on (T1/T2/T4 → full DC-link voltage applies to T3; T1/T3/T4 → full DC-link voltage applies to T2)
- Four IGBTs switched on (T1/T2/T3/T4) → DC+ and DC- shorted or (T1/T5/T6/T4) → DC+, DC- and N shorted.
- Five or six switches turned on lead to several short circuits or exposure of one device to full DC-link voltage.

5. Commutations and Commutation Paths

5.1 NPC, TNPC & ANPC

Figure 8 shows a sine voltage (blue trace) and the related current (red trace) at inductive load. The inverter operation can be divided in four operating areas. For cos φ = +1 (no phase shift) voltage and current waveforms are in phase; only working areas 1 and 3 are active. For cos φ = -1 (180° phase shift) only working areas 2 and 4 are active.

Figure 8: Operating areas



For any value of cos φ between -1 and +1 the phase shift changes and so do the time shares of the four working areas.

The active switches and the relevant commutations for these four working areas are listed below:

1. both voltage and current are greater than 0 (V > 0, I > 0):
   - 2L: $T_{TOP} \leftrightarrow D_{BOT}$
   - 3L NPC: T1/T2 ↔ D5/T2 (*short commutation path*)
   - 3L TNPC: T1 ↔ T2/D3
   - 3L ANPC (HF/LF): T1/T2 ↔ D5/T2 (*short commutation path*)
   - 3L ANPC (LF/HF): T1/T2 ↔ D3/T6 (*long commutation path*)

1.1 transition from operating area 1 to operating area 2:
   - 3L ANPC (HF/LF): T1/T2 ↔ T6/D3 (*long commutation path*)
     D6/T2 ↔ D3/D4 (*long commutation path*)
   - 3L ANPC (LF/HF): T1/T2 ↔ D5/T2 (*short commutation path*)
     T6/D3 ↔ D3/D4 (*short commutation path*)

2. voltage is less and current is greater than 0 (V < 0, I > 0):
   - 2L: $T_{TOP} \leftrightarrow D_{BOT}$
   - 3L NPC: D5/T2 ↔ D3/D4 (*long commutation path*)
   - 3L TNPC: T2/D3 ↔ D4
   - 3L ANPC (HF/LF): T6/D3 ↔ D3/D4 (*short commutation path*)
   - 3L ANPC (LF/HF): D5/T2 ↔ D3/D4 (*long commutation path*)

3. both voltage and current are less than 0 (V < 0, I < 0):
   - 2L: $T_{BOT} \leftrightarrow D_{TOP}$
   - 3L NPC: T3/T4 ↔ T3/D6 (*short commutation path*)
   - 3L TNPC: T4 ↔ T3/D2
   - 3L ANPC (HF/LF): T3/T4 ↔ T3/D6 (*short commutation path*)
   - 3L ANPC (LF/HF): T5/D2 ↔ T3/T4 (*long commutation path*)

3.1 transition from operating area 3 to operating area 4:
   - 3L ANPC (HF/LF): T3/T4 ↔ T5/D2 (*long commutation path*)

	D1/D2 ↔ T3/D6 (*long commutation path*)
3L ANPC (LF/HF):	T3/T4 ↔ T3/D6 (*short commutation path*)
	D2/T5 ↔ D1/D2 (*short commutation path*)

4. voltage is greater and current is less than 0 (V > 0, I < 0):

2L:	T_{BOT} ↔ D_{TOP}
3L NPC:	T3/D6 ↔ D1/D2 (*long commutation path*)
3L TNPC:	T3/D2 ↔ D1
3L ANPC (HF/LF):	T5/D2 ↔ D1/D2 (*short commutation path*)
3L ANPC (LF/HF):	D1/D2 ↔ D6/T3 (*long commutation path*)

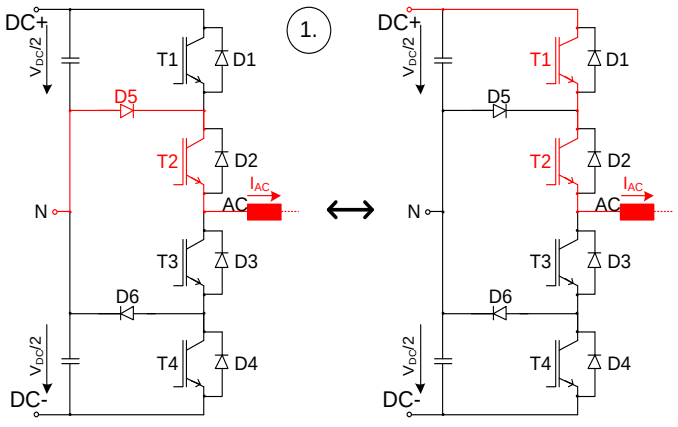
The commutations are different for ANPC HF/LF and ANPC LF/HF:

- ANPC HF/LF uses only short commutation paths within the four operating areas but inherits large stray inductances (i.e. long commutation paths) for the transitions between operating area 1 and 2 (respectively 3 and 4). That makes it suitable for a setup from standard 2L power modules with rather easy bus-bar connections.
- ANPC LF/HF, however, comes with long commutation paths within the operating areas, and short paths for the transitions. Due to larger stray inductances for the long commutation loops it is not suitable for a setup from 2L modules; all semiconductors need to be inside one housing with optimized commutation paths. The advantages in ANPC LF/HF lies in the reduced number (and therefore reduced cost) of HF switches in case fast switching semiconductors shall be used (SiC, etc.).

5.2 NPC

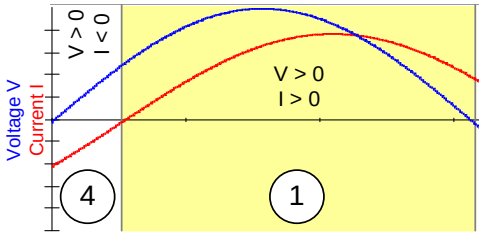
While in a "short commutation path" the commutation affects only one of the two active switches (e.g. T1 ↔ D5) the current through the other active switch does not change (e.g. T2). In a "long commutation path" (e.g. D5/T2 ↔ D3/D4) both devices are affected.
The name "short/long commutation path" also indicates the geometric length of the commutations, while the short commutation takes place either within the upper or the lower half of the 3L module in a long commutation the current changes from the upper to the lower half (or vice versa).

Figure 9: Short commutation path for NPC operating area 1



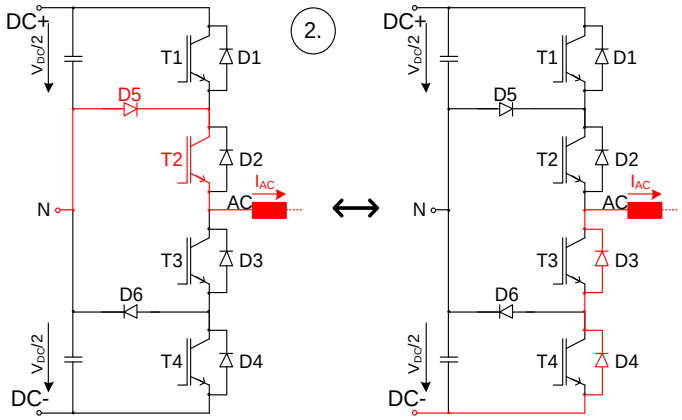
The short commutation (Figure 9) in the upper half of the module (device indices 1, 2 and 5) is active in operating area 1 (Figure 10); both voltage and current are positive.
The commutation goes back and forth between T1 and D5; the current flows from DC+ via T1 and T2 to the AC terminal as long as T1 is switched on. When T1 switches off, the current commutates to the clamping diode D5; now the current flow is from N via D5 and T2 to AC. T2 stays switched on all the time.

Figure 10: Operating area 1



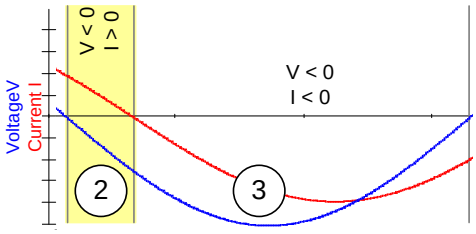
The long commutation for positive output current (Figure 11) goes back and forth between D5/T2 in the upper half of the module and D3/D4 in the lower half => across the entire device.

Figure 11: Long commutation path for NPC operating area 2



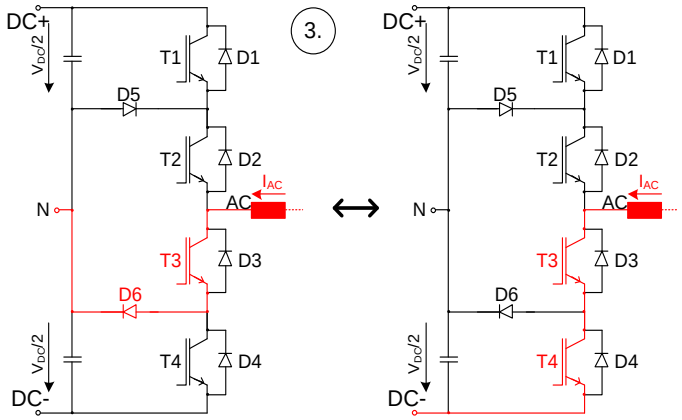
This commutation across the entire device is due to the fact that in operating area 2 (Figure 12) the current is still positive (flowing from the DC-link towards the load) while the output voltage is negative.

Figure 12: Operating area 2



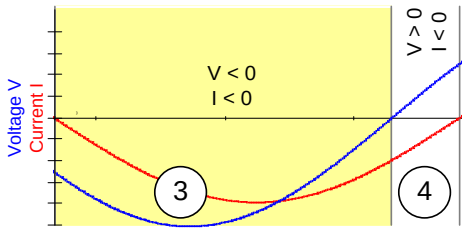
The other short commutation path is active in operating area 3 (Figure 13 and Figure 14), in the lower half of the module. Output current and voltage are negative.

Figure 13: Short commutation path for NPC operating area 3



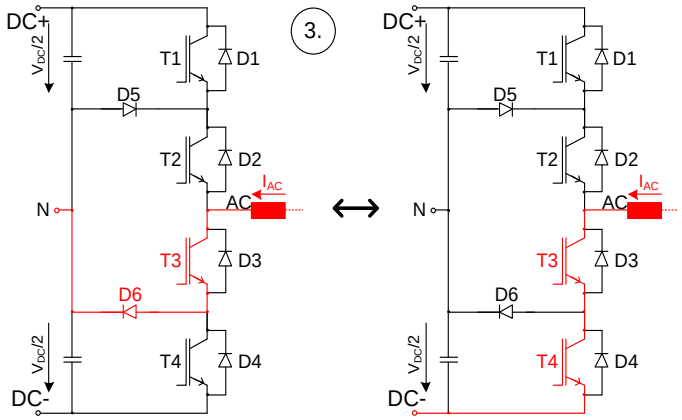
The commutation goes back and forth between T4 and D6; the current flows from the AC terminal across T3 and T4 to DC- as long as T4 is switched on. As soon as T4 switches off, the current commutates to the clamping diode D6; the new conduction path is from AC vie T3 and D6 to N. T3 stays switched on all the time.

Figure 14: Operating area 3



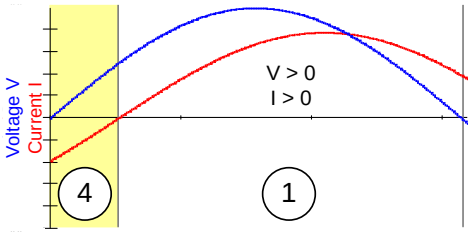
The long commutation path for negative current (Figure 15) goes back and forth between D6/T3 in the lower half of the module and D1/D2 in the upper half across the entire device.

Figure 15: Long commutation path for NPC operating area 4



The long commutation in operating area 4 (Figure 16) comes with negative output current (flowing from the AC terminal towards the DC-link) and positive voltage.

Figure 16: Operating area 4

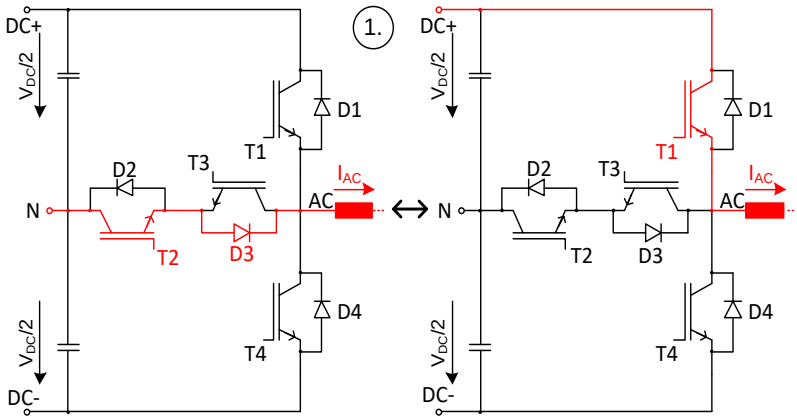


5.3 TNPC

There are no "short" or "long" commutation paths in TNPC topology; all paths are of the same geometric length and inherit one outer switch (indices 1 or 4; either IGBT or diode) and two inner switches (either T2 and D3 or T3 and D2). In normal operation the commutation always affects one outer and two inner switches; there is no commutation between T1/D1 and T4/D4.

In operating area 1 (Figure 17 and Figure 10) output voltage and current are positive, the current flows towards the AC terminal. The commutation goes back and forth between T1 and T2/D3; the current flows from DC+ via T1 to the AC terminal as long as T1 is switched on. When T1 switches off, the current commutates to the inner switches T2/D3; the current now flows from N via T2 and D3 to AC. T2 stays switched on all the time; as soon as T1 is switched on, the diode D3 blocks the voltage and so avoids a short cut of the upper half of the DC-link.

Figure 17: Commutation path for TNPC operating area 1



In operating area 2 (Figure 18) the output current is still positive while the voltage is negative (Figure 12). It commutates back and forth between the inner switches T2/D3 and the diode D4.

Figure 18: Commutation path for TNPC operating area 2

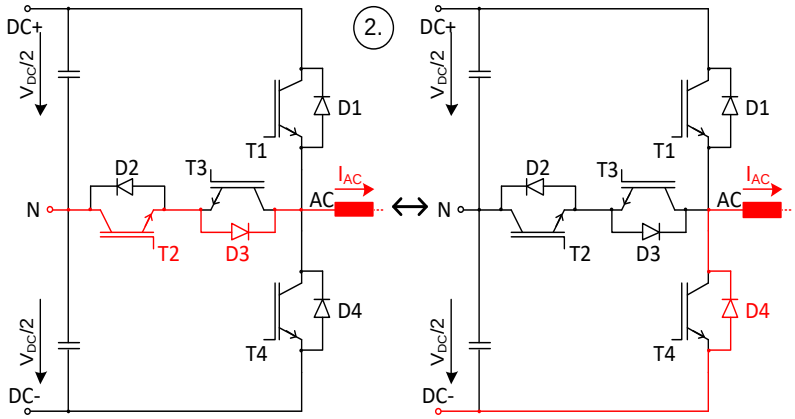
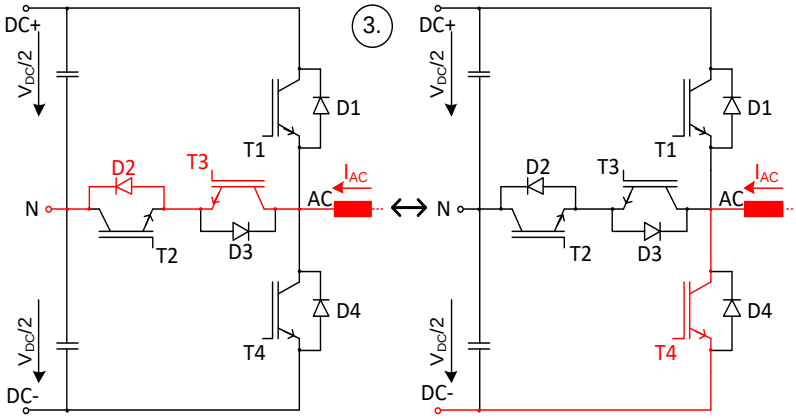


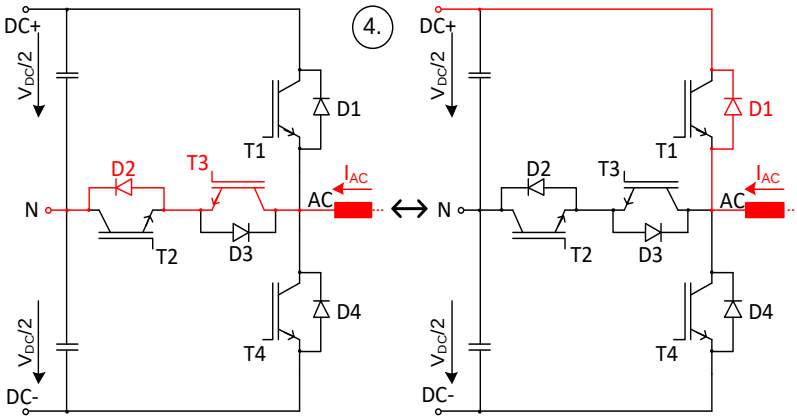
Figure 19 shows the conduction paths of operating area 3; the current commutates between T4 and the inner switches T3/D2. The current flows from the AC terminal to the DC-link and, current and voltage are negative (see Figure 14). T3 stays switched on permanently as long as T4 is switched on as well the diode D2 blocks the voltage and avoids shorting the negative half of the DC-link.

Figure 19: Commutation path for TNPC operating area 3



In operating area 4 (Figure 20) the output current is negative while the voltage is positive (Figure 16). The current commutates back and forth between the inner switches T3/D2 and the diode D1.

Figure 20: Commutation path for TNPC operating area 4

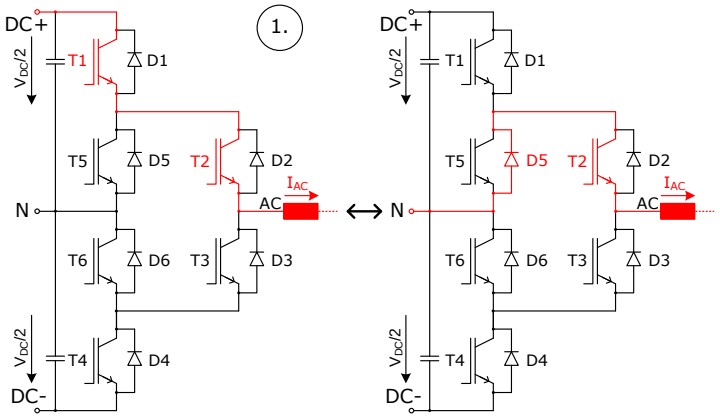


5.4 ANPC HF/LF

At ANPC HF/LF the input stage pulses with the switching frequency ("HF", e.g. 10kHz), while the output stage pulses with the line frequency ("LF", e.g. 50Hz). The output stage switches back and forth between positive and negative output voltage.
In the "HF" part of ANPC only short commutation paths are used as the current commutates between neighboured switches only. During each short commutation, only two switches are affected.
As soon as the output voltage needs to change polarity, that is either a transition from operating area 1 to operating area 2 (positive → negative), or a transition from operating are 3 to operating area 4 (negative → positive), a long commutation loop is used, which inherits four switches.

In operating area 1 (Figure 10 and Figure 21) output voltage and current are positive, the current flows towards the AC terminal. The commutation goes back and forth between T1 and D5; the current flows from DC+ via T1 and T2 to the AC terminal as long as T2 is switched on. When T1 switches off, the current commutates to D5; the current now flows from N via D5 and T2 to AC. T2 stays switched on all the time.

Figure 21: Commutation path for ANPC HF/LF operating area 1



In operating area 2 (Figure 22) the output current is still positive while the voltage is negative (Figure 12). It commutates back and forth between T6 and D4.

Figure 22: Commutation path for ANPC HF/LF operating area 2

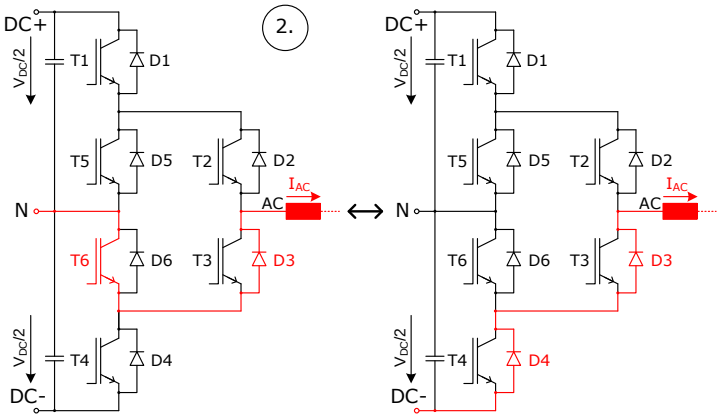
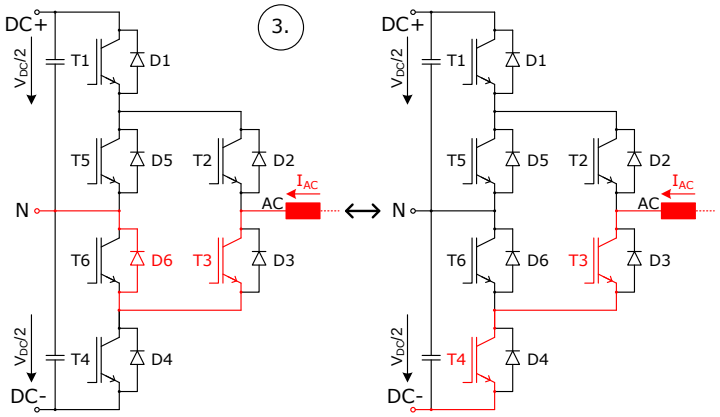


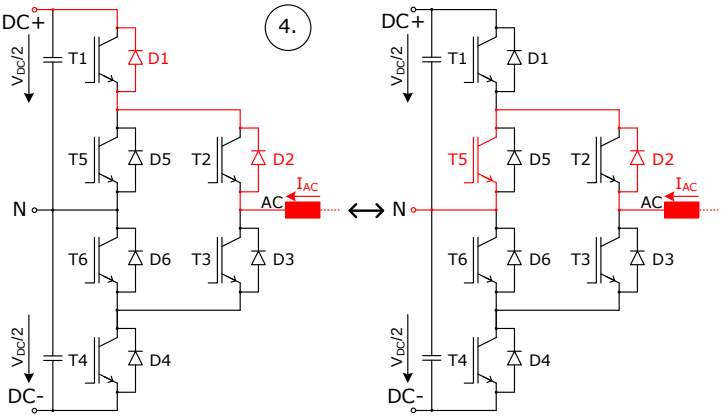
Figure 23 shows the conduction paths of operating area 3; the current commutates between T4 and D6. The current flows from the AC terminal to the DC-link and current and voltage are negative (see Figure 14). T3 stays switched on permanently.

Figure 23: Commutation path for ANPC HF/LF operating area 3



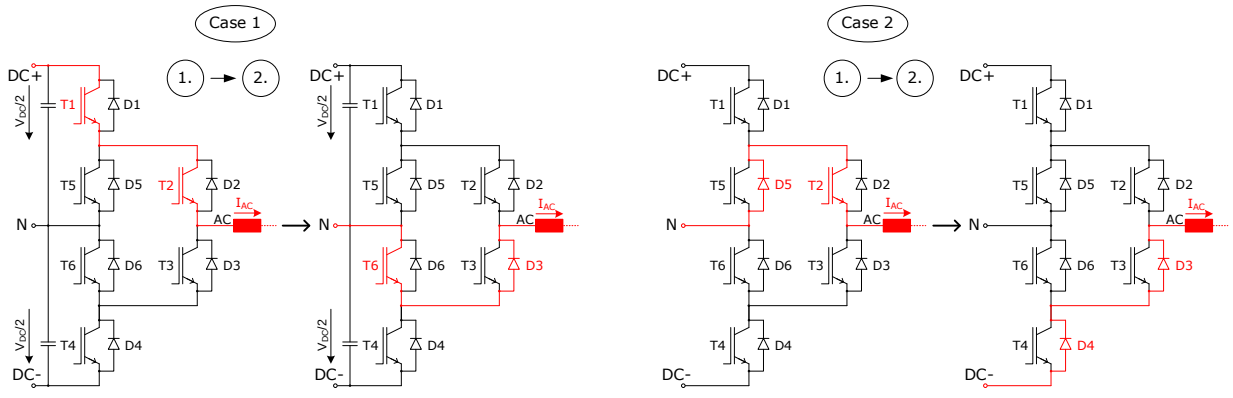
In operating area 4 (Figure 24) the output current is negative while the voltage is positive (Figure 16). The current commutates back and forth between T5 and D1.

Figure 24: Commutation path for ANPC HF/LF operating area 4



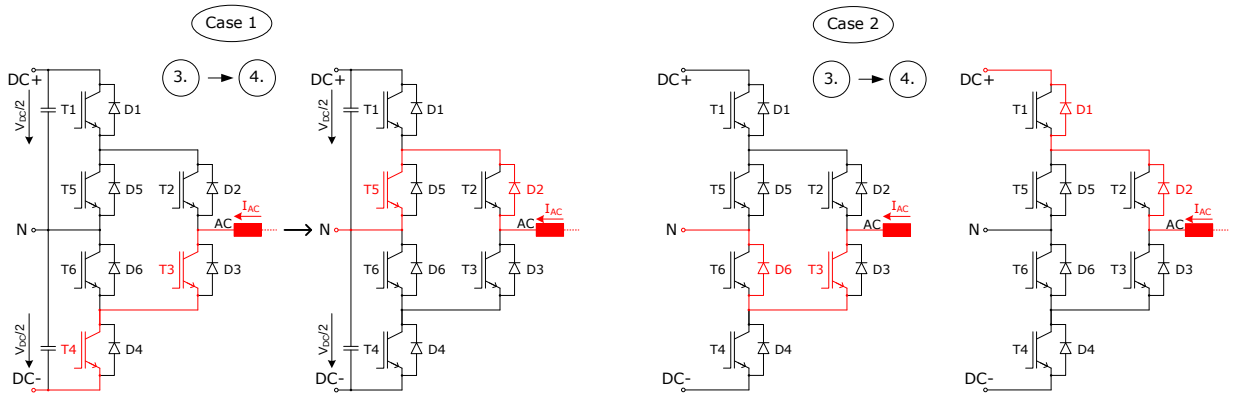
The transition between positive and negative output voltage inherits a long commutation across four switches; T2 is turned off for a half period, T3 turned on (Figure 25).

Figure 25: Transitions between ANPC HF/LF operating area 1 and operating area 2



The transition in the other direction, negative to positive output voltage inherits again a long commutation across four switches; T3 is turned off for a half period, T2 turned on (Figure 26).

Figure 26: Transitions between ANPC HF/LF operating area 3 and operating area 4



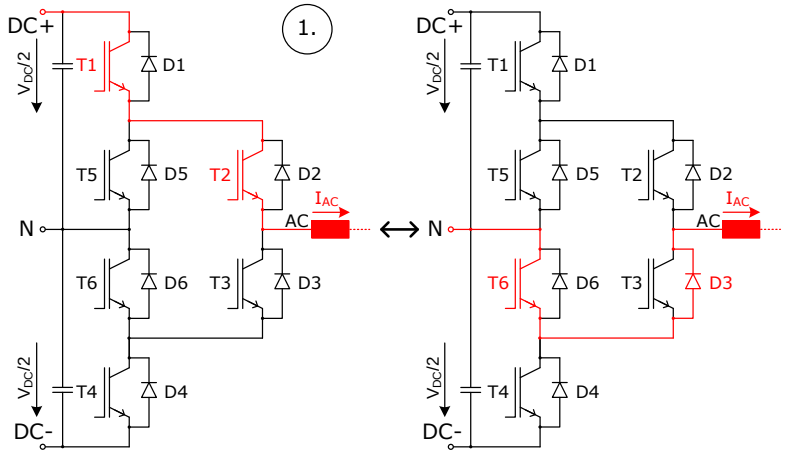
In addition to the two shown transitions between operating areas 1 and 2 (Figure 25) and operating areas 3 and 4 (Figure 26) a third transition is possible directly from DC+ to DC- inheriting the largest possible stray inductance. Hence it will never be used. A fourth transition is the transition of two paths both leading from N to AC (or vice versa). In operation the fourth path has no use and will therefore also not be used.

5.5 ANPC LF/HF

At ANPC LF/HF the input stage pulses with the line frequency ("LF", e.g. 50Hz), while the output stage pulses with the switching frequency ("HF", e.g. 10kHz).
The input stage switches back and forth between positive and negative output voltage.
The "HF" part of ANPC LF/HF switches long commutation paths only. Therefore ANPC LF/HF is most suitable for small power module all-in-one packages, where the commutation loops can be optimized regarding stray inductance.
Changing the polarity of the output voltage either a transition from operating area 1 to operating area 2 (positive → negative), or a transition from operating are 3 to operating area 4 (negative → positive) is required, which inherits a short commutation loop.

In operating area 1 (Figure 10 andFigure 27) output voltage and current are positive, the current flows towards the AC terminal. The commutation goes back and forth between T1/T2 and T6/D3; the current flows from DC+ via T1 and T2 to the AC terminal as long as T2 is switched on. When T2 switches off, the current commutates to T65; the current now flows from N via T6 and D3 to AC. T1 and T6 stay switched on all the time.

Figure 27: Commutation path for ANPC LF/HF operating area 1



In operating area 2 (Figure 28) the output current is still positive while the voltage is negative (Figure 12). It commutates back and forth between D5/T2 and D3/D4. T4 and T5 stay switched on all the time.

Figure 28: Commutation path for ANPC LF/HF operating area 2

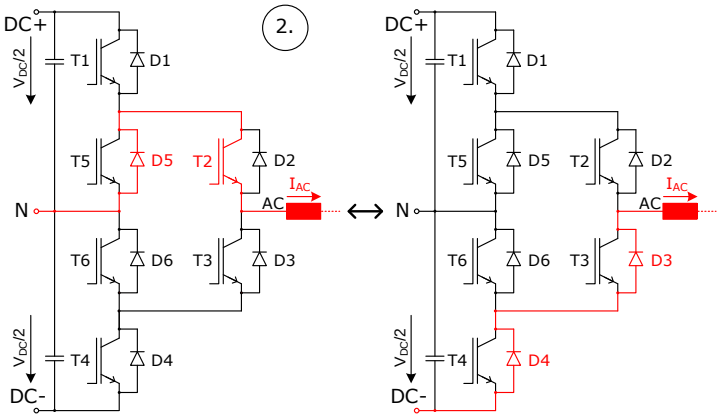
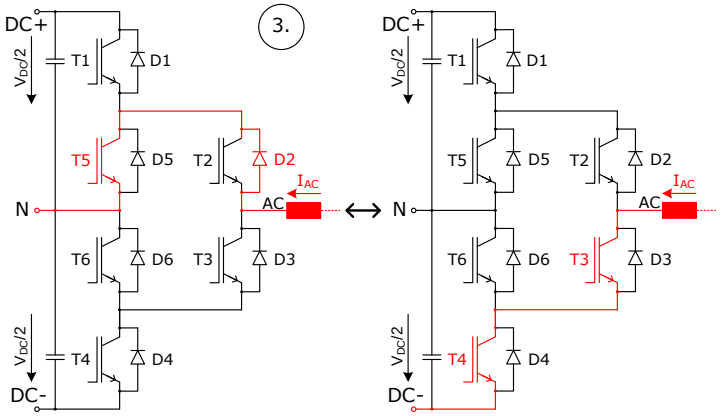


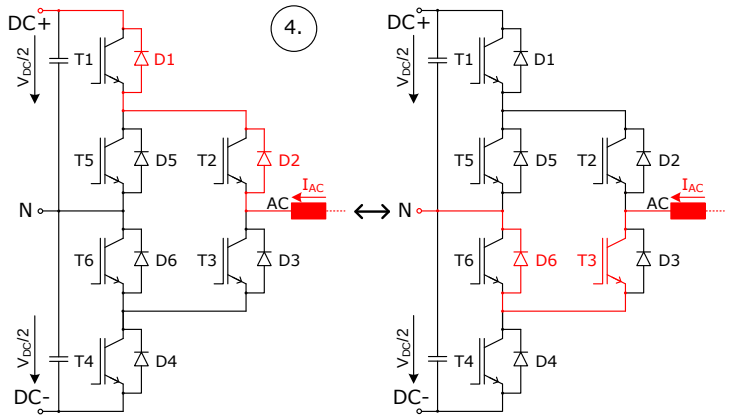
Figure 29 shows the conduction paths of operating area 3; the current commutates between T5/D2 and T3/T4. The current flows from the AC terminal to the DC-link and current and voltage are negative (see Figure 14). T4 and T5 stay switched on permanently.

Figure 29: Commutation path for ANPC LF/HF operating area 3



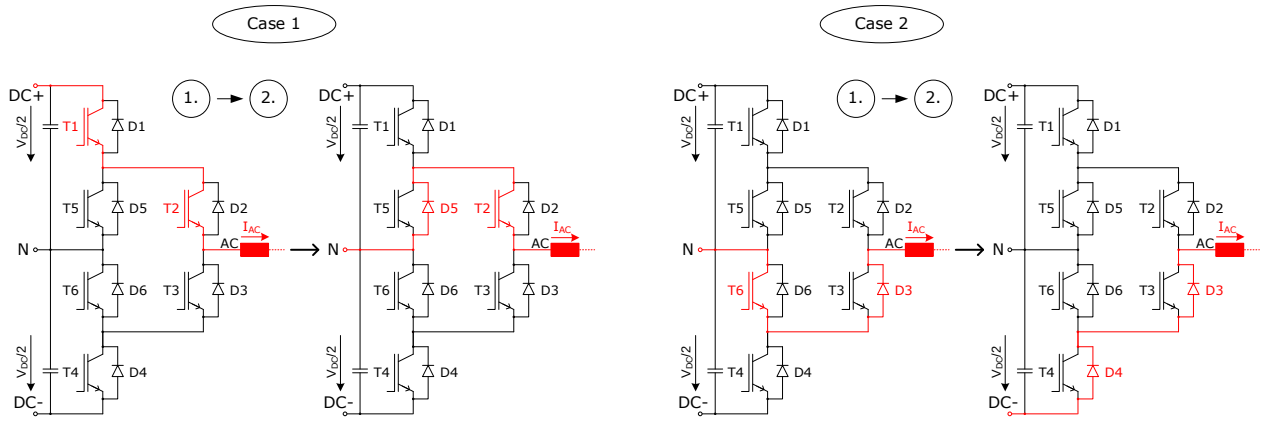
In operating area 4 (Figure 30) the output current is negative while the voltage is positive (Figure 16). The current commutates back and forth between D1/D2 and T3/D6. T1 and T6 stay switched on all the time.

Figure 30: Commutation path for ANPC LF/HF operating area 4



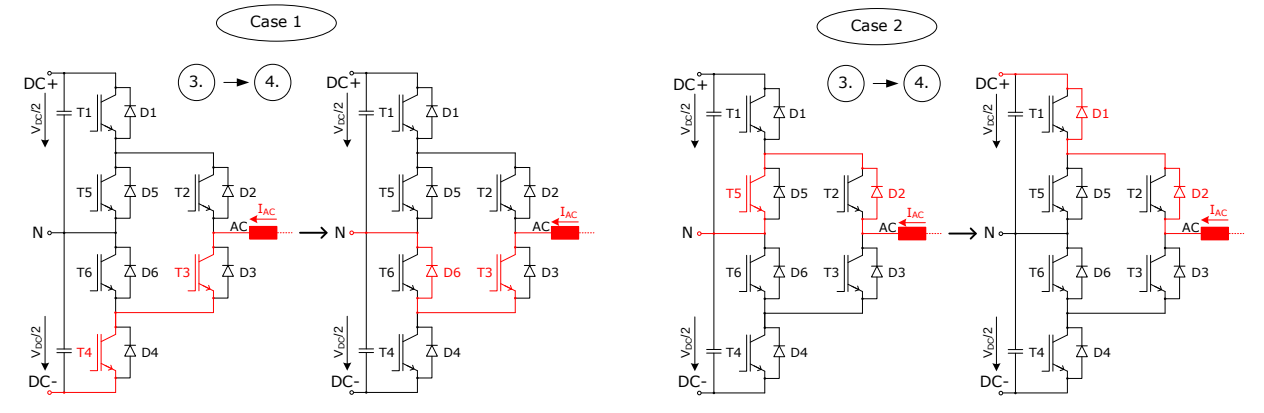
The transition between positive and negative output voltage inherits a short commutation across two switches (Figure 31).

Figure 31: Transitions between ANPC LF/HF operating area 1 and operating area 2



The transition in the other direction, negative to positive output voltage inherits again a short commutation across two switches (Figure 32).

Figure 32: Transitions between ANPC LF/HF operating area 3 and operating area 4



6. 3L Converter

6.1 Module consideration

When a dedicated 3L module is designed, especially the commutation paths find consideration: large commutation paths inherit large stray inductances. When the load current through a conduction path with large stray inductance is switched off, high voltage overshoots occur. To avoid a destruction of the semiconductor, the voltage overshoot must stay below its blocking voltage. That can be reached by either reducing the maximum allowed DC-link voltage and allowing higher overshoots or by reducing the stray inductances producing less overshoots.
Of course, the aim is to reduce the stray inductance and allow higher DC-link voltages (that increases the possible AC output voltage and so the module power).
A special case is ANPC HF/LF, when set up from 2L modules. The larger stray inductance of the long commutation loops of the "LF" path can be handled by using larger gate resistors to slow down the particular semiconductor and thus the di/dt to reduce the voltage overshoot. The resulting higher switching energies that need to be dissipated can be accepted as the "LF" path switches very rarely (with line frequency) and the contribution to the total switching energies is not important.

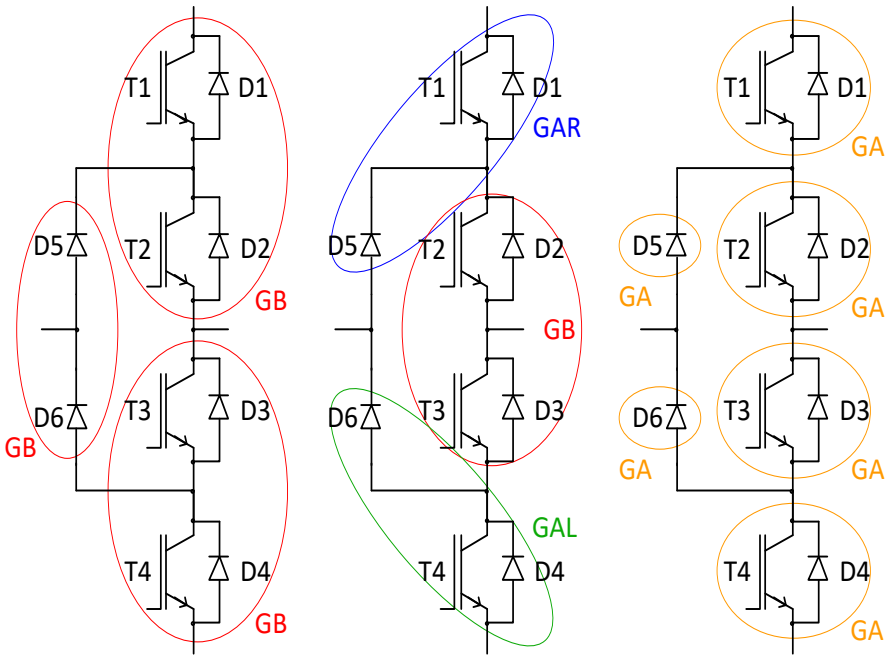
6.2 Setup with standard 2L modules

Theoretically 3L topologies can be set up with already existing standard 2L modules (Figure 33 and Figure 34). The assembly would require bus bar interconnection of the modules and would be very scalable.

NPC

Practically the NPC setup from 2L modules (Figure 33) inherits always very long conduction paths, especially for the commutations across module boundaries (that gets even worse for the long commutation paths).
Due to the stray inductance these large commutation paths produce very high voltage overshoots so that the shown setups offer no advantages in regard to 2L designs.

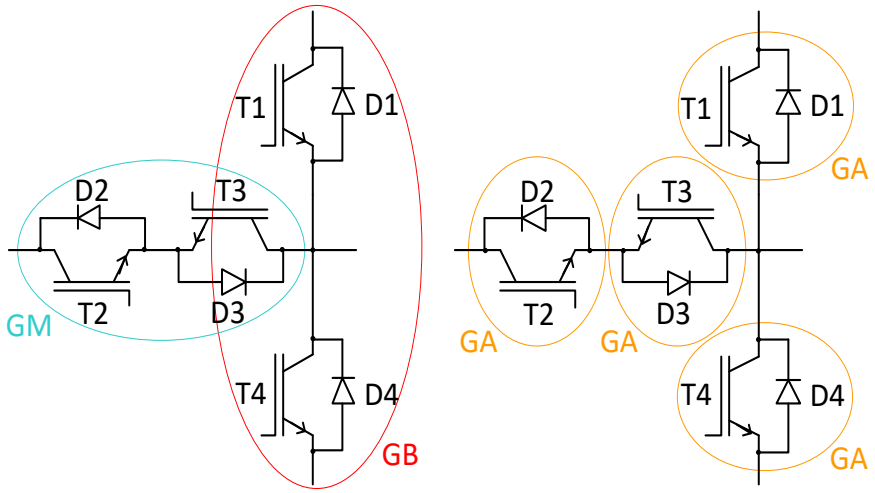
Figure 33: Configurations to set up a 3L NPC design from 2L modules



TNPC

In the TNPC setup from 2L modules (Figure 34) every commutation path is across module borders. Like the NPC setup stray inductances lead to high voltage overshoots which make this solution unattractive.

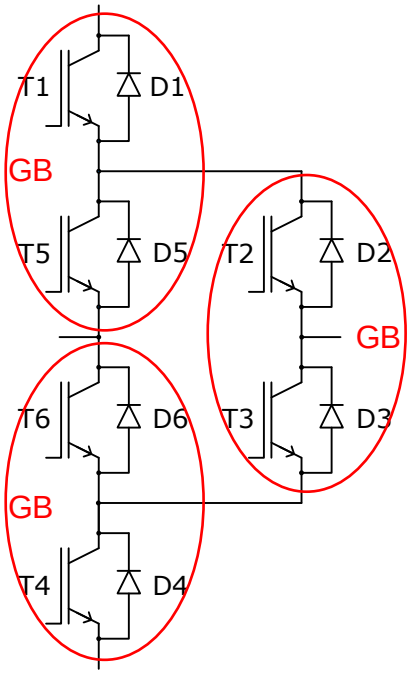
Figure 34: Configurations to set up a 3L TNPC design from 2L modules



ANPC

ANPC can be set up from 2L modules as shown in Figure 35.
Using ANPC HF/LF the big number of commutations takes place in the "HF" part, between switches 1 and 5 (6 and 4 respectively), so within already optimized 2L modules. Only the change in output voltage polarity inherits a long commutation path across all 2L modules. As that takes place with line frequency only, it has no big contribution to the total switching energies, if these long commutations are slowed down to decrease voltage overshoots by using larger gate resistors (which increases the switching energies of these particular commutations).
For ANPC LF/HF a setup from 2L modules is not attractive, as the big number of commutations goes across all 2L modules. Slowing down the switching speed would have a large impact on switching energies. Thus, a ANPC LF/HF should be a dedicated all-in-one power module with internally optimized commutation paths.

Figure 35: Configurations to set up a 3L ANPC design from 2L modules



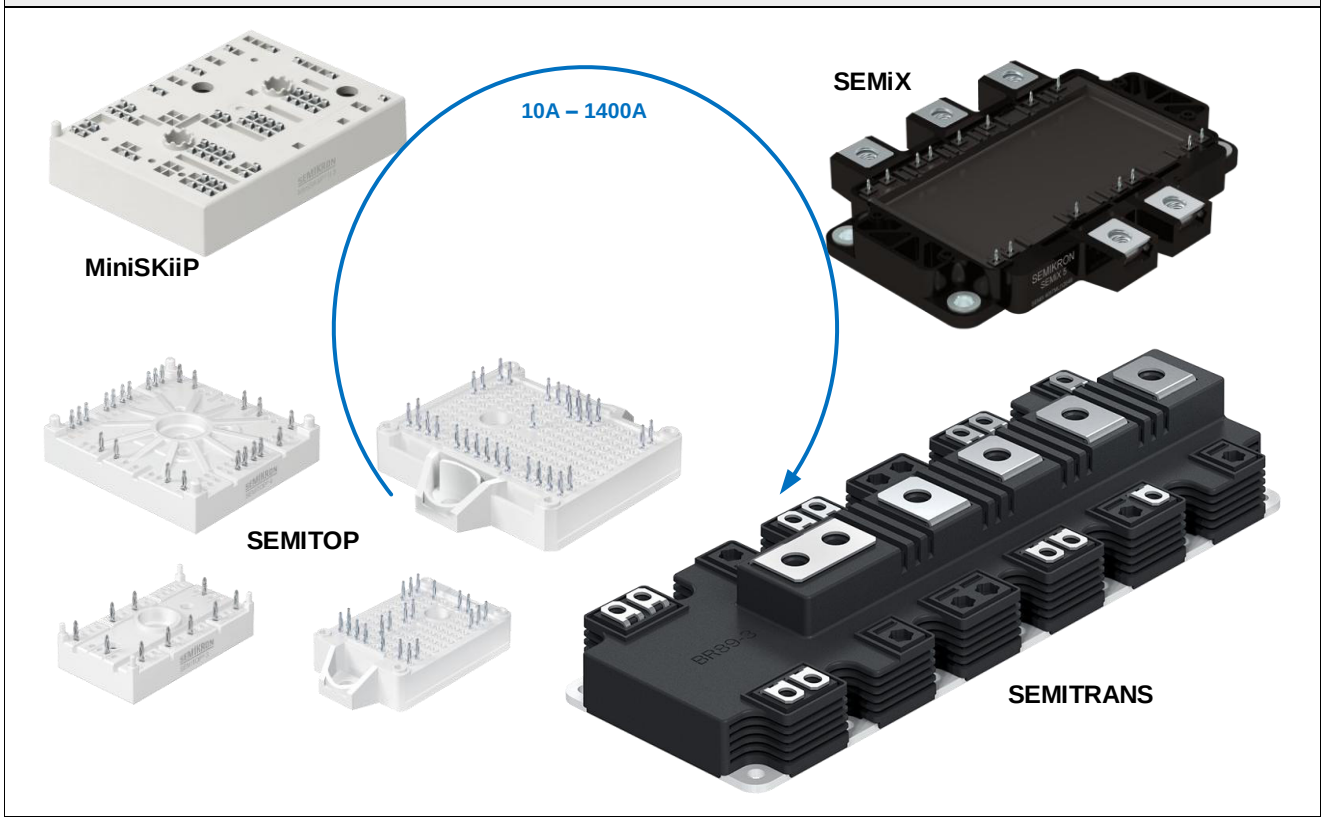
6.3 Dedicated 3L modules

As the 3L topology setup from 2L modules appears not to be the best solution, new module designs facing the special requirements coming with the 3L technology need to be made.
At the very beginning a choice must be made concerning the module size and the related electric module power: the bigger the module shall become the more power it can provide as large chip area is available. Unfortunately, larger module size also stands for higher stray inductances leading to high switching voltage overshoots thus limiting the maximum current.
High power can either be realized by one large module or by many smaller modules in parallel. The latter solution requires an equally high number of driving units that need to be parallelized (with known problems: cost, space, jitter of separate drivers, compensation current when using paralleled drivers…).

6.4 Semikron Danfoss 3L modules

Semikron Danfoss provides a number of 3L modules that have been specially designed to minimize stray inductance. The module range starts with SEMITOP at a rated chip current of 10A to 150A followed by MiniSKiiP (75A - 400A) up to SEMiX modules with 150A - 600A rated current. SEMITRANS is offered as split topology (two power modules inherit one 3L phase leg) up to 1400A.
Figure 36 shows an excerpt of the power modules offered with either NPC, TNPC, or ANPC topology in different voltage classes. Please visit our website [1] for more and detailed information.

Figure 36: Semikron Danfoss 3L module portfolio (excerpt)



7. Driving 3L Devices

7.1 Normal operation sequences

When all devices are switched off and the 3L NPC or TNPC converter starts operation it must be one of the inner IGBTs to be switched on first. In case of positive output voltage that is T2. After a short while (when T2 is entirely switched on) T1 may be pulsed. For the switch-off sequence the reverse order must be maintained: it must be made sure that T1 is thoroughly switched off before T2 may be turned off. That can be achieved by turning off T2 a short time (1..3µs) after the turn-off signal for T1 has occurred; this dead time is well known as interlock-time between TOP and BOT switch at Semikron Danfoss 2L gate drivers.

NPC & TNPC

The gate signals of T1 and T3 (T2 and T4 respectively) are invers. It has to be made sure that one IGBT is securely switched off before the other one is switched on.

NPC

When an inner IGBT (T2 or T3) is switched off before the corresponding outer IGBT (T1 or T4) the inner switch would be exposed to the full DC-link voltage. In case this voltage was higher than the blocking voltage of that semiconductor it would be destroyed.
As shown in Figure 6 there are switching patterns that are not allowed because they are destructive. Those states must be avoided if the device shall not be destroyed.

TNPC

The same rules as stated for NPC also apply for TNPC converters. When an inner IGBT (T2 or T3) is switched off before the corresponding outer IGBT (T1 or T4) the load current would commutate from an outer IGBT (T1 or T4) to an outer diode (D4 or D1). This commutation path inherits a higher inductance and thus the outer IGBT switching off would be exposed to a higher voltage overshoot. In case this overshoot exceeded the blocking voltage of that semiconductor it would be destroyed.
Subsequently turning off in different order or turning off all IGBT simultaneously is only possible when the semiconductors' blocking voltages are not exceeded.
As shown in Figure 7 there are switching patterns that are not allowed because they are destructive. Those states must be avoided if the device shall not be destroyed.

ANPC

Also, for ANPC the outer switches T1 (switching simultaneously with T6) and T4 (switching simultaneously with T5) have to be switched off before the inner switches T2 and T3. Otherwise, the inner switch could be exposed to the full DC-link voltage which usually exceeds the blocking voltage of the semiconductor leading to its destruction.

7.2 Emergency shut-down

There are several events that may occur which in 2L application lead to immediate switch-off by the driver to protect the semiconductors. Imaginable events are:

- thermal overload
- current overload or
- desaturation.

Any of these scenarios must lead to a quick shut-down in 3L application as well.

NPC, TNPC, & ANPC

But it must be made sure that the correct switch-off sequence is maintained: outer IGBT first (T1 or T4), inner IGBT afterwards (T2 or T3) to avoid destruction due to voltage breakdown.
Where thermal overload or a slowly rising current can be monitored with NTC/PTC and current sensors and leave some time for the supervising controller to react in an appropriate time, a desaturation event leaves a maximum of 10µs time for switch-off.
When an outer switch (T1 or T4) desaturates, it may be switched off immediately by the driver. Within 1..3µs the according inner IGBT is to be switched off as well.
It gets more complicated, when the desaturation happens at an inner switch (T2 or T3): when the event is monitored the driver must have the information if an according outer switch is switched on as well or not. If it is switched on the gate driver must switch off the outer IGBT immediately, wait 1..3µs and then switch off the inner IGBT as well. If no outer IGBT is switched on the driver must switch off the inner IGBT immediately. In any case the driver generates an error message so that the controller can shut down the other devices of the converter as well and so establish a secure state.

8. Protection of 3L Devices against Voltage Overshoots

As soon as a current path is interrupted (by switching off an IGBT or a diode) the voltage across the switched off device begins to rise. This voltage overshoot is caused by the energy stored as magnetic field of the current path. The energy increases linearly with rising stray inductance L_S ($E = 0.5*L_S*i^2$); e.g. doubled

parasitic inductance L_S causes doubled energy E. The voltage overshoot ($V = L_S*di/dt$) is added to the DC-link voltage; the sum must not exceed the blocking voltage of the semiconductor as it would be destroyed.

Since a 3L module is larger than a 2L device and a conduction path inherits two switches the current paths are longer and hence the stray inductances higher. Especially the long commutation paths (NPC topology; T2/D5 ⇔ D3/D4 or T3/D6 ⇔ D1/D2) must be paid attention to when the module is designed.
While with a good design low values of the stray inductances can be realised it is very challenging to construct a low inductive 3L setup with standard 2L modules. The long commutation path passes at least three modules in NPC topology (see Figure 33) or two or three modules in TNPC topology (Figure 34) what leads to a stray inductance much larger than that of a dedicated 3L module. Assuming the di/dt is the same this setup produces much higher voltage overshoot.
For that reason, Semikron Danfoss recommends the use of dedicated 3L modules.

If there are no further possibilities to reduce the voltage overshoot at its root cause (i.e. even shorter connections between the semiconductors which at a certain point is not possible anymore) the overshoot needs to be handled in a way protecting the semiconductors.

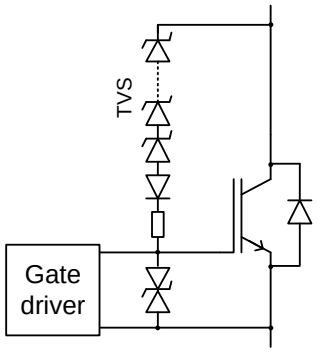
8.1 Snubber

Snubber capacitors can be connected to DC+ and N respectively N and DC-. They must be positioned as close to the module as possible and can be chosen according to the hints given in Semikron Danfoss Application Note AN 07-006 [3].

8.2 Active clamping

Another way to handle harmful voltages is to use an active clamping network at the IGBTs (Figure 37).
This network consists of several in series connected transient voltage suppressor (TVS) diodes providing a breakdown voltage which is slightly below the IGBT's breakdown voltage. The clamping network is connected between collector and gate of the device that shall be protected.
When the switch is turned off and the voltage across increases above the breakdown voltage of the TVS diodes they start conducting a current into the gate of the IGBT. The IGBT starts conducting as well; that leads to a voltage breakdown across the device as soon as the energy stored as magnetic field is exhausted, the TVS diodes go into blocking mode again and the IGBT switches off.
More information can be found in Semikron Danfoss Application Note AN 19-001 [4].

Figure 37: Simple active clamping circuit



9. 3L Loss Calculation

For choosing a 3L module that is best suited for a certain application it is necessary to calculate the power losses that emerge in the different semiconductors. Subsequently the equations for calculating the power losses in 3L NPC and 3L TNPC are shown.

9.1 NPC

The power losses of the ten semiconductors in 3L NPC topology can be calculated according to the following formulas:

T1 & T4

$$P_{cond} = \frac{M\hat{I}}{12\pi} \cdot \{3V_{ce0} \cdot [(\pi - \varphi) \cdot cos(\varphi) + sin(\varphi)] + 2r_{ce}\hat{I} \cdot [1 + cos(\varphi)]^2\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}}\right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}}\right)^{K_V} \cdot \left(\frac{1}{2\pi}[1 + cos(\varphi)]\right) \cdot G_I$$

T2 & T3

$$P_{cond} = \frac{\hat{I}}{12\pi} \cdot \{V_{ce0} \cdot [12 + 3M(\varphi\, cos(\varphi) - sin(\varphi))] + r_{ce}\hat{I} \cdot [3\pi - 2M(1 - cos(\varphi))^2]\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}}\right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}}\right)^{K_V} \cdot \left(\frac{1}{2\pi}[1 - cos(\varphi)]\right) \cdot G_I$$

D5 & D6

$$P_{cond} = \frac{\hat{I}}{12\pi} \cdot \{V_{f0} \cdot [12 + 3M[(2\varphi - \pi)\, cos(\varphi) - 2\, sin(\varphi)]] + r_f\hat{I} \cdot [3\pi - 4M(1 + cos^2(\varphi))]\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}}\right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}}\right)^{K_V} \cdot \left(\frac{1}{2\pi}[1 + cos(\varphi)]\right) \cdot G_I$$

D1 & D4

$$P_{cond} = \frac{M\hat{I}}{12\pi} \cdot \{3V_{f0} \cdot [-\varphi\, cos(\varphi) + sin(\varphi)] + 2r_f\hat{I} \cdot [1 - cos(\varphi)]^2\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}}\right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}}\right)^{K_V} \cdot \left(\frac{1}{2\pi}[1 - cos(\varphi)]\right) \cdot G_I$$

D2 & D3

$$P_{cond} = \frac{M\hat{I}}{12\pi} \cdot \{3V_{f0} \cdot [-\varphi\, cos(\varphi) + sin(\varphi)] + 2r_f\hat{I} \cdot [1 - cos(\varphi)]^2\}$$

$$P_{sw} = 0$$

9.2 TNPC

The power losses of the eight semiconductors in 3L TNPC topology are different from those of 3L NPC and can be calculated as follows:

T1 & T4

$$P_{cond} = \frac{M\hat{I}}{12\pi} \cdot \{3V_{ce0} \cdot [(\pi - \varphi) \cdot cos(\varphi) + sin(\varphi)] + 2r_{ce}\hat{I} \cdot [1 + cos(\varphi)]^2\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}}\right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}}\right)^{K_V} \cdot \left(\frac{1}{2\pi}[1 + cos(\varphi)]\right) \cdot G_I$$

T2 & T3

$$P_{cond} = \frac{\hat{I}}{12\pi} \cdot \{V_{ce0} \cdot [12 + 6M(\varphi\, cos(\varphi) - sin(\varphi)) - 3M\pi\, cos(\varphi)] + r_{ce}\hat{I} \cdot [3\pi - 4M(1 + cos^2(\varphi))]\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}}\right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}}\right)^{K_V} \cdot \left(\frac{1}{2\pi}[1 - cos(\varphi)]\right) \cdot G_I$$

D1 & D4

$$P_{cond} = \frac{M\hat{I}}{12\pi} \cdot \{3V_{f0} \cdot [-\varphi\, cos(\varphi) + sin(\varphi)] + 2r_f\hat{I} \cdot [1 - cos(\varphi)]^2\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}}\right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}}\right)^{K_V} \cdot \left(\frac{1}{2\pi}[1 - cos(\varphi)]\right) \cdot G_I$$

D2 & D3

$$P_{cond} = \frac{\hat{I}}{12\pi} \cdot \{V_{f0} \cdot [12 + 3M(2\varphi\, cos(\varphi) - 2\, sin(\varphi)) - 3M\pi\, cos(\varphi)] + r_f\hat{I} \cdot [3\pi - 4M(1 + cos^2(\varphi))]\}$$

$$P_{sw} = f_{sw} \cdot E_{sw} \cdot \left(\frac{\hat{I}}{I_{ref}}\right)^{K_I} \cdot \left(\frac{V_{CC}}{V_{ref}}\right)^{K_V} \cdot \left(\frac{1}{2\pi}[1 + cos(\varphi)]\right) \cdot G_I$$

9.3 ANPC

See chapter 10.

9.4 NPC, TNPC, & ANPC

The equations are valid for M = 0…1. The modulation index M correlates DC-link voltage and RMS voltage:

$$M = \frac{\sqrt{2} \cdot V_{RMS}}{\sqrt{3} \cdot {}^{V_{DC}}/_{2}}$$

Typical values for K_V, K_I and G_I for Semikron Danfoss modules are shown in Table 1.

Table 1: Typical K_V, K_I and G_I values for Semikron Danfoss modules

Technology	**Si**		**SiC**	
Letter symbol	IGBT	Diode	MOSFET	Body Diode
K_V	1.4	0.6	1 … 1.4	0.6
K_I	1	0.6	1	0.6
G_I	1	1.15	1	1.15

10. SemiSel

SemiSel is Semikron Danfoss' online simulation tool to calculate losses and temperatures of power semiconductors in customer specific applications.
From specific values for cooling (e.g. type and performance of the heatsink, ambient temperature) and electric parameters (e.g. input/output voltage, switching frequency, load current, etc.) SemiSel calculates the power losses and junction temperatures of all IGBTs and diodes within a few seconds. By changing certain parameters the optimum setup (which type of module, switching frequency,…) can easily be found.
The latest version of SemiSel has been extended to calculate all 3L topologies mentioned in this document in the same convenient way as 2L designs.

Symbols and Terms

Letter Symbol	Term
2L	Two level
3L	Three level
CD	Clamping Diode
cos φ	Power factor
CS1	Collector Sense of IGBT 1
DC+	Positive potential (terminal) of a direct voltage source
DC-	Negative potential (terminal) of a direct voltage source
di/dt	Rate of rise and fall of current
E	Electrical energy
E_{SW}	Sum of energy dissipation during turn-on and turn-off-time
f_{SW}	Switching frequency
FWD	Free Wheeling Diode
GA	Single Switch
GAL	Chopper, low IGBT
GAR	Chopper, high IGBT
GB	Half-bridge
G_I	Adaptation factor for the non-linear semiconductor characteristics
GM	Half-bridge with anti-serial switches (IGBT and antiparallel diode)
i	Time dependant value of current
$\hat{I}$	Peak value of current
$I_{C,NOM}$	Nominal collector current
IGBT	Insulated Gate Bipolar Transistor
I_{peak}	Peak value of current
I_{ref}	Reference current value of the switching loss measurement
I_{RMS}	AC terminal current
φ	Conduction angle
K_I	Exponent for the current dependency of switching losses
K_V	Exponent for the voltage dependency of switching losses
L_S	Parasitic inductance / stray inductance
M	Modulation index
N	Neutral potential (terminal) of a direct voltage source; midpoint between DC+ and DC-

NPC	Neutral Point Clamped
NTC	Temperature sensor with negative temperature coefficient
P	Active power
P_{cond}	Conduction power losses
P_{SW}	Switching power losses
PTC	Temperature sensor with positive temperature coefficient
Q	Reactive power
r_{CE}	On-state slope resistance (IGBT)
r_f	On-state slope resistance (diode)
RMS	Root Mean Square
R_{th}	Thermal resistance
S	Apparent power
t	Time
THD	Total Harmonic Distortion
T_J	Junction temperature
TNPC	T-type Neutral Point Clamped
TVS	Transient voltage suppressor diode
V	Voltage
V_{CC}	Collector-emitter supply voltage
V_{CE}	Collector-emitter voltage
V_{ce0}	Forward threshold voltage (IGBT)
V_{f0}	Collector-emitter threshold voltage (diode)
V_{CEsat}	Collector-emitter saturation voltage
V_{DC}	Total supply voltage (DC+ to DC-)
V_{ref}	Reference voltage value of the switching loss measurement
V_{RMS}	AC terminal voltage

A detailed explanation of the terms and symbols can be found in the "Application Manual Power Semiconductors" [2].

References

[1] www.semikron-danfoss.com
[2] A. Wintrich, U. Nicolai, W. Tursky, T. Reimann, "Application Manual Power Semiconductors", 2nd edition, ISLE Verlag 2015, ISBN 978-3-938843-83-3
[3] J. Lamp, "IGBT Peak Voltage Measurement and Snubber Capacitor Specification", Application Note AN 07-006 – rev01, Semikron Danfoss, www.semikron-danfoss.com
[4] J. Lamp, "Gate Driver Configuration and Short Circuit Protection for 3-Level Topologies", Application Note AN 19-001 – rev01, Semikron Danfoss, www.semikron-danfoss.com

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