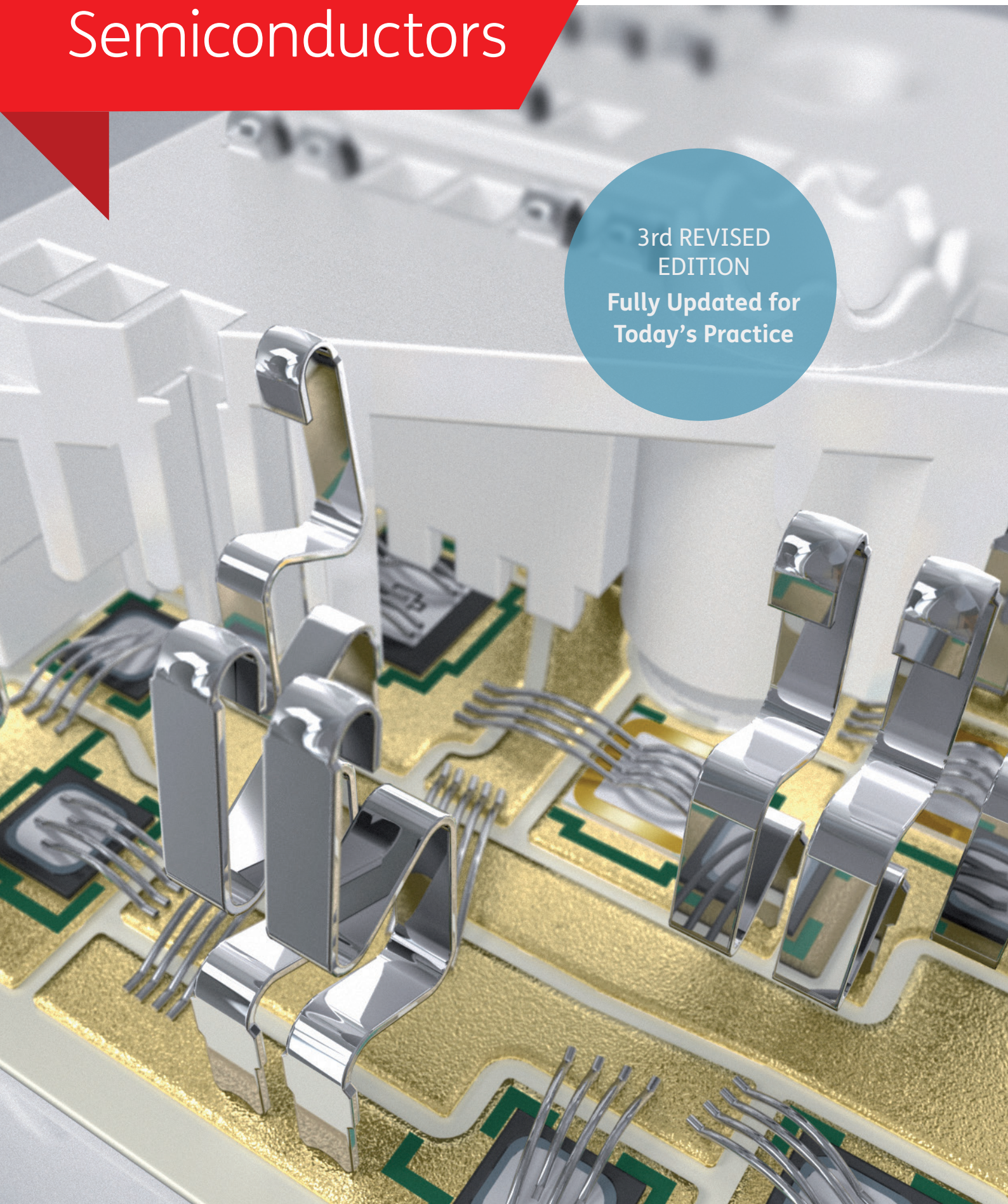
APPLICATION MANUAL

Power Semiconductors

SEMIKRON DANFOSS



3rd REVISED EDITION

Fully Updated for Today's Practice



APPLICATION MANUAL

Power Semiconductors

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Published by
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3rd revised edition
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Edited by: Semikron Danfoss International,
Sigmundstrasse 200, D-90431 Nuremberg, Germany

Printed in Germany

Preface

This is the 3rd edition of our "Application Handbook Power Semiconductors".
Since 2015, when the last edition was published, the world of power electronics has once again developed rapidly - on the one hand due to ever new areas of application and increasing demands on all components and on the other hand due to enormous progress in manufacturing technologies and new materials for power semiconductors and the assembly and connection technologies in power modules. These aspects and also the possibilities offered by circuit topologies that were rarely used in the past in connection with today's power semiconductors are dealt with in more detail in this issue than before. Power modules with silicon carbide MOSFET have been included for the first time, well aware of the present development dynamics of their properties.

The general development trends (space requirements, costs, energy efficiency) and the expansion of the application fields result in ever increasing demands on the reliability and robustness of power semiconductors. The consequences - both for the design and for test procedures - are described with reference to the latest research results.

The book is primarily aimed at users and is intended to summarize experiences that have so far only been presented in a large number of individual articles. In the interest of a manageable scope, theoretical principles are only briefly outlined where this seems absolutely necessary for understanding. A large number of excellent academic textbooks are available today for further in-depth study, some of which are listed in the list of sources.

Based on the properties of the most important power semiconductors, information is given on how to use the data sheets and application notes, e.g. on cooling, power layout, control, protection, parallel and series connection; supplemented by notes on the utilisation of IGBT and MOSFET in 3-level topologies.

This book uses contributions from the authors of earlier editions of the application handbook Prof. Dr.-Ing. Josef Lutz and Prof. Dr.-Ing. habil. Jürgen Petzoldt (ed. 1998), Dr. techn. Werner Tursky and Prof. Dr.-Ing. Tobias Reimann (ed. 2010/2015), whose authorship is not cited again in the text. Special thanks to Prof. Reimann for the revision of chapter 1.1 and Dr. Uwe Schilling for his contribution to the cosmic ray topic in chapter 4 of this edition. We would also like to take this opportunity to thank Joachim Lamp, Rainer Weiss and Martin Roeblitz for their selfless and professional support with measurements and during technical discussions.

We hope that you find this book interesting and useful. Critical comments are always welcome.
If this book makes your component selection and design-in work easier, our expectations will be fulfilled.

The authors dedicate this book to Werner Tursky, our deceased former co-author and valued colleague. We would like to thank Werner for always patiently and kindly sharing his knowledge and experience and will always honour his memory.

Nuremberg in February 2025

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1 Power Electronic Switches

1.1 Switches in power electronic circuits

1.1.1 Basics of commutation

With the exception of a few special applications (such as quasi-stationary linear operation), power semiconductors operate in switching mode. Basic types of switching operations can be derived depending on the specific circuit environment. These in turn differ in the specific time characteristics of switch current and switch voltage on the one hand and the resulting losses in the switch on the other hand.
The goal of every current and further development as well as application of power semiconductors is to approximate an ideal, i.e. loss-free switch behaviour in all static (on-state, off-state) and dynamic (turn-on, turn-off) operating conditions while minimizing the power required to control and monitor the switch.
The control of the electrical power transmitted by a power converter and thus the energetic coupling between generation and consumption is realized by periodic switching of the power electronic switches. Power converters are therefore electronic networks with currents or voltages applied on their external terminals, which can have additional internal energy storage devices (L, C). The electronic networks can be more or less complex in terms of the type and number of switches used or required.
Due to the currents or voltages applied on the external terminals of the power electronic network, it must be ensured that when a current-carrying switch is turned-off, the impressed current has to be taken over by another switch that is turned-on. Similarly, when a voltage carrying switch is turned-on, the impressed voltage must be taken over by another switch that turned-off.
The dynamic interaction of both switches in the course of the mutual transfer of current and voltage is called commutation. Almost all topologies in power electronics circuit works on the principle of commutation. The so-called commutation cell is the smallest, internal functional unit of a power converter. From the analysis the commutation cell it is possible to derive all operating modes of power electronic switches and circuit topologies. Converter circuits can consist of one (e.g. buck converter) or several (e.g. three-phase voltage inverter) commutation cells. Only by a detailed understanding of the switching and commutation processes a systematic access to power electronic circuit technology in theory and practice is possible. Figure 1.1.1 shows the most general representation of a commutation cell. It represents the basic principle of the complete power electronic circuit topologies (DCDC, ACAC, DCAC, ACDC).

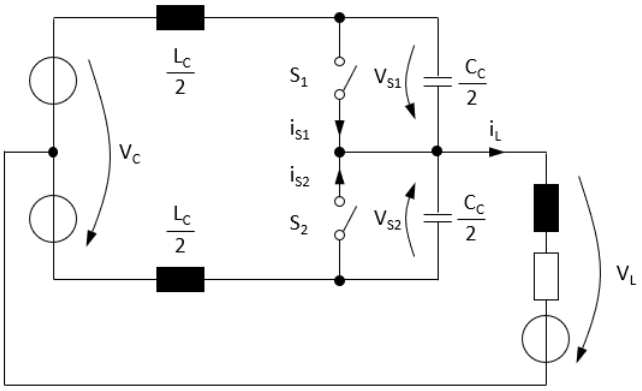


Figure 1.1.1 Principle circuit drawing of a commutation cell

v_C: applied commutation voltage (alternating or direct voltage)
i_L: feed in commutation current /load current (alternating or direct current)
L_C: represents all existing inductive components in the commutation cell; in series to the switches it can be summed up to: $L_C=L_C/2+L_C/2$
C_C: represents all in the commutation loop existing capacitive components; in parallel to the switches it can be summed up to: $C_C=C_C/2+C_C/2$
S_1, S_2: power electronic switches (commutation partners) simplified as ordinary switches
i_{S1}, v_{S1}: current and voltage of switch 1 in positive defined polarity
i_{S2}, v_{S2}: current and voltage of switch 2 in positive defined polarity

In the following, typical switching and commutation processes of power electronic switches are discussed and the influence of the elements L_C and C_C on the switching curves and switching losses of S_1 and S_2 is shown. In order to make understanding more easy, the general representation of the commutation cell is first transformed into the well-known buck converter circuit (step down converter, DCDC), which represents precisely one commutation cell (Figure 1.1.2).

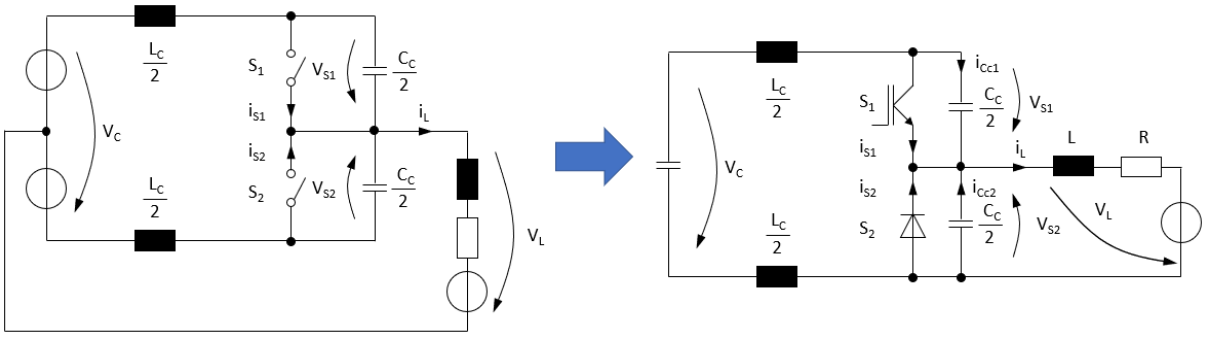


Figure 1.1.2 Transformation of a principle commutation cell to buck converter (DCDC converter)

For the explanation of the switching and commutation procedures following simplifications are assumed:

v_C: applied constant voltage
i_L: flowing constant current
$i_{S1}(t)$, $v_{S1}(t)$: idealised, linear time function of current and voltage at the transistor
$i_{S2}(t)$, $v_{S2}(t)$: idealised, linear time function of current and voltage at the freewheeling diode
ideal conduction behaviour of transistor and freewheeling diode

Case 1 L_C=0; C_C=0 (theoretical case)

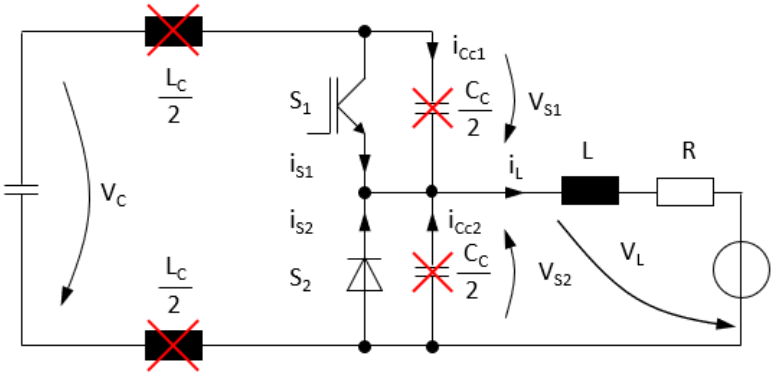


Figure 1.1.3 Commutation cell of case 1

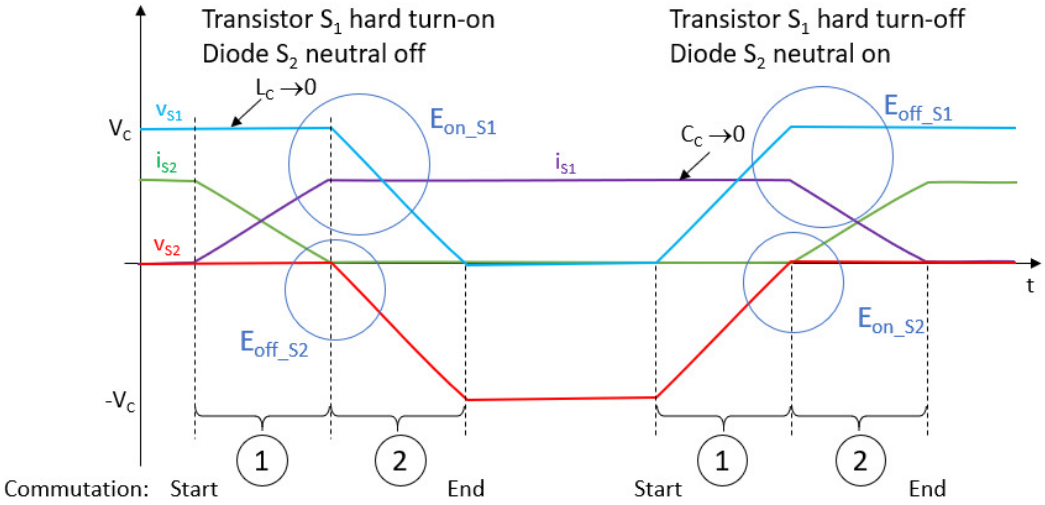


Figure 1.1.4 Current and voltage commutation (wave forms) of case 1

The sequences of the voltages across and currents through the switches are determined by the natural switching behaviour of the diode. The left part of Figure 1.1.4 shows the commutation from the diode to the transistor. It begins with the turn-on command for the transistor S_1. First, the currents must commute ① because the diode S_2 can only take over voltage ②, when its current has become zero. As a result, the transistor must be switched on hard with a high turn-on energy E_{on}. The instantaneous peak power for the transistor is $v_C \cdot i_L$. The diode, on the other hand, turns-off neutrally. With an ideal diode, this means that no switching energy E_{off} is dissipated.
The right-hand part of Figure 1.1.4 shows the commutation from the transistor to the diode. It begins with the turn-off command for transistor S_1. First, the voltages must commutate ①, as the diode S_2 can only accept current ②, when its voltage has become zero. This results in a mandatory hard turn-off for the transistor with high switch-off energy E_{off}. The instantaneous peak power for the transistor is again $v_C \cdot i_L$.
In contrast, the diode turns on neutrally. With an ideal diode, this means that no switching energy E_{on} is dissipated.

Case 2 L_C>0; C_C=0 (theoretical case)

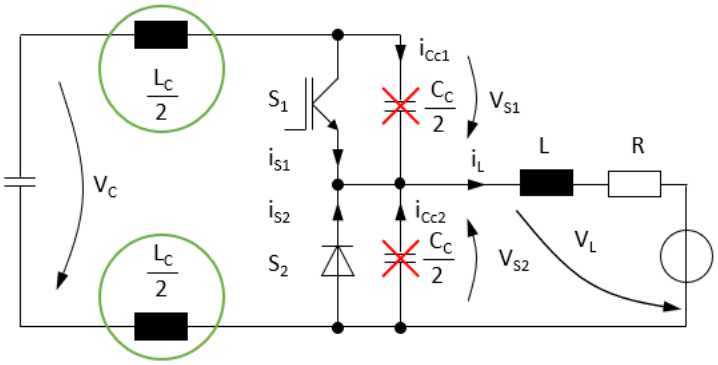


Figure 1.1.5 Commutation cell of case 2

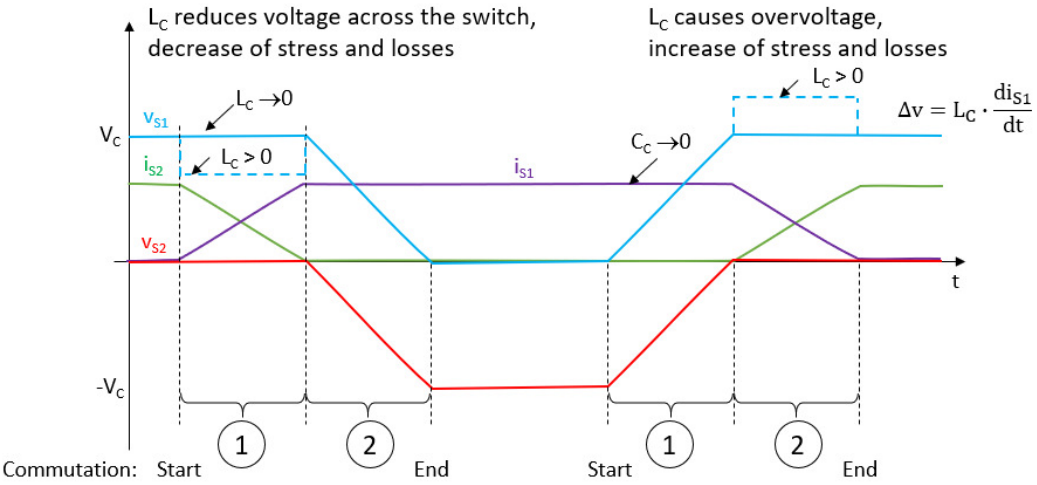


Figure 1.1.6 Current and voltage commutation for case 2

Figure 1.1.6 shows the switching and commutation processes according to case 2. An effect of the total inductance L_C on the switch S_1 can always be measured during current commutation, since the change in current over time induces a voltage across the inductance:

$$\Delta v = L_C \cdot \frac{di_{S1}}{dt}$$

When the transistor S_1 is switched on, due to the increasing current i_{S1}, the voltage v_{Lc} is directed in such a way that it reduces the voltage v_{S1} ①. In this case one speaks of a relieved or soft switch-on process. In comparison to case 1, both the instantaneous peak power loss and the switch-on loss energy E_{on} decrease for the transistor. In certain power electronic circuit topologies (e.g. parallel resonant converter or quasi-resonant converter) this effect is deliberately exploited and the value for L_C is increased. This usually has the inevitable consequence that the transistor must be switched off without current or with little current (ZCS – zero current switching @ turn-off).

When the transistor S_1 is switched off, due to the falling current i_{S1}, the voltage v_{Lc} is directed in such a way that it increases the voltage v_{S1} (② switching overvoltage). In this case one speaks of an hard switch-off process. In comparison to case 1, both the instantaneous peak power loss and the switch-off loss energy E_{off} increase for the transistor.
The maximum allowed values for the transient overvoltage on the switch is determined by the blocking voltage of the power semiconductor components (e.g. 650V, 1200V or 1700V). This must not be exceeded in order to prevent the power semiconductors from being destroyed. The effective total inductance L_C in the commutation cell is made up of the following components, among others together:

- parasitic series inductances (ESL) of the DC-link capacitors
- inductance of the electrical connections in the commutation cell (wiring, bus bar)
- package internal inductances of the power semiconductor components
- stray inductances of transformers in the commutation cell (e.g. flyback converter)

The developer's task when designing commutation cells with current-carrying switch-off processes is to carefully minimize all components of the overall inductance L_C. If the achieved L_C is still too high taking into account all technical and commercial criteria, the following measures can be taken:

- Selecting a higher blocking voltage rating (at the expense of higher switch losses)
- addition of snubber circuits (at the expense of increased circuit complexity)
- slower turn-off means di/dt reduction (at the expense of higher turn-off losses)
- Changing the circuit concept of the power converter circuit or the operating mode of the power electronic switches (e.g. ZCS)

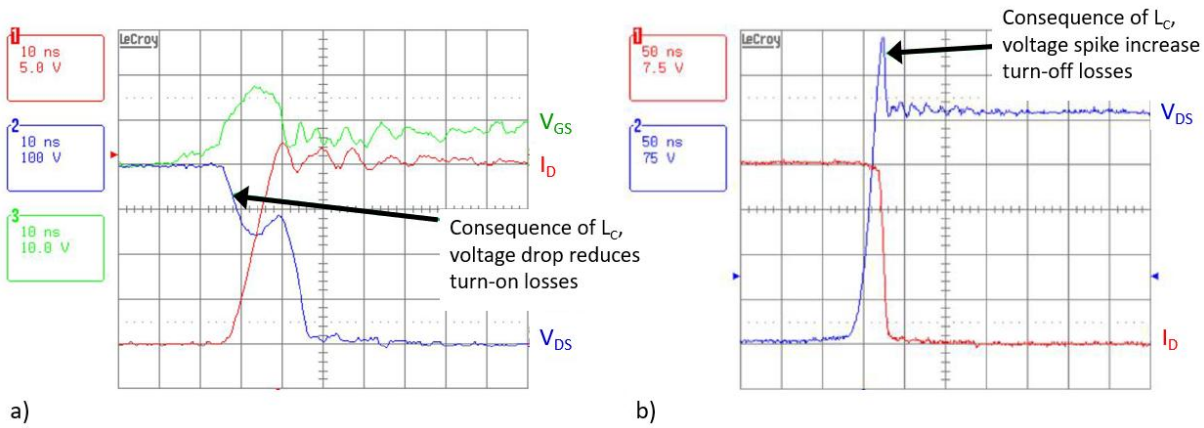


Figure 1.1.7 Influence of the commutation inductance L_C on switching behaviour of a power transistor a) reduced stress, peak power and switching energy during turn-on; b) increased stress peak power and switching energy during turn-off

If the freewheeling diode S_2 is considered as an ideal component in the circuit of the buck converter (Figure 1.1.5), the inductance L_C has no influence on its switching curves or switching behaviour. In real bipolar diodes, however, a switching overvoltage caused by L_C can be observed during reverse recovery current.

Case 3 L_C=0; C_C>0 (theoretical case)

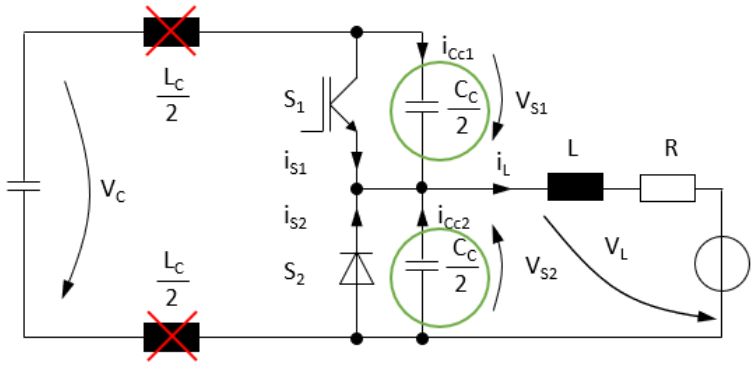


Figure 1.1.8 Commutation cell of case 3

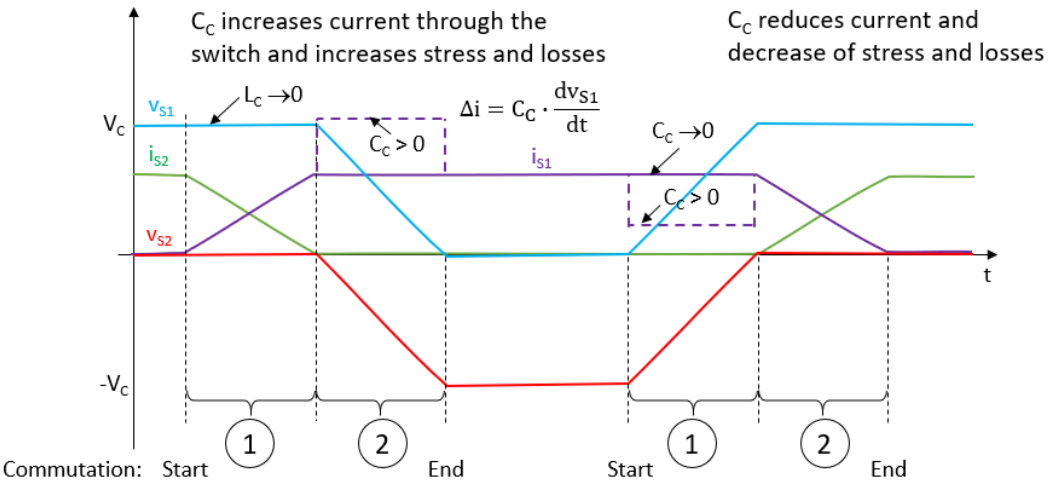


Figure 1.1.9 Current and voltage commutation for case 3

An effect of the total capacitance C_C on the switch S_1 (transistor) can always be measured during voltage commutation, since the change in voltage over time causes a current to flow through the capacitance C_C, which increases or reduces the transistor current:

$$i_{C_C} = C_C \cdot \frac{dv_{S1}}{dt}$$

When the transistor S_1 is switched on, due to the falling voltage v_{S1}, the current i_{Cc} is directed in such a way that it increases the current i_{S1} by the amount of i_{Cc} (② dynamic overcurrent). In this case one speaks of a hard turn-on. In comparison to case 1, both the instantaneous peak power and the turn-on energy E_{on} increase for the transistor.
The maximum permitted value for the transient overcurrent of the switch is specified by the repetitive pulse current limit of the power semiconductor (e.g. I_{CRM}). This must not be exceeded in order to prevent the power semiconductors from being damaged.
When the transistor S_1 is switched off, the current i_{Cc} is directed in such a way that it reduces the current i_{S1} due to the increasing voltage v_{S1} (①). In this case one speaks of a relieved or soft switch-off process. In comparison to case 1, both the instantaneous peak power and the turn-off energy E_{off} decrease for the transistor.
In certain power electronic circuit topologies (e.g. series resonant converter or quasi-resonant converter) this effect is deliberately exploited and the value for C_C is increased. This usually means that the transistor must be turned on without voltage or with low voltage (ZVS – zero voltage switching @ turn-on).
The effective total capacitance C_C in the commutation cell is composed, among other things, of the following components:

- intrinsic capacitances of the power semiconductor components (chip capacitances, Q_{rr}, C_{oss}, C_{out})
- load capacitances connected in parallel to the switches
- other (parasitic) capacitances that are pronounced from the centre of the switch pair against v_{C+}, v_{C-} or ground potential and are (virtually) connected in parallel to the switches

The developer's task when designing voltage commutation cells is to carefully minimize all components of the total capacitance C_C, for example through appropriate component selection and construction. In contrast to influencing L_C, the system designer has significantly less influence on the size of the capacitance C_C.
One possibility might be to select the power semiconductor component according to its voltage-dependent C_{oss} characteristic (e.g. Si Super Junction MOSFET vs. SiC MOSFET) and/or diodes with low recovery charge Q_{rr} (Schottky diodes). The design of inductive components (transformers, chokes) with minimal parasitic winding and coupling capacitances can also make a contribution.
If the achieved C_{Cmin} is still too high with regard to the transient overcurrent, even taking all technical and commercial criteria into account, the following measures can be taken:

- slower turn-on or dv/dt reduction (at the expense of higher turn-on losses)
- usage of power electronic components with higher pulse current capability
- changing the circuit concept of the power converter or the operating mode of the power electronic switches (e.g. ZVS)

Figure 1.1.10 shows the influence of the capacitance C_C of the commutation cell when switching a power transistor on and off, measured in the laboratory.

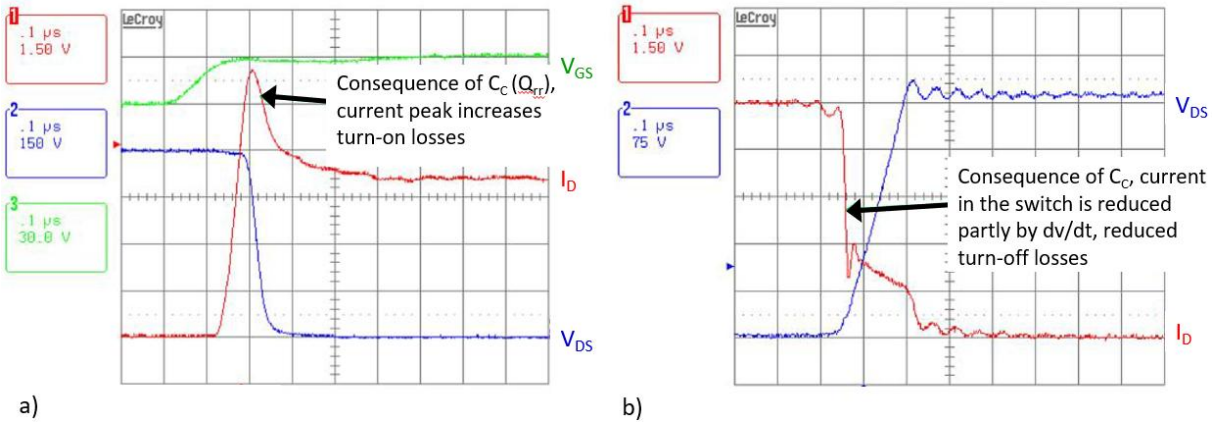


Figure 1.1.10 Influence of C_C on switching behaviour of a power transistor a) increased stress, peak power and switching energy during turn-on caused by an additional current peak; b) reduced stress, peak power and switching energy during turn-off

If the freewheeling diode S_2 is considered as an ideal component in the buck converter (Figure 1.1.2), then the capacitance C_C has no influence on its switching curves or switching behaviour. The following idealised curves in Figure 1.1.11 can be used to summarize cases 1-3 (switching path) for switching the switch S_1 (transistor of the buck converter) and the switch S_2 (freewheeling diode of the buck converter), taking into account the influence of L_C and C_C:

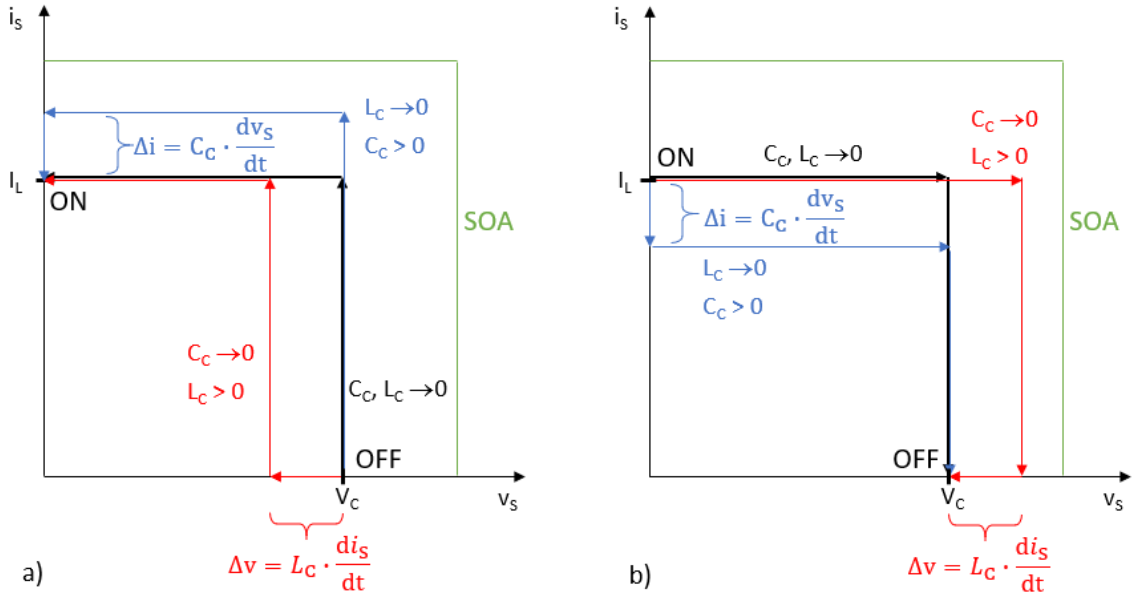


Figure 1.1.11 Idealised voltage and current transients during commutation; black: case 1, red: case 2, blue: case 3; for a) turn-on and b) turn-off; the area under the curves indicate a ratio for the turn-on and -off losses

Case 4 L_C>0; C_C>0 (real case)

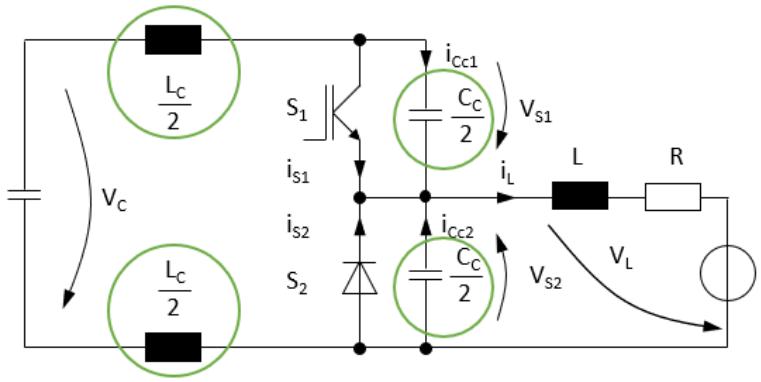


Figure 1.1.12 Commutation cell of case 4

In real commutation circuits, both C_C and L_C are always greater than zero. The smallest possible values can be referred to as C_{Cmin} and L_{Cmin}. Especially in hard-switching, PWM-controlled circuits, these minimum values are aimed for by the design of the converter. The simultaneous presence of C_C and L_C initially leads to the overlapping of the individual effects described in cases 1-3 during the switching and commutation processes. The overall effective C_C and L_C are made up of several individual components of different sizes, which form resonant circuits with different resonance frequencies. These resonance circuits can be excited to oscillate with every switching process. The steeper the switching and commutation edges are, the larger the frequency range of the excited oscillations that are superimposed on the switching curves. Figure 1.1.13 shows this effect using the example of a measured turn-off process of a fast Si MOSFET.

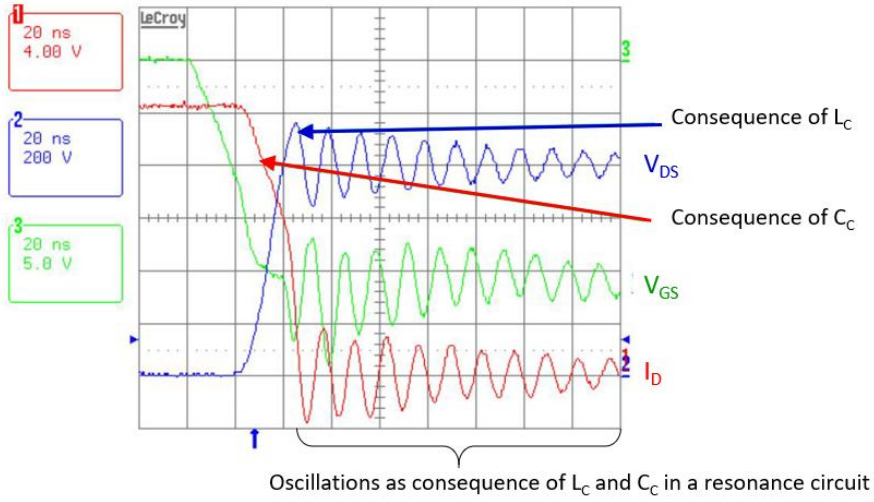


Figure 1.1.13 Turn-off of a fast MOSFET with high frequency oscillations

The oscillations shown cause losses on the one hand and electromagnetic interferences on the other. In general it can be said that the result of the design of a commutation cell is always a compromise between electrical, thermal and electromagnetic behaviour.

1.1.2 Basic types of switching processes

As a result of the analysis of the commutation processes in the previous section, Figure 1.1.14 below summarizes the basic types of switching processes.

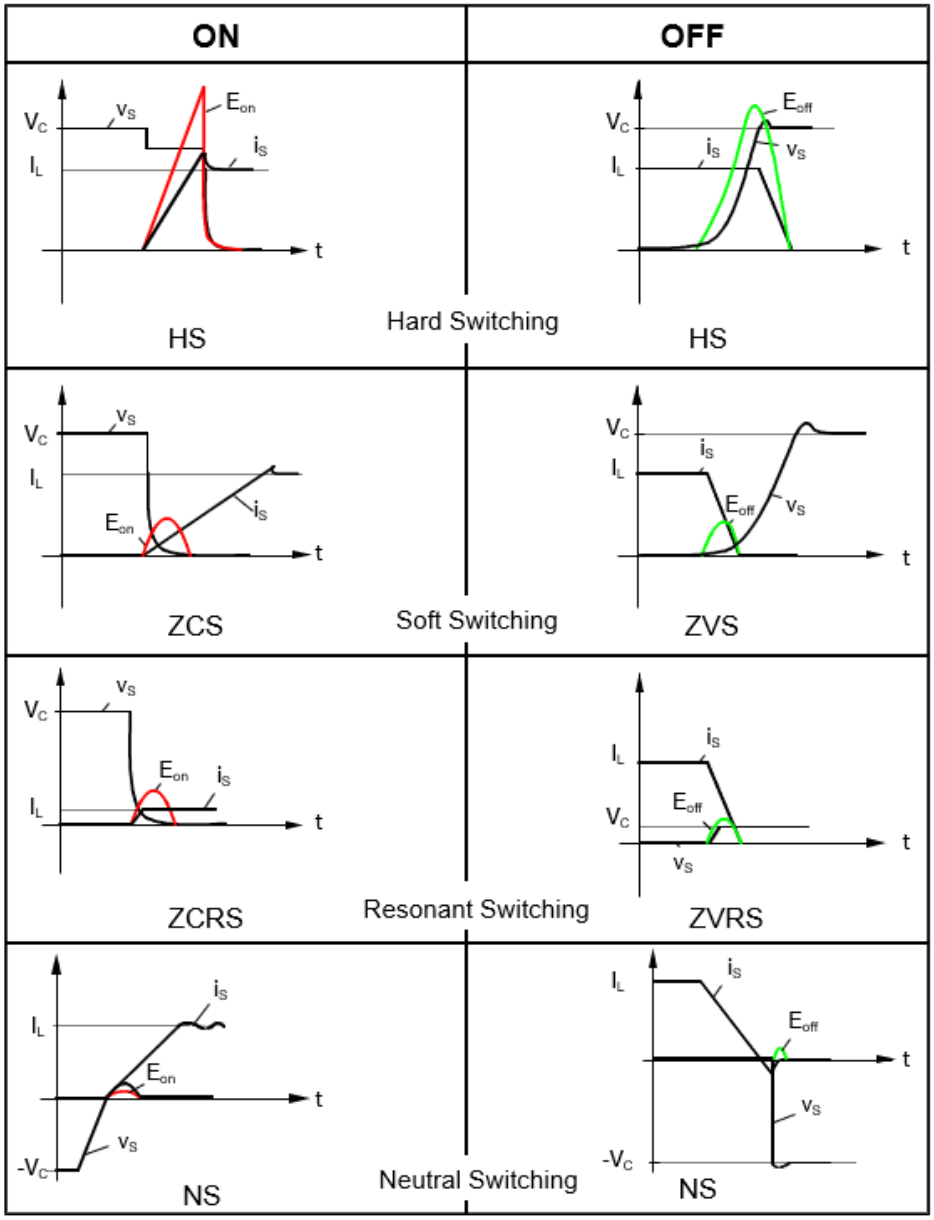


Figure 1.1.14 Types of switching processes (V_C= driving commutation voltage, I_L=load current to be commutated)

1.2 Applications and limits of power semiconductors

The development of power semiconductors saw the onset of lasting success for power electronics across all fields of electrical engineering. This old statement is true also in the 2020th because even artificial intelligence needs a power supply. Given the ever increasing call for resource conservation (e.g. energy saving agenda), the use of renewable energies and energy storage (e.g. wind power, photovoltaics) and the need for alternatives to fossil fuels (e.g. electric and hybrid vehicles, battery charging), this success is gaining more and more momentum today.
This development is also largely driven by the interactions between system costs and market penetration, as well as the energy consumption required for production and the energy saving potential of products in operation. In addition to the general aim to expand the performance profile, the development aims "low materials consumption / low costs" and "high efficiency" are important as already described in the last edition 10years ago.
Figure 1.2.1 shows maximum current and voltage values for controllable power semiconductors on the market today. Here has the availability of wide bandgap material lead to some changes in the last decade. High voltage Si MOSFET (**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor) have become a niche product just like GTO (**G**ate **T**urn **O**ff-) thyristors (and IGCT - **I**ntegrated **G**ate **C**ommutated **T**hyristor).

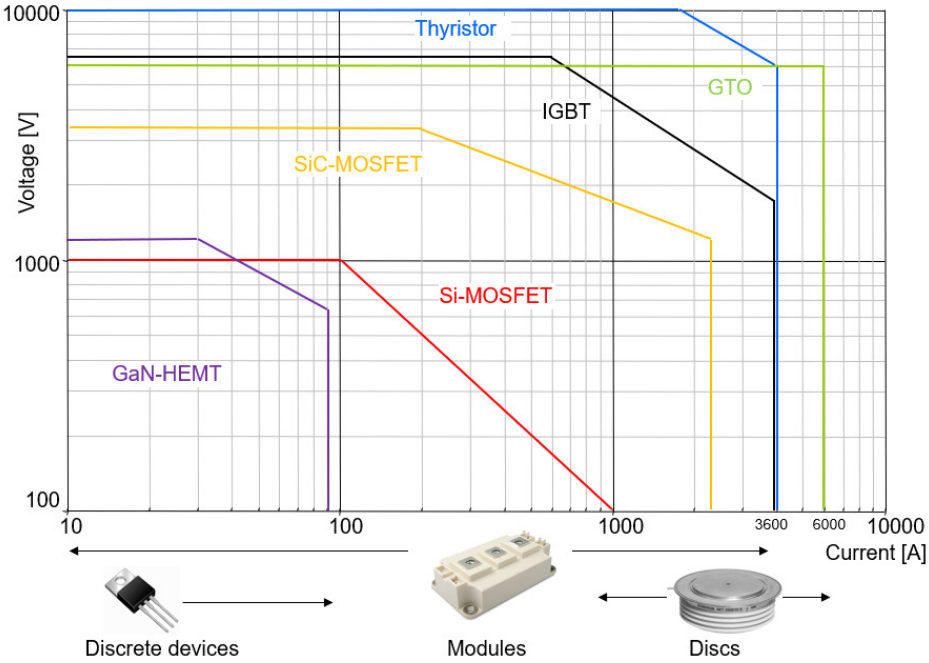


Figure 1.2.1 Present current and voltage limits for controllable power semiconductors

Today, the use of parallel and series connections for power semiconductors, as well as power converters equipped with semiconductors, means that virtually any amount of electric power can be transformed (e.g. up to GW range in HVDC transmission), converted into another form of energy or "generated" from another type of energy. The thyristors are single-chip devices, whereby the most powerful IGBT (**I**nsulated **G**ate **B**ipolar **T**ransistors) chips today are 300 A. Higher current ratings are realised by paralleling in modules. Today, most applications for currents of some 10 A use power semiconductors with chips integrated in potential-free power modules. In 1975, it was SEMIKRON who launched them commercially for the first time. These modules contain several chips of identical or different functionality (e.g. IGBT and freewheeling diode, thyristor, line rectifier diode) and additional components (e.g. temperature and current sensors) and even control and protective circuits ("intelligent power modules"/IPM), if required. The reason that modules are popular is that, apart from easy assembly, they boast "integrated", well-proven electrical isolation between chip and heat sink, almost any combination of different components and circuitry in one module to relatively low costs thanks to batch production.
Figure 1.2.2 shows common switching frequency and power range for various power semiconductors. IGBT are still the work horses and important for the "mass markets" of mains-powered systems in the range of some kW up to several MW. This is particularly true for potential-free power modules. IGBT modules are cost-effective and matured solutions and the preferred component in many markets, such as drives, wind energy and today also for electric vehicles.

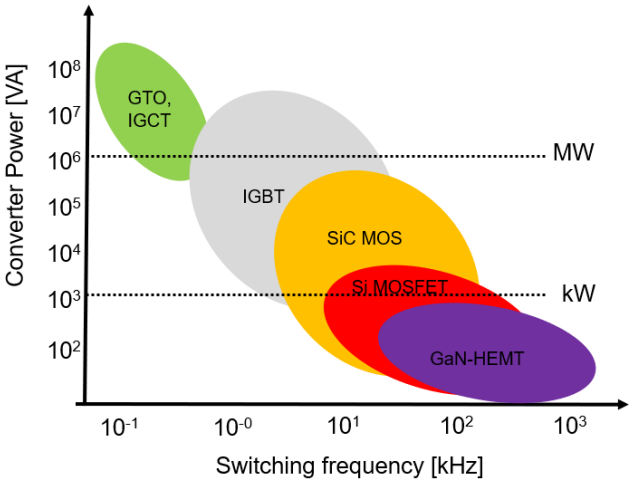


Figure 1.2.2 Switching frequency and power ranges for the most important switched power semiconductors

Silicon-MOSFET in the lower power segment and GTO thyristors and IGCT in the high power segment are pushed back. Actively switched thyristors might even disappear in the next years because IGBT in combination with intelligent circuit topologies like multi cell converter (MCC) can take over the functionality. Si MOSFET are used billions of times but more or less only in low voltage applications (DCDC power supply, automotive) as discrete devices or integrated in power IC. For higher voltages above 200V SiC based MOSFET have taken over the market because of a lower $R_{DS(on)}$·mm² and the now decreasing costs and the increasing availability of these devices. The latter is the reason why SiC MOSFET is taking over more and more market share from IGBT, because we are now in a situation where the higher efficiency pays off the initial additional costs in a short time. The resistive characteristics of a unipolar MOSFET can be an advantage even if the better switching performance compared to a bipolar IGBT is not as important. This is particularly true for applications with predominantly partial load operation, such as in electric vehicles.
HEMT (**H**igh **E**lectron **M**obility **T**ransistor) also using wide bandgap materials such as gallium nitride (GaN) or gallium arsenide (GaAs) are almost ideal switches with almost no conduction and switching losses. Today these are the only power semiconductor build as lateral devices, which requires two topside contacts for the main current. They are therefore limited to a lower power range (20…30A) compared to SiC MOSFET and IGBT and with some exceptions to voltages of <700V. The high electron mobility allows switching frequencies up to the MHz range. They are the preferred solution for power supply connected to 110V… 230V mains in discrete solutions and up to now not in the focus of module manufacturer.
The general aims and directions for the further development of power semiconductors and modules can be summarised as follows:

- Cost reduction
- Reducing losses in the semiconductors as well as in control circuits
- Expanding the operating temperature range for peak loads (<= 200°C)
- Improving the switching performance (switching losses, dv/dt control)
- Increasing power density (A/mm²)
- Improved service life, ruggedness and reliability
- Reducing the effort for control and protection

The development directions can be broken down to the field of:

Semiconductor

- Widespread use of new semiconductor materials (e.g. wide bandgap materials)
- Higher permissible chip temperatures or current densities (reduction of chip area)
- Finer structures (cell pitch, reduction of chip area)
- New structures (improvement of chip characteristics)
- Integration of functions on the chip (e.g. gate resistance, temperature and current measurement)
- New monolithic components by combining functions (RC-IGBT, RB-IGBT)
- Improved stability of chip characteristics under different operating and climatic conditions (moisture, sulphur,…)

Packaging

- Increase in thermal and power cycling capability (sintering, welding)
- Improvement of heat dissipation, thermal resistance (isolation substrate, integrated heat sink)
- Wider scope of application with regards to climatic conditions (improvements in casing and potting materials or new packaging concepts)
- Optimisation of internal connections and connection layouts (parasitic elements)
- User-friendly package optimisation to simplify converter construction
- Reduction of packaging costs
- environmental compatibility in production, operation and recycling (ROHS and REACH compatibility)

More complex technologies, smaller semiconductor structures and precise process control are inevitably driving the properties of modern power semiconductors towards the physical limits of silicon. For this reason, research into alternative semiconductor materials, which began as early as the 1950s, was pushed in recent years and has since resulted now in mass products of wide bandgap semiconductors (WBG). These materials display a far higher energetic gap between valence and conduction band, resulting in comparatively lower forward on-state losses and switching losses, higher permissible chip temperatures, and better heat conductivity than silicon.

Table 1.2.1 contains quantitative data on the key material parameters, Figure 1.2.3 shows the impact they have on material properties.

Parameters	Symbol	Unit	Si	4H-SiC	GaN
Bandgap energy	E_g	eV	1.12	3.26	3.39
Intrinsic density	n_i	cm^{-3}	$1.4 \cdot 10^{-10}$	$8.2 \cdot 10^{-9}$	$1.9 \cdot 10^{-10}$
Breakdown field intensity	E_c	MV/cm	0.23	2.2	3.3
Electron mobility	μ_n	cm^2/Vs	1400	950	1500
Drift velocity	n_{sat}	cm/s	10^7	$2.7 \cdot 10^7$	$2.5 \cdot 10^7$
Dielectric constant	e_r	-	11.8	9.7	9.0
Heat conductivity	λ	W/(cm·K)	1.5	3.8	1.3

Table 1.2.1 Wide band-gap semiconductor materials versus silicon: a comparison of material properties [1.1]

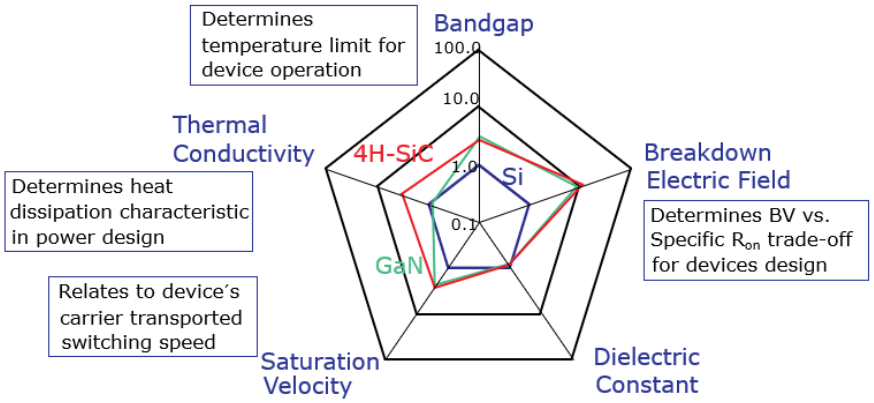


Figure 1.2.3 Impact of different physical parameters of semiconductor materials [1.2]

Today, the key to more widespread use of SiC, however, is to enable the cost-efficient production of suitable monocrystalline chips that are sufficiently high in quality to eliminate crystal degradation (micropipes), and that are available in optimum wafer sizes for the power electronics industry. Especially for SiC the cost for the raw material will always be higher because of much higher energy consumption and much longer processing time.
While Si is currently produced on 12" wafers virtually defect-free SiC wafers with a diameter of 8" are in development and have still a much lower yield compared to Silicon. Further developments of the WBG semiconductor material with regards to reliability, long term stability and reduction of parameter spread are still necessary. On the other hand the power density with SiC devices is factor 2 … 3 higher (W/mm²) which overcomes the disadvantage of the higher production costs on wafer level. System designers consider the overall cost of the system, where lower cooling requirements and smaller passive components can lead to a reduction in system cost. End user looking on the total cost during service life and are willing to pay a higher price if the energy saving pay off for that in the first few years.
In order to fully exploit the significant advantages of WBG power semiconductors compared to conventional components, it is essential to further develop and improve the packaging accordingly such as:

- low conduction and switching losses allow higher current ratings and require lower lead resistance
- higher possible power densities require improved heat spreading and cooling
- higher permissible operating temperatures require package materials which can scope with it and leads to increased power cycle requirements
- shorter switching times, higher switching frequencies require lower stray inductances.

1.3 References

[1.1] N. Kaminski, "State of the Art and the Future of Wide Band-Gap Devices", EPE Conference Proceedings, 2009
[1.2] G. Majumdar, T. Oomori, "Some key researches on SiC device technologies and their predicted advantages", EPE Conference Proceedings, 2009

2 Basics of Power Semiconductors

2.1 Diodes for mains applications

2.1.1 Structure and functional principle

Diodes for mains applications (hereinafter also referred to as rectifier diodes) are used in large numbers in line-commutated converters due to their robustness, low forward losses and comparatively low cost. Today, diodes for mains applications are produced mainly based on monocrystalline silicon. The rectifying effect is caused by the transition of mobile charge carriers from an n-doped to a p-doped area in the semiconductor chip (pn-diodes).
To enable the high reverse voltages required in most power electronics applications, diodes for power electronics have a "pin" junction structure. The junction consists of a heavily p-doped p^+ layer with many freely moving holes, a heavily n-doped n^+ layer with many freely moving electrons and, in between, an only weakly n-doped n^- layer (also known as an i-layer, i for intrinsic = intrinsically conductive). Its width w_p and doping density determine the maximum blocking voltage. The glass passivation of the edge zones provides protection from environmental impacts and stabilize reverse currents. (Figure 2.1.1).

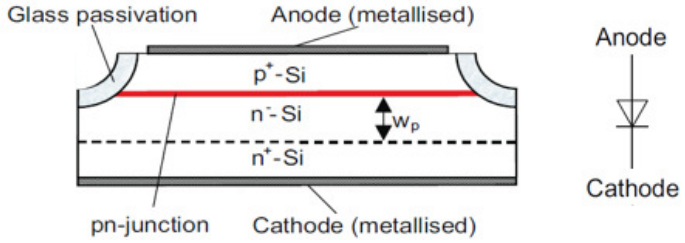


Figure 2.1.1 General structure and circuit symbol of a pin-diode

Diodes have an asymmetrical current-voltage characteristic. Without external voltage being applied, the electrons and holes present in the vicinity of the pn-junction recombine with each other, which is why they are no longer available for current transmission. Thus, an insulating thin layer with no free-moving charge carriers is created. This is called the space charge region, since a potential difference between p-doped and n-doped silicon is built up here because of the non-mobile charges of ionised doping atoms.
If a negative voltage is applied to the p-silicon (anode terminal) and a positive voltage to the n-silicon (cathode terminal), free electrons in the n-silicon are sucked toward the cathode, and the holes in the p-silicon toward the anode. Owing to this effect, the insulating space charge region is widened and the electric field intensity in the vicinity of the pn-junction increases. The diode is poled in reverse direction and there is (almost) no current flow.
Even if a diode is poled in reverse direction, a small current will flow. This is called the leakage current. This current results from the fact that free charge carrier pairs are generated in the space charge region as a result of thermal energy or irradiation. These charge carrier pairs are separated in the field of the space charge region and drained toward the terminals.
If a positive voltage is applied to the p-silicon (anode terminal) and a negative voltage to the n-silicon (cathode terminal), the free electrons in the n-silicon and the holes in the p-silicon are pushed into the space charge region. The space charge region is flooded by mobile charge carriers and disappears. A current flow and more charge carriers are supplied from the outer circuit. The diode is poled in forward direction (Figure 2.1.2).

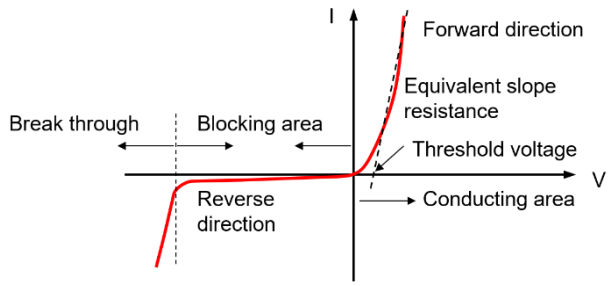


Figure 2.1.2 Current-voltage characteristic of a diode with voltage directions, current/voltage areas and equivalent resistance line

As indicated in Figure 2.1.1 the termination of the pin-junction at the edge of the chip is implemented by means of the mesa technology. That means that a groove or trench modifies the electric field at the discontinuity from bulk to dicing line at the edge of the chip. This is required to optimize the reverse blocking behaviour and minimizes the leakage currents. A passivation material is applied to the trench to further optimize the electric behaviour, and protecting the surface from environmental influences such as contaminants. Please refer to [2.1], [2.2] and [2.3] for more detailed explanations.

2.1.2 Static behaviour of pin diodes

2.1.2.1 Forward conducting behaviour

When forward voltage is applied, the current will increase steeply as soon as the threshold voltage ("ideal" 0.7V) for silicon pn-junction has been reached (Figure 2.1.2). Only at very high currents, which are far above the permissible continuous current, does this forward curve flatten out slightly. For low and medium currents, the temperature coefficient of the forward voltage is negative. At very high currents, this behaviour is reversed. When the forward current flows, losses ($I_F \cdot V_F$), heating up the diode. This heat limits the forward current, since excessive heat damage the diode.

2.1.2.2 Reverse blocking behaviour

If voltage is applied to a diode in reverse direction, the reverse current will initially rise until it reaches a level - at just a few volts -, which will barely increase further as the voltage is increased. The reverse current is highly temperature-dependent and rises proportionate to temperature. Under normal operating conditions, however, the losses that occur (blocking voltage · reverse current) are so small that they can be neglected when calculating the overall losses.
If the voltage applied in reverse direction is increased until it reaches the breakdown region (Figure 2.1.2), the reverse current will rise steeply (Avalanche effect). These results of sufficiently high electric field strength, the free charges generated in the space charge zone are accelerated so strongly that their kinetic energy is high enough to release other electrons from their bond in the lattice. These new free electrons and the holes created at the same time are also accelerated in the field and receive enough energy to create further charge carrier pairs by impact ionisation. This avalanche multiplication of free charge carriers increases the conductivity, and the reverse current rises rapidly (Figure 2.1.2).
In contrast to the reverse current, which increases with temperature, the avalanche breakdown voltage decreases with increasing temperature. Operating a diode in avalanche breakdown is only permitted if explicitly specified in the datasheet.

2.1.3 Dynamic behaviour of pin diodes

2.1.3.1 Turn-on behaviour

When the diode switches to conductive state, the voltage will initially increase to the peak turn-on voltage V_{FRM}. Only when the n^--region has been completely flooded by charge carriers will the forward voltage drop to its static value V_F (Figure 2.1.3). The forward recovery time t_{fr} is in the range of 100ns. The steeper the current rise and the thicker the low-doped n^--region in the diode, the higher the turn-on peak voltage V_{FRM} will be. V_{FRM} is hard to measure is often in the range of several 10V and may be 300V and above in extreme cases with high currents and high di/dt.

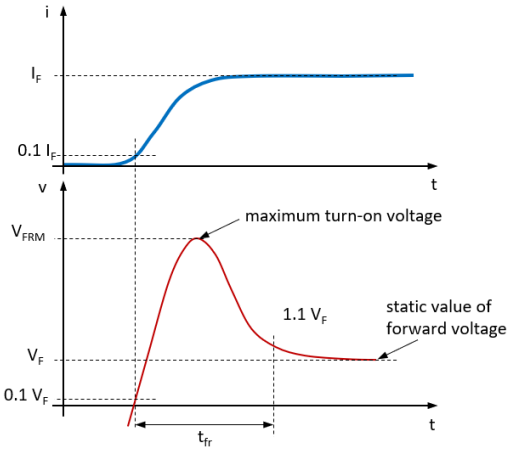


Figure 2.1.3 Turn-on behaviour of a pin diode

2.1.3.2 Turn-off behaviour

In conductive state, the entire volume of the diode is flooded with electrons and holes. If voltage polarity is reversed, the diode will also conduct in reverse direction, meaning that no blocking voltage can be built up. Owing to the reverse current and the recombination of electrons and holes, excess charge is depleted in the diode. As soon as all excess charge carriers are depleted to zero at the pin-junction, the diode can take up blocking voltage again, the peak reverse recovery current I_{RRM} is reached, and from this point on the reverse current will decline again (Figure 2.1.4).

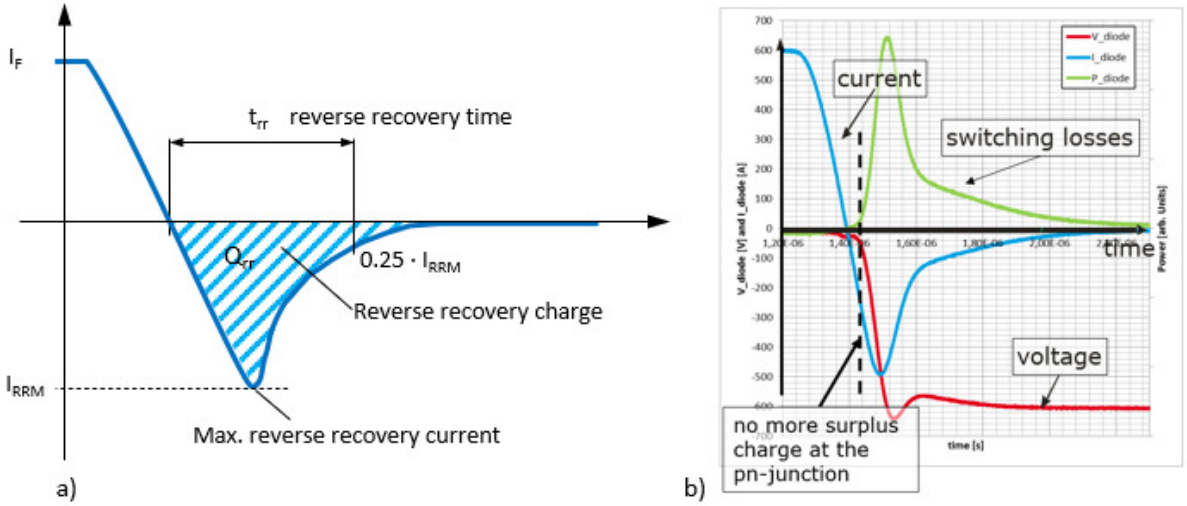


Figure 2.1.4 Turn-off behaviour of a pin diode: a) definitions and current curve; b) voltage and switching losses

The hatched area in Figure 2.1.4 a) represents the charge stored Q_{rr} in the diode (reverse recovery charge). When the peak reverse recovery current I_{RRM} has passed, voltage is present at the diode and a current flows through it. This results in switching losses, which may reach considerable levels at frequencies substantial higher as mains frequency. Reverse recovery time t_{rr}, reverse recovery charge Q_{rr} and peak reverse recovery current I_{RRM} increase strongly at higher temperatures. Diodes with a short reverse recovery time t_{rr}, small reverse recovery charge Q_{rr} and low peak reverse recovery current I_{RRM} are called fast diodes (cf. chapter 2.3 below) and are obtained by reducing the carrier lifetime, for example. However, the improved suitability for higher switching frequencies is offset by disadvantages - e.g., in the forward conduction behaviour.

2.1.4 Latest developments

Rectifier diodes by Semikron Danfoss featuring the **P**ower **E**nhancing **P**assivation technology (PEP) represent the next generation of input rectifier devices. They combine the established mesa edge termination known from today's classic SKR ("SEMIKRON Rectifier") diodes [2.1] with an innovative passivation process, allowing customers either to make use of a higher junction temperature and/or to increase the reliability of their power device [2.3].
The PEP diode technology consists of two product families: SKR PEP 1600V and SKR PEP 2200V. The main feature of the SKR PEP 1600V family is the maximum permissible junction temperature increase to 175°C. This allows for 20% to 25% higher current density compared to the existing SKR technology under the same thermal boundary conditions.
As initial examples of the SKR PEP 2200V family, Semikron Danfoss offers a bondable rectifier diode with a voltage rating of 2200V. Due to the higher blocking voltage, the junction temperature is limited to 150°C. The advances in chip technology also enable improved robustness in humid environments.

2.2 Thyristors for mains applications

2.2.1 Structure and functional principle

Thyristors for mains applications (also referred to as phase control thyristors) are used in large numbers in line-commutated converters due to their robustness, low forward losses and comparatively low cost. These are power semiconductor devices with at least three pn-junctions that can be switched from the off-state to the on-state in one of the two polarities (forward

blocking direction). In the opposite polarity (reverse blocking direction), switching on is not possible. In addition to the two terminals that a diode provides, a thyristor has a gate which serves to switch the thyristor to the on-state.
As shown in Figure 2.2.1, a thyristor consists of four alternating n- and p-doped zones. Together with the adjacent p-doped regions, the middle n⁻-region forms the high-blocking pin-junctions in forward and reverse direction. To avoid voltage flashovers at the chip edges, edge passivation must be carried out for both pin-junctions.

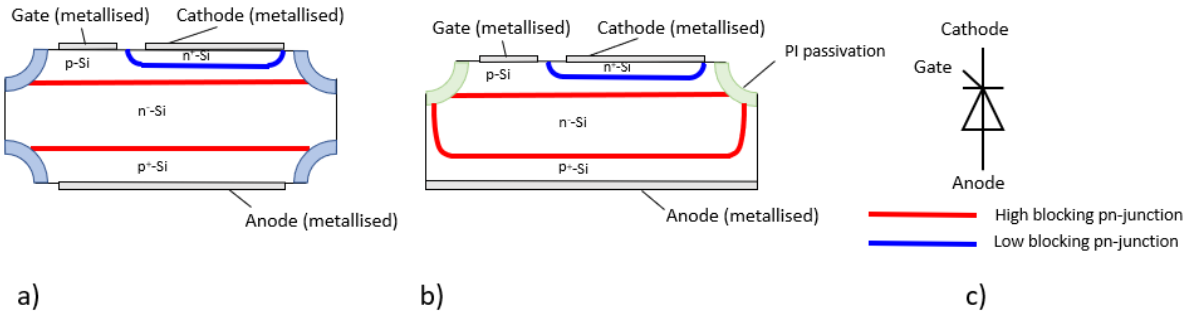


Figure 2.2.1 Structure and circuit symbol of a thyristor (The passivation provides protection from environmental impacts and stabilise reverse currents): a) General structure (conventional MESA design); b) SKT IEP technology; c) circuit symbol

Compared to the conventional (double) MESA insulation, the new developed semi-planar Semikron-Danfoss Isolation Diffusion Enhanced Passivation (IEP technology) enables a reduction in on-state slope resistance and thermal resistance by reducing the chip thickness. The main resulting features are lower on-state losses and a maximum permissible junction temperature increase to 150°C.

Figure 2.2.2 shows the characteristic field of a symmetrical thyristor. If the cathode is negatively polarized towards the anode (first operating quadrant of the current-voltage characteristic field in Figure 2.2.2 a), the thyristor can be switched from the forward blocking state to the conducting state (on-state) by means of a trigger signal.

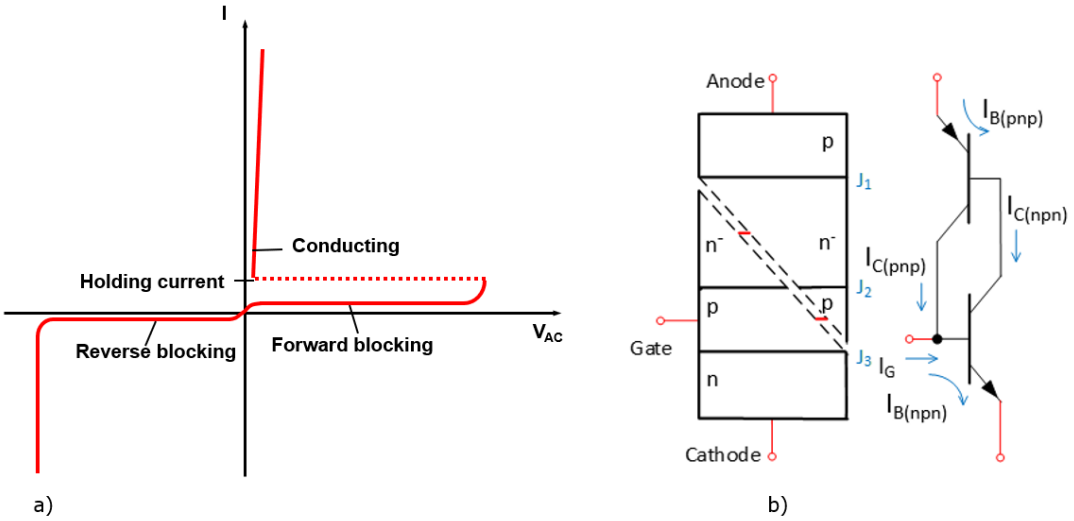


Figure 2.2.2 Thyristor working principle: a) Current-voltage characteristics and operating areas of symmetrical thyristors; b) two-transistor equivalent circuit diagram

To be able to understand how a thyristor works, you can first imagine the thyristor divided into a npn transistor and a pnp transistor as seen in Figure 2.2.2 b). In this two-transistor equivalent circuit of a thyristor, a positive trigger current I_G can flow in the forward direction through the gate-cathode pn-junction, J_3, and affect an injection of electrons from the n-cathode (emitter of the npn transistor). These electrons amplify I_G, and via J_2 in part reach the low-doped n⁻-zone, represented by the collector of the npn and base of the pnp transistor. The current in the pnp transistor is amplified by holes injected from the anode (emitter of the pnp transistor) into J_1 and flows through J_2 into the base of the npn transistor. This coupling of the transistor parts is crucial for the functioning of the thyristor.

The current gains of both transistors increase with current. As soon as the sum of the gate and anode currents is high enough that the sum of the current gains becomes $\alpha_{npn} + \alpha_{pnp} \geq 1$, the thyristor "fires" (triggers) and the characteristic curve changes from the "Forward blocking" to "Conducting" on-state. Therefore, a short current pulse to the gate is sufficient to trigger the thyristor generally. If the forward current reaches the latching current, I_L, the thyristor remains in the on-state even if the trigger current is removed. If later, the forward current drops below the holding current I_H, the thyristor returns to the forward blocking state.
When the thyristor is polarised in reverse-blocking direction, a current into the gate does not cause the thyristor to turn on. However, since the reverse current and thus the reverse losses increase due to this gate current, the injection of (positive) gate current in the reverse blocking state is not permissible.
However, when the polarity is in the forward direction, any current flowing through the pn-junction J_3 from the gate zone to the cathode zone may act as trigger current if it (or the sum of currents) is high enough:

- External trigger current from gate to cathode
- Parasitic current from the drive circuit (glitches, inductive or capacitive interference on the control lines, etc.)
- Forward blocking current generated thermally and/or by a high forward blocking voltage leading to breakover triggering when exceeding the zero-threshold-voltage
- Very high intensity light or radiation
- Capacitive displacement current caused by steeply rising forward-off-state voltage.

This leads to an inter-dependency of some trigger conditions (e.g., amplitude, rate of rise and duration of gate current) and conditions in the load circuit. More details of "Impermissible Triggering" cf. chapter 2.2.4.2 below.
As indicated in Figure 2.2.1 the termination of the pin junction at the edge of the chip is implemented by means of the mesa technology. That means that a groove or trench modifies the electric field at the discontinuity from bulk to dicing line at the edge of the chip. This is required to optimize the forward and reverse blocking behaviour and minimises the leakage currents. A passivation material is applied to the trench to further optimise the electric behaviour and protecting the surface from environmental influences such as contaminants. Please refer to [2.1], [2.2] and [2.4] for more detailed explanations.

2.2.2 Static behaviour of thyristors

2.2.2.1 On-state conducting behaviour

The on-state behaviour of thyristors essentially corresponds to that of diodes; only the forward voltage is slightly higher due to the two additional pn-junctions. When forward voltage is applied, current will increase steeply as soon as the threshold voltage has been reached. Only at very high currents, which are far above the permissible continuous current, does this on-state curve flatten out slightly. For low and medium currents, the temperature coefficient of the on-state voltage is negative. At very high currents this behaviour is reversed. When the on-state current flows, on-state losses are created (on-state current · on-state voltage), heating up the thyristor. This heat build-up limits the on-state current, since excessive heat might damage the thyristor.

2.2.2.2 Reverse blocking behaviour

If voltage is applied to a thyristor in reverse direction, the off-state current will initially rise until it reaches a level of a few micro- to milliamps - that will barely increase further as the voltage is increased. The reverse blocking current is highly temperature-dependent and increases in proportion to the temperature. If the voltage applied in reverse blocking direction is increased until it reaches the breakdown region, the off-state current will rise steeply as a result of the avalanche effect, cf. corresponding explanations in chapter 2.1.2.2.

2.2.2.3 Forward blocking behaviour

If voltage is applied to a thyristor in forward blocking direction, it initially behaves in the same way as when a voltage is applied in reverse direction. If breakover voltage is reached, the thyristor will suddenly transit into on-state and stays in this condition until this value falls below the latching current.
The forward blocking voltage is also temperature-dependent. At high temperatures, the forward off-state current is often higher than in reverse direction. The reason for this is usually the off-state current gain from the npn transistor for which this off-state current is a base current. Under normal

operating conditions, the losses that occur (blocking voltage · off-state current) are so small that they can be neglected when calculating the overall losses.

2.2.3 Dynamic behaviour of thyristors

2.2.3.1 Turn-on behaviour

The gate current required to turn-on a thyristor (gate trigger current I_{GT}) e.g., depends on its following properties:

- Chip geometry of the thyristor
- Position and geometry of the gate (edge gate, central gate, amplifying gate)
- Doping density of the gate zone (p-base)
- Adjusted lifetime of the charge carriers in the n^--zone
- Chip temperature (lower required I_{GT} at higher temperature)
- Applied anode-cathode voltage

The trigger process by external gate trigger current starts locally at the boundaries of the gate, as this is the area of the highest trigger current density. In mains thyristors the propagation of the triggered area is relatively slow with a speed of about 30…100µm/µs. This low propagation speed initially leads to very high current densities and intense local heating of the gate, depending on the load current slope which is limited by the external circuitry (Figure 2.2.3).

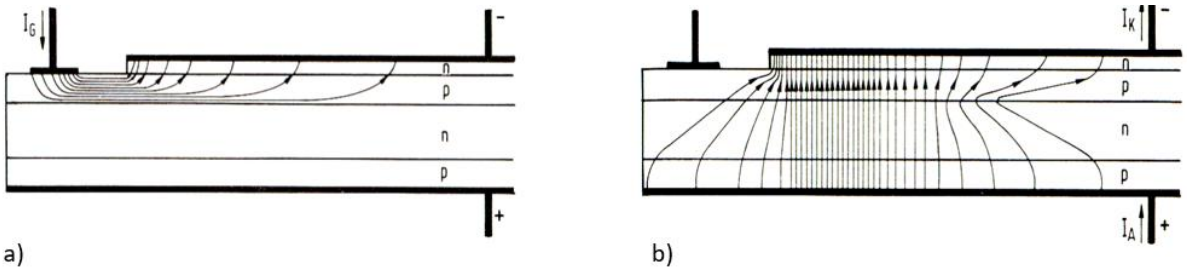


Figure 2.2.3 Current distribution in the thyristor: a) after gate current turn-on; b) immediately after trigger

After the thyristor has been triggered, the forward voltage will drop comparatively slowly to the static value V_T. This results in a power loss peak that grows in proportion to the current rise slope (Figure 2.2.4).

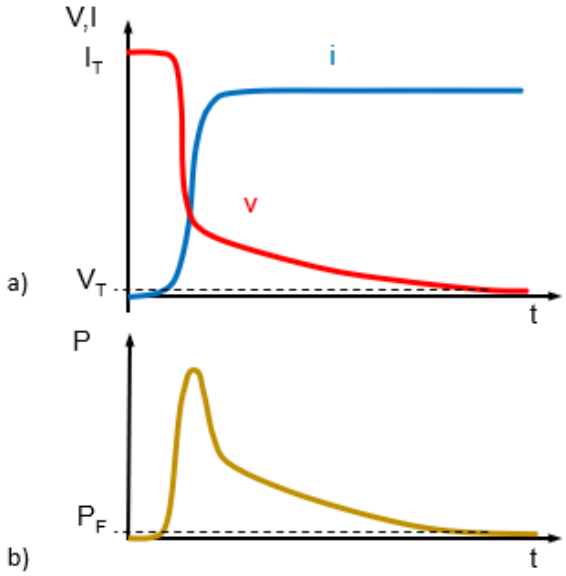


Figure 2.2.4 Thyristor turn-on: a) Current and voltage curves; b) course of thyristor power losses at turn-on

Since the area triggered initially is very small, the turn-on losses caused by the gradual decline of the on-state voltage to its static value V_T are concentrated on a small area. This causes the silicon to heat up locally. In order to avoid damage to the thyristor, the rate of current rise must be limited to the highest permissible critical rate of rise of on-state current $(di/dt)_{cr}$.

The $(di/dt)_{cr}$ rate - indicated in thyristor data sheets - is the highest permissible increase in forward current without damaging the thyristor. Thyristors with different gate structures (perimeter gate, central gate and amplifying gate) have different permissible values of $(di/dt)_{cr}$.
Table 2.2.1 qualitatively illustrates the dependence of the thyristor (di/dt) capability on some circuit parameters and operating conditions. This means that, for example, the (di/dt) capability decreases as chip temperature T_j or applied voltage V_D increases. The (di/dt) capability also increases with increasing gate current I_G, gate current slew rate di_G/dt, or trigger pulse duration t_p.

Affecting Parameter	**T_j**	**V_D**	**I_T**	**f**	**I_G**	**di_G/dt**	**t_p**
(di/dt) capability	↘	↘	↘	↘	↗	↗	↗

Table 2.2.1 Dependence of the (di/dt) capability on chip temperature T_j, operating voltage V_D, forward current I_T, mains frequency f, amplitude I_G, slew rate di_G/dt, and pulse duration t_p of the trigger current

Higher power thyristors are usually designed with an "amplifying gate" structure. These are equipped with an integrated auxiliary thyristor structure to improve the trigger behaviour and the critical current rise rate $(di/dt)_{cr}$. The auxiliary thyristor, whose cathode is connected to the gate of the main thyristor, amplifies the trigger current (Figure 2.2.5). The trigger energy for the main thyristor is taken from the main circuit.

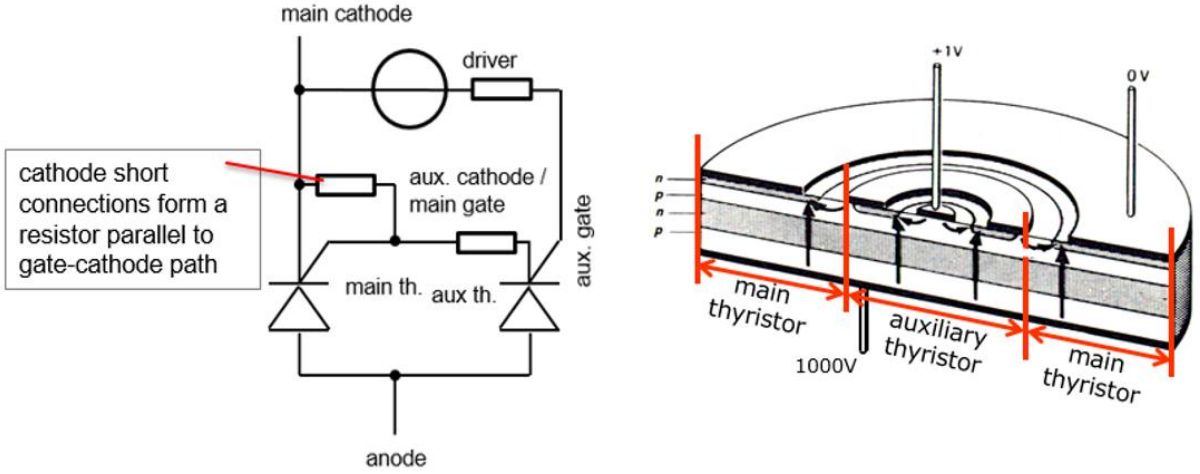


Figure 2.2.5 Equivalent circuit and structure of an amplifying gate thyristor

At a current into the auxiliary thyristor gate above its minimum trigger current, the voltage drop across the p-region exceeds the threshold voltage of the auxiliary gate-cathode diode path. The auxiliary thyristor triggers and opens a first conducting channel just below the boundary of the n-doped region of the auxiliary cathode. The width of this channel increases at 30…100m/s.
The current increase through the open channel is limited only by the resistance/saturation of the conducting channel, the lateral resistance of the p-region and by the load conditions of the thyristor (impedance of the load circuit). When the voltage drop across the resistance formed by the main cathode shorts exceeds the threshold voltage of the gate-cathode diode path of the main thyristor, current also flows through it and triggers the main thyristor. This opens a second conducting channel just below the boundary of the n-doped region of the main cathode. The main current begins to rise and the width of this channel also increases at 30…100m/s until the entire active region is flooded. At the same time, the auxiliary cathode current decreases (Figure 2.2.6).

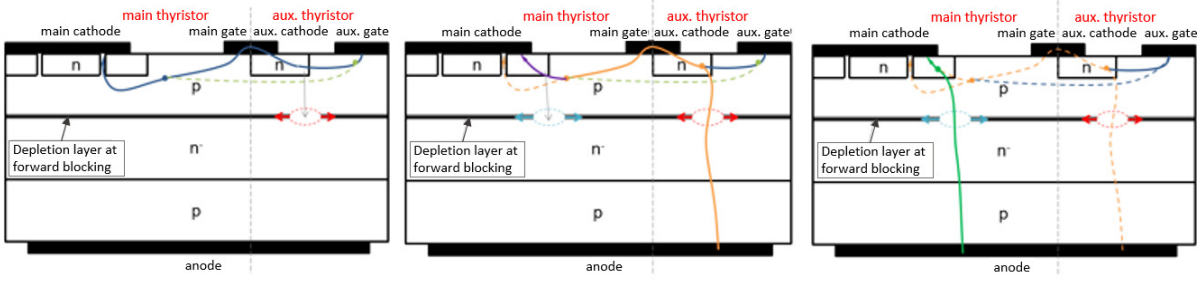


Figure 2.2.6 Trigger process of an amplifying gate thyristor

The ratio of $(di/dt)_{cr}$ is further improved by the finger-shaped amplifying gate which extends the edge length between auxiliary and main thyristor (Figure 2.2.7).

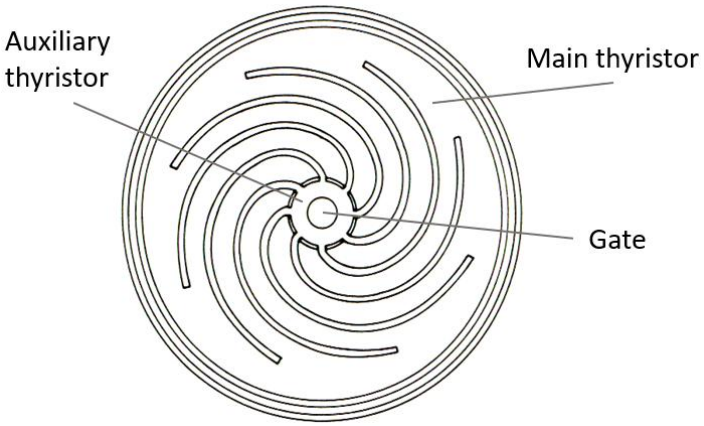


Figure 2.2.7 Example of a gate structure of an amplifying gate thyristor

2.2.3.2 Turn-off behaviour

Similar to mains diodes, the volume of a thyristor is flooded by charge carriers when a forward current flows. The majority of these charge carriers have to be depleted when the voltage is reversed for the thyristor to be able to pick up voltage in reverse direction.
Even then, there are still residual charge carriers in the semiconductor volume, which can lead to renewed, unwanted trigger of the thyristor if voltage is applied in the forward blocking direction before these charge carriers are not dissipated. The time that is necessary between the zero-crossing of the current and the recurring forward blocking voltage in order to avoid a renewed trigger of the thyristor is called circuit commutated turn-off time t_q (Figure 2.2.8).

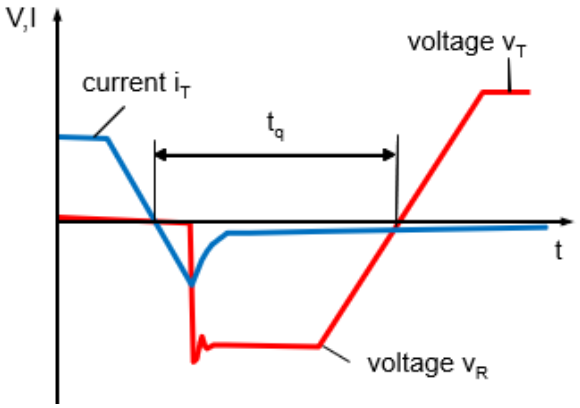


Figure 2.2.8 Anode current i_T and anode-cathode voltage v_T curves of a thyristor during turn-off and circuit commutated turn-off time t_q

Typical t_q values of mains thyristors described here are between 100µs and 500µs and are thus sufficiently short for most applications with mains frequency. For special applications at higher frequencies, some manufacturers are producing a strongly shrinking spectrum of fast ("frequency") thyristors, in which the release time has been reduced to 10…100µs by measures to reduce the carrier lifetime at the expense of other properties.

2.2.4 Trigger behaviour of thyristors

2.2.4.1 Thyristor control characteristics

After the basic triggering process has already been described in chapter 2.2.3.1, the quantitative requirements for safe triggering of thyristors are shown in Figure 2.2.9 as an example of a 100A SEMIPACK thyristor module with the data relevant for the design of the trigger circuit.

Characteristics					
Symbol	Conditions	min.	typ.	max.	Unit
Chip					
t_{gd}	T_j = 25 °C, I_G = 1 A, di_G/dt = 1 A/µs		1		µs
t_{gr}	V_D = 0.67 * V_{DRM}		2		µs
t_q	T_j = 130 °C		200		µs
I_H	T_j = 25 °C		150	250	mA
I_L	T_j = 25 °C, R_G = 33 Ω		300	600	mA
V_{GT}	T_j = 25 °C, d.c.	2.5			V
I_{GT}	T_j = 25 °C, d.c.	100			mA
V_{GD}	T_j = 130 °C, d.c.			0.25	V
I_{GD}	T_j = 130 °C, d.c.			4	mA

Figure 2.2.9 Tabular datasheet section of SKKT107/16E including trigger parameters [2.5]

The data sheet mentions values for gate-controlled delay time t_{gd} and gate-controlled rise time t_{gr}. These are the time intervals from applying the trigger current until the beginning of the forward voltage decay V_D across the thyristor (t_{gd}) or from the beginning to the end of this decay (t_{gr}) respectively. The circuit commutated turn-off time t_q is the required time between zero crossing of thyristor current i_T and the earliest re-application of forward off-state voltage, without parasitic turn-on of the thyristor.
The latching current I_L is the lowest anode current at which the thyristor remains in the on state at the end of the trigger pulse and does not turn off at the end of the trigger pulse. Turn-off occurs when the anode current falls below the holding current I_H.
Gate trigger voltage V_{GT} and Gate trigger current I_{GT} are the minimum values of control current and control voltage, which are required at 100µs pulse width for a guaranteed trigger. Below the highest gate non-trigger current I_{GD} or the highest gate non-trigger voltage V_{GD} at the gate, the thyristor will not trigger.

Influences	T_j	V_D	I_G	di_G/dt	t_p
I_H	↘	↘			
I_L	↘	↘	↘	↘	↘
V_{GT}	↘	↗	↗		
I_{GT}	↘		↘	↘	↘
V_{GD}	↘				
I_{GD}	↘	↘			

Table 2.2.2 Dependency of trigger parameters on chip temperature T_j, operating voltage V_D as well as amplitude I_G, rate of rise di_G/dt and pulse duration t_p of the trigger current

2.2.4.2 Impermissible Trigger

The current-voltage characteristic of a trigger circuit has to ensure that the current and voltage of the trigger pulses are within the safe trigger range over the full operating temperature range and the permissible peak trigger power is not exceeded, cf. chapter 7.2.
Triggering conventional thyristors by means other than supplying current to the gate is not permitted, as this is not a defined control pattern. The final destructive failure mode resulting from impermissible triggering is a $(di/dt)_{cr}$ failure.
Impermissible triggering may be caused by any current that flows via the p-base-emitter-junction J_3 in Figure 2.2.2 b) from the gate zone to the cathode zone. This leads to an inter-dependency of some trigger conditions (e.g., amplitude, rate of rise and duration of gate current) and conditions in the load circuit.
A parasitic current from the gate zone to the cathode zone can be for example:

Parasitic current from the gate driver

For example, residual currents in gate drivers circuit's off-state, glitches, inductive or capacitive interference on the control lines are parasitic currents that may contribute to impermissible trigger.

Forward off-state current

Current, generated thermally and/or by a high forward blocking voltage beading breakover triggering when exceeding the zero-threshold-voltage If the breakover voltage is exceeded (Figure 2.2.10), the off-state current will become so high that it will trigger the thyristor.

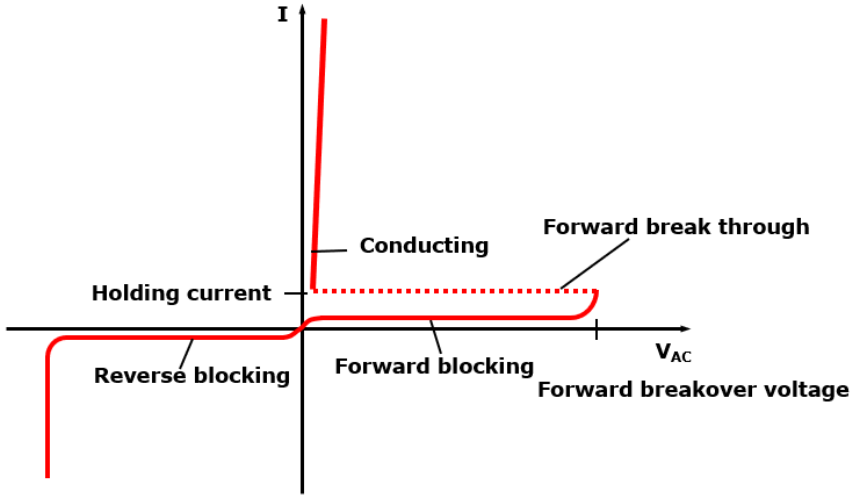


Figure 2.2.10 Impermissible trigger a thyristor by exceeding the breakover voltage

Since the off-state current rises in proportion to the temperature and the necessary trigger current decreases in proportion to the temperature, the breakover voltage will decline in proportion to the increase in temperature.

Current caused by very high intensity light or radiation

Light or radiation incidence creates charge carrier pairs which are separated in the space charge region and flow through the pn-junction to the cathode. They therefore act like a trigger current. The same is true for thermally generated charge carrier pairs.

Capacitive displacement current caused by steeply rising forward off-state voltage

Every pn-junction is a voltage-dependent capacitance. This capacitance will be biggest if no voltage is applied and will drop as the blocking voltage applied is increased. Changes in voltage (high dv/dt) cause a capacitive displacement current to flow through the pn-junction. If this current is high enough, it can, like any other current through the p-base–n-emitter junction, induce thyristor trigger.
The limit of impermissible trigger of a thyristor due to the steeply increasing off-state voltage is the critical rate of rise of (forward) off-state voltage $(dv/dt)_{cr}$, listed in the data sheets. The test condition for Semikron Danfoss thyristors is an exponential voltage rise up to 66% of the repetitive peak off-state voltage V_{DRM} at the maximum junction temperature T_{jmax} and an open gate. At lower T_j or lower off-state voltages, $(dv/dt)_{cr}$ is slightly higher. A parallel RC-snubber circuit for limiting internal overvoltage in combination with a suitable line inductance also limits the dv/dt, cf. chapter 8.4.2.

Trigger pulses during reverse blocking phase

Danger of destruction also exists with incomplete trigger if "regular" trigger pulses are insufficient for complete trigger or, if during the reverse blocking phase (3rd quadrant in the characteristic field), trigger pulses are generated, and current is injected into the gate. The trigger current then causes a strong increase in reverse current i_R and thus of the blocking losses in the thyristor (Figure 2.2.11).

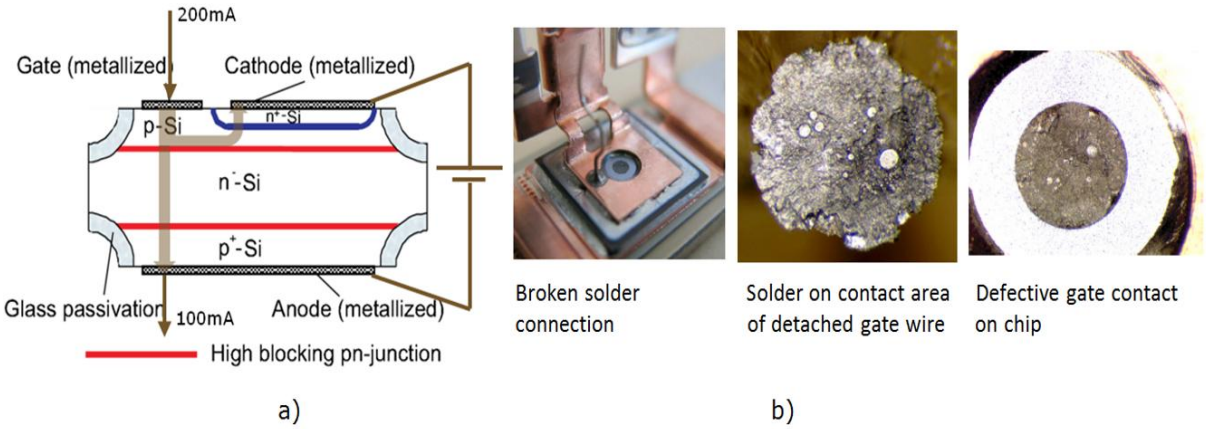


Figure 2.2.11 Trigger pulses during reverse blocking: a) Sectional drawing of thyristor with current flow from gate to cathode and anode (brown); b) Failure pattern of a thyristor chip inside a module

2.2.5 Further thyristor structures

Chapter 2.2 exclusively dealt with thyristors for mains applications up to around 690V AC voltage, as they can be found in Semikron Danfoss' current production programme. For reasons of available space, the design and properties of other types of thyristors for applications beyond this were not considered.
The Table 2.2.3 contains an overview of the basic characteristics of the thyristor design types produced by various manufacturers today. More detailed explanations of their operating principles and properties can be found in the literature, e.g. in [2.6] and [2.7].

Thyristor design	Typical application field		Blocking behaviour	Gate controllability	
	mains frequency	mains to middle frequency		turn-on	turn-off
Phase control thyristors (SCR)	✔		bidirectional	✔	
Symm. Fast thyristors (SCR)		✔	bidirectional	✔	
Asymm. Fast thyristors (ASCR)		✔	forward direct.	✔	
Light triggered thyristors (LTT)	✔		bidirectional	✔	
Reverse conducting thyr. (RCT)		✔	forward direct.[1)]	✔	
Bidirect. phase control thyr. (BCT)	✔		bidirectional	✔[2)]	
Bidirect. triode thyristors (TRIAC)	✔		bidirectional	✔[2)]	
Symm. Gate-turn-off thyr. (GTO)		✔	bidirectional	✔	✔
Asymm. Gate-turn-off thyr. (GTO)		✔	forward direct.	✔	✔
Integrated gate-commutated turn-off thyristors (IGCT)		✔	forward direct.	✔	✔
MOS-controlled thyristors (MCT)		✔	forward direct.[3)]	✔	✔
Static Induction thyristors (SITH)		✔	bidirectional	✔	✔

Meaning of the notes: [1)] Reverse conducting, [2)] Bidirectional gate control, [3)] Normally-on-state

Table 2.2.3 Basic thyristor designs

2.3 Fast diodes

2.3.1 Basics

Modern fast switching devices require fast diodes with adapted switching behaviour as freewheeling diodes in the power circuit. In the predominant applications which use inductive loads, the freewheeling diode is commutated from conductive to blocking state with every turn-on operation of the switch. Here, stored charges are to be depleted gently in order to avoid induced voltage spikes and high-frequency oscillations. For this reason, these diodes are also referred to as soft-recovery diodes. They are also instrumental to switch performance. When designing these devices,

a compromise between conflicting requirements has to be found. Two main types of fast diodes exist: the Schottky diode and "pin" or more precise "pn$^-$n^{+}"-diodes in epitaxial or diffused design

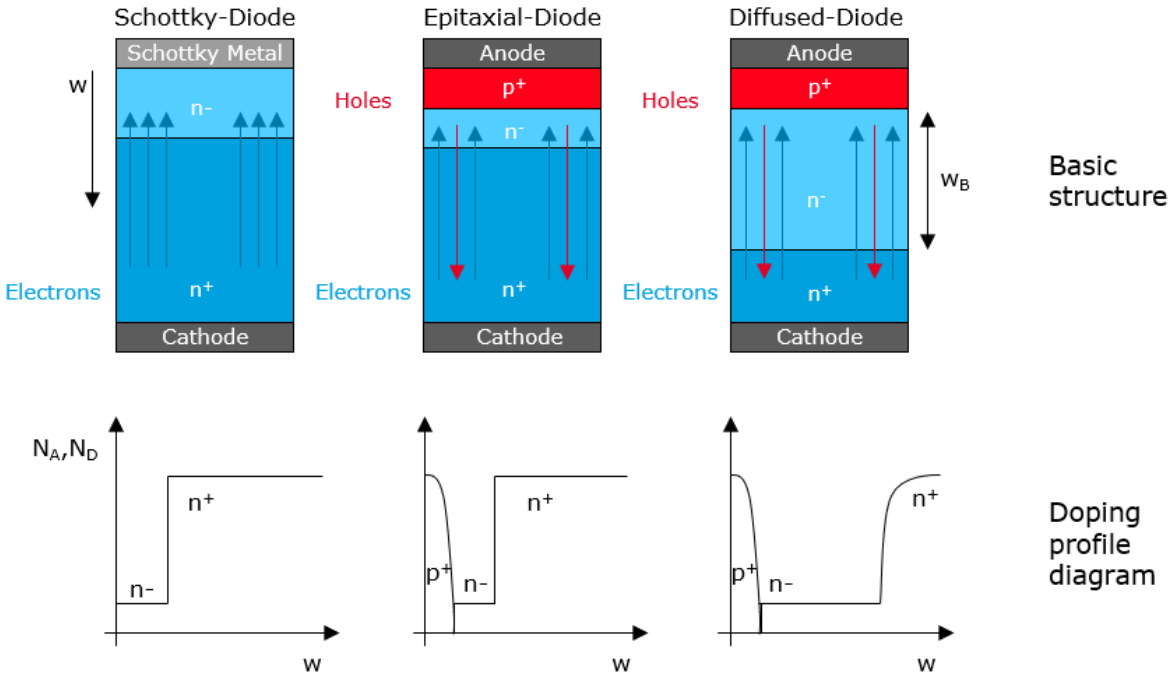


Figure 2.3.1 Schottky, pin-epitaxial and pin diffused diode

2.3.2 Structure and functional principles

2.3.2.1 Schottky diodes

In Schottky diodes (more precisely Schottky barrier diode SBD), the metal-semiconductor junction serves as a blocking junction. In on-state, only the small potential barrier between metal and semiconductor material must be overcome (around 0.3V for silicon or 1V for silicon carbide SiC). There is no diffusion voltage at the pn-junction as is the case in pin-diodes (approx. 0.7V for Si); this ensures a lower on-state voltage than occurs in any pin-diode, provided the n$^-$-region is thin. With n-doped material, only electrons participate in the current flow (unipolar). When diodes are operated close to the blocking voltage range and at higher temperatures, the off-state current will considerably increase. This must be considered for power loss ratings; otherwise, thermal stability cannot be ensured.
When switching from conductive to blocking state, ideally only the low capacitance of the space charge region must be charged. For this reason, the component storage charge is some powers of ten lower than the pin-diode, thus causing very low switching losses. As a result, the Schottky diode comes very close to being an ideal diode. Furthermore, are the turn-on losses of an IGBT reduced if used in combination with an IGBT as a freewheeling diode. The Schottky diode is particularly well suitable for use at higher frequencies and as a snubber diode with an extremely low on-state voltage.
For silicon, these advantages are limited to voltages ~100V. When higher blocking voltages are to be applied, the n$^-$-region must be extended, and the on-state voltage will increase considerably. In this voltage range, wide bandgap WBG materials with a higher permissible electric field strength such as SiC (<=3300V) are used. They have similar on-state characteristics to pin-diodes, but the advantages they offer as regards switching properties are retained. The costs for base material and production of WBG diodes are higher, however it will pay off easily by a high efficiency in applications that require higher switching frequencies.

2.3.2.2 Epitaxial diodes

The advantages of pin-diodes become effective from 100V upwards. In diodes produced today, the middle region is not "i" (intrinsic), but n$^-$-type, with a much lower doping level than in the outer regions. In epitaxial PIN diodes (Figure 2.3.1 mid) an n$^-$-region is first separated from the highly doped n$^+$-substrate (epitaxy). Then the p-region is diffused. In this manner, very small base widths w_B in the region of just a few µm can be obtained. By integrating recombination centres (mostly

gold), ultra-fast diodes can be achieved. Owing to the small base width w_B, the on-state voltage will remain low despite the recombination centres. That said, it will still always be greater than the diffusion voltage of the pn-junction (0.6 to 0.8V). The main field of application for epitaxial (epi)-diodes are applications with off-state voltages of between 100V and 600V.

2.3.2.3 Soft recovery diodes with controlled carrier lifetime (CAL)

From 1000V upwards, the n^--region is being enlarged to such an extent that a diffused PIN diode (Figure 2.3.1 to the right) can be obtained. The p- and n^+-regions are diffused into the n^--wafer. Recombination centres are also used. Recombination centre profiles similar to those shown in Figure 2.3.2 can be generated by implanting protons or He^{++}-ions into silicon. Implantation requires particle accelerators performing up to 10MeV.

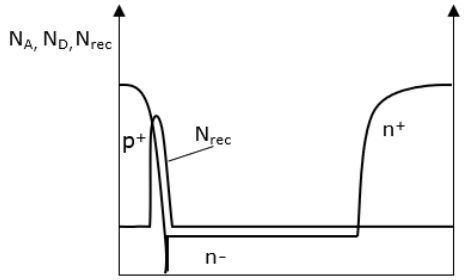


Figure 2.3.2 Narrow region with a high concentration of recombination centres at the pn-junction, generated by light ion irradiation

The arrangement of the high recombination centre density at the pn-junction (Figure 2.3.2) is an optimum set-up [2.1], [2.8]. In [2.9] it is demonstrated that the closer the arrangement of recombination centres at the pn-junction, the better the relation between peak reverse recovery current and forward on-state voltage will be. In on-state condition, charge carrier distribution will be inverted, with a higher charge carrier density at the n^--n^+-junction. The peak of radiation-induced recombination centres is even placed in the p-region close to the pn-junction in a CAL diode, since this will result in lower off-state currents. He^{++} implantation is combined with an adjustment to the basic charge carrier lifetime, preferably achieved by electron beam radiation. The height of the recombination centre peak can be adjusted by varying the dose of He^{++}-implantation: The higher the peak, the smaller the peak reverse recovery current. The main part of the CAL diode storage charge occurs in the tail current. The tail current itself can be controlled by the basic recombination centre density. A reduction in basic charge carrier lifetime will reduce tail current duration; however, this is to the detriment of the diode on-state voltage. The two parameters "basic charge carrier lifetime" and "He^{++} implantation dose" enable the recovery behaviour be controlled to a large extent. In this way, the diode will display soft-recovery behaviour under any operating conditions, especially when low currents are applied. CAL diodes manufactured in this way boast excellent dynamic ruggedness. CAL diodes dimensioned for 1200 V and 1700V have been tested under lab conditions at di/dt up to 15 kA/(cm²·µs) and did not result in diode destruction.
A comparatively narrow base width w_B can be chosen for CAL diodes regarding the Punch Through (PT) dimensioning described in chapter 2.3.3.2. This provides a comparatively low on-state voltage or results in a better compromise between switching characteristics and on-state voltage. The base width w_B also has a considerable impact on the turn-on behaviour of the diode. The forward recovery voltage V_{FR} rises in proportion to the increase w_B. In contrast to conventional diodes, 1700V diodes were shown to result in a more than a 50% reduction in V_{FR} [2.10]. Optimised dimensioning in the direction of PT dimensioning results also in improved cosmic ray stability.
The CAL diode has been improved over the years. The current main product is CAL 4F, accompanied by several variants from the same technology curve. For new products, the CAL 7 has been adapted to the different switching behaviour of MPT-IGBT (see 2.4.4). The new technology step comes along with a reduced forward voltage (see Figure 2.3.4) and is characterized by a particularly low turn-off overvoltage at low currents. These improvements could be reached with a thinner chip thickness and a changed profile of n+ region (Figure 2.3.3). The shallow profile at the n^--n^+-junction guaranties the soft recovery behaviour without scarifying the robustness against cosmic ray. Details can also be found in [2.11].

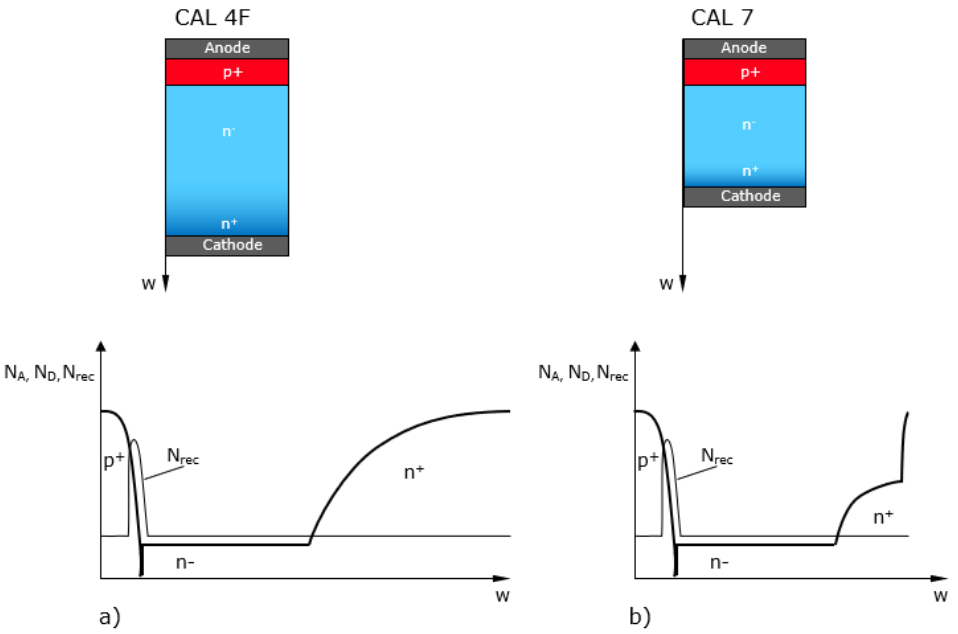


Figure 2.3.3 Comparison of structure of and doping profile of CAL 4F with CAL 7

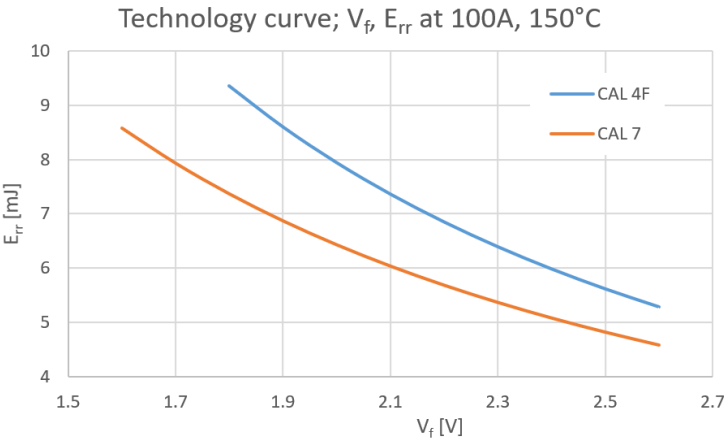


Figure 2.3.4 Figure of merit (V_f – E_{rr} characteristic) of CAL 7 in comparison to its predecessor CAL 4F

2.3.2.4 Emitter concept

In a common PIN diode, the pn-junction is flooded by more charge carriers than the n^--n^+-junction (Figure 2.3.12). The idea behind the emitter concept is to invert this charge carrier distribution: the n^--n^+-junction is to be flooded by more charge carriers than the pn^--junction. This is achieved by reducing the injection quantity at the p-emitter.

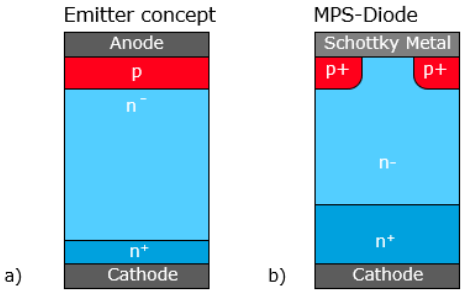


Figure 2.3.5 Diodes with emitter structures to improve soft recovery behaviour, a) reduced p-doping, b) Merged PIN/Schottky diode

A number of emitter structures whose functions basically result in this effect have been proposed. The Emitter Controlled Lifetime concept [2.11] is advantageous in combination with thin wafer

technology. The wafer is ground to a thickness slightly higher than the required base width of the voltage class (~n^--region, see also 2.3.3.2). Very thin p^+ and n^- regions are generated by diffusion from both sides of the wafer. Now with the possibility of diffusion from the n^+ side it is possible to optimise the carrier lifetime and distribution in the n^--n^+-region for example with platinum diffusion. The doping profile from n^- to n^+ is not a sharp junction anymore but a stepwise or smooth transition from the n^- level to the high n^+ level and is used to optimise the charge carrier concentration for a soft switching behaviour.
One other example is the "Merged PIN/Schottky diode", which consists of a series of p^+-regions and Schottky regions [2.13] (Figure 2.3.5). A number of similar structures also exist, including structures with diffused p-regions and n-regions. The advantages of Schottky regions or similar regions, however, are restricted to voltages below 600V. For blocking voltages of 1000V and above, the ohmic voltage drop outweighs this effect. What is left is the reduction of the area of injecting sub-areas at the p-region.

2.3.3 Static behaviour

2.3.3.1 On-state behaviour

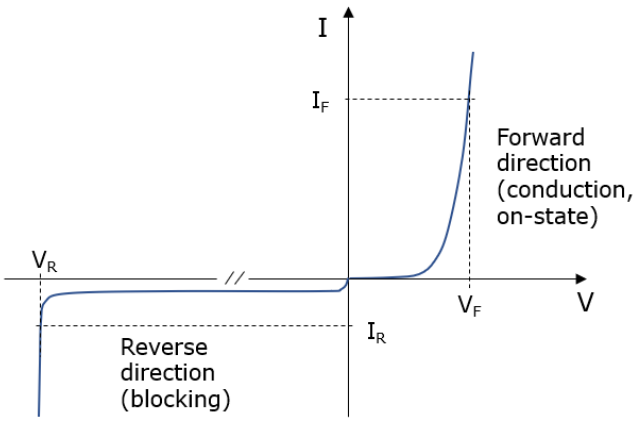


Figure 2.3.6 Definition of reverse and forward voltage and current

The maximum forward voltage V_F indicates that, at a specified current, the forward voltage drop across the diode must not exceed the specified limit value. This specification is made for room temperature and a higher temperature, typically the maximum recommended operating temperature. In forward direction, the current must overcome the diffusion voltage of the pn-junction and the resistance of the adjacent n^--region. The voltage drop is composed of

$$V_F = V_{diff} + V_{drift}$$

The diffusion voltage at the pn-junction depends on the amount of doping of both sides of the pn-junction and it is typically in the range of 0.6...0.8 V. The drift share depends on the base width w_B (proportionate to the blocking voltage) and the charge carrier density. For fast diodes with a blocking voltage of 600V and above, the drift part dominates. The charge carrier lifetime of freewheeling diodes has to be kept short. In the classic approximation derived by Hall [2.14], V_{drift} is given by:

$$V_{drift} = \frac{{w_B}^2}{(\mu_n + \mu_p) \cdot \tau_{HL}}$$

The on-state voltage will depend quadratically on the base width w_B and inverse proportional on the high-injection charge carrier lifetime τ_{HL}, for not too short τ_{HL}. Due to this exponential correlation, it is important to select the smallest possible w_B. Further, μ_n and μ_p represent electron and hole mobility, provided the n^--region is flooded with free electrons and holes. However, in this equation there is no direct dependency of V_{drift} from the current. This obviously contradicts measurements. The experimental forward voltage is noticeably higher and increases stronger with current than according to above equation. The reason is that the characteristics in modern power devices including freewheeling diodes are strongly determined by emitter recombination.
In one way, this can be expressed by an effective carrier lifetime τ_{eff} [2.15]:

$$V_{drift} = \frac{{w_B}^2}{(\mu_n + \mu_p) \cdot \tau_{eff}}$$

where τ_{eff} includes the emitter recombination, is current dependent and decreases with current density since the emitter efficiency decreases with increasing current. Also, it can be written as

$$V_{drift} = \frac{{w_B}^2}{(\mu_n + \mu_p) \cdot \tau_{HL}} \cdot \left(\frac{1}{2} + \sqrt{\frac{1}{4} + \frac{H}{q} \cdot \frac{{\tau_{HL}}^2}{{w_B}^2} \cdot j} \right)$$

Here, j is the current density, and H stands for the emitter influence of both the p-emitter and the n^+-emitter of the diode. Small H means strong emitter efficiency, and for very small H this equation approaches to the classical Hall approximation. The last equation is very useful for a fit of measured forward characteristics of freewheeling diodes. In very most cases a dependency of V_F to the square-root of the current density is found. A detailed consideration is given in [2.16].
The diffusion voltage V_{diff} has a negative temperature coefficient, while μ_n and μ_p decrease with temperature, and τ_{HL} increases with temperature. Depending on which part is dominant, there will be an intersection of the on-state characteristic "Hot" and "Cold" at different current levels, typically within the rated current range or up to 3-4 times the rated current.

2.3.3.2 Blocking behaviour

The reverse voltage V_R indicates that, at a specified value, the reverse current must not exceed the limit for I_R. Specifications in the databooks are made for an operating temperature of 25°C. In case of lower temperatures, the blocking capability will decrease, for example by about 1.5V/K for a 1200V diode. For components which are operated at temperatures below room temperature, this has to be taken into account in the circuit layout. At higher temperatures, the blocking voltage will increase accordingly. At the same time, the reverse current will also rise, doubling roughly every 10K. For this reason, a reverse current is also specified for a high temperature (125°C or 150°C). For gold-diffused components, the reverse current increase may be very strong, possibly causing problems due to thermal instability in systems operated at high temperatures.

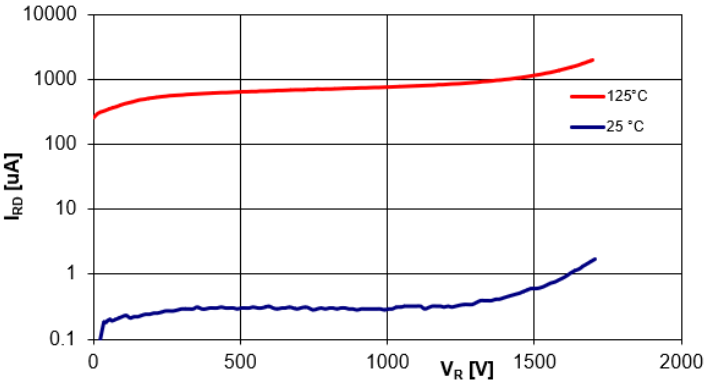


Figure 2.3.7 Example of the reverse current of a 1700V CAL diode, parameter T_j

The base width w_B not only affects the on-state voltage but also has a crucial impact on the blocking voltage. Two cases can be distinguished between (Figure 2.3.8): if w_B has been dimensioned such that the space charge zone cannot protrude into the n+-region (triangular field shape), this is called Non-Punch-Through (NPT) dimensioning in line with the terminology used for IGBT [2.17]. If w_B has been dimensioned such that the space charge region protrudes into the n+-region, the field shape will be trapezoidal, and the diode is called a Punch-Through (PT) diode. This, however, is not actual punch-through, where the space charge region would reach the area of the other doping type. This designation has nonetheless become widely accepted.

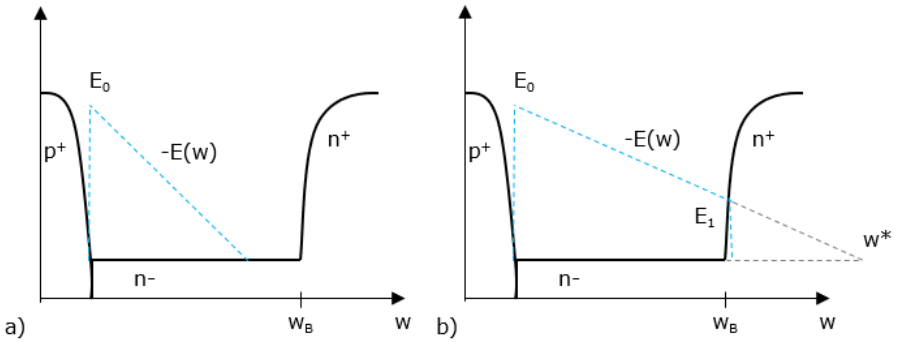


Figure 2.3.8 Diode dimensioning for triangular (NPT a)) and trapezoidal (PT b)) field shape for $0 \leq w \leq w_B$

For an ideal NPT diode, w_B is selected such that, at maximum reverse voltage, the end of the triangular field is located at this point. For optimum doping, the minimum width would then be

$$w_{B(NPT)} = 2^{\frac{2}{3}} \cdot C^{\frac{1}{6}} \cdot V_{BD}^{\frac{7}{6}}$$

$C = 1.8 \cdot 10^{-35}\ cm^6V^{-7}$

The minimum doping needed for PT diodes can be calculated in the same way. In the extreme case, the field would be rectangular, $E_1 = E_0$ (Figure 2.3.8). This results in

$$w_{B(PT,limit\ case)} = C^{\frac{1}{6}} \cdot V_{BD}^{\frac{7}{6}}$$

Compared to w_B for the NPT diode, the following applies:

$$w_{B(PT,limit\ case)} = 2^{\frac{-2}{3}} \cdot w_{B(NPT)} \cong 0.63 \cdot w_{B(NPT)}$$

Although this extreme case cannot be achieved, available technology allows us to come close to this, i.e.:

$$w_{B(PT)} \cong 0.66 \cdot w_{B(NPT)}$$

For the charge carrier lifetimes presently in use, the difference in forward voltage for PT dimensioning and NPT dimensioning is approximately 0.8V. For this reason, PT dimensioning is to be given preference if possible.

2.3.4 Dynamic behaviour

2.3.4.1 Turn-on behaviour

When a pin diode is turned on, it has to overcome the resistance of the low-doped base. The turn-on peak voltage thus increases proportionate to w_B. The turn-on peak voltage becomes especially critical if a significant base width w_B has to be chosen due to a high blocking voltage of more than 1200V. For this reason, optimum turn-on behaviour is once again achieved with PT diodes. Freewheeling diodes always contain recombination centres to reduce charge carrier lifetime. Recombination centres (e.g. gold) causing an increase in base resistance are to be avoided for diodes with a high blocking voltage. Recombination centres generated by platinum diffusion, electron beam radiation or light ions will only slightly increase the turn-on overvoltage in comparison to diodes without recombination centres.
When the diode turns into the conductive state, the voltage will initially increase to the repetitive peak forward voltage V_{FRM} before dropping to the forward voltage level again (Figure 2.1.3). When the current is actively switched at a very high di/dt ratio, V_{FRM} may reach between 200V and 300V for an unsuitable 1700V-diode, a level which is more than 100 times the value of V_F. Turning the diode on from a blocked state will result in a far higher V_{FRM} than turning it on from a neutral state. A low V_{FRM} is one of the most important requirements of snubber diodes, since the snubber circuit becomes effective only after diode turn-on.
The repetitive peak forward voltage is also of importance for freewheeling diodes in IGBT which are designed for a blocking voltage > 1200V. When the IGBT is turned-off, a voltage spike is generated across the parasitic inductances which still superimposes the V_{FRM} of the freewheeling diode. The sum of both components may cause critical voltage peaks. However, this measurement is not

trivial, since the inductive component and V_{FRM} cannot be told apart in application-oriented chopper circuits in a double pulse measurement for example. Measurements can be taken on an open construction directly from the diode bonding wires. Turn-on behaviour of a diode is rarely important for the total power losses, since turn-on losses only amount to a small percentage of the turn-off and forward on-state losses and are therefore negligible.

2.3.4.2 Turn-off behaviour

When turning from the conductive into the blocking state, the stored charge carriers must be discharged. This allows a current to flow in reverse direction through the diode. The waveform of this current characterises the reverse recovery behaviour.

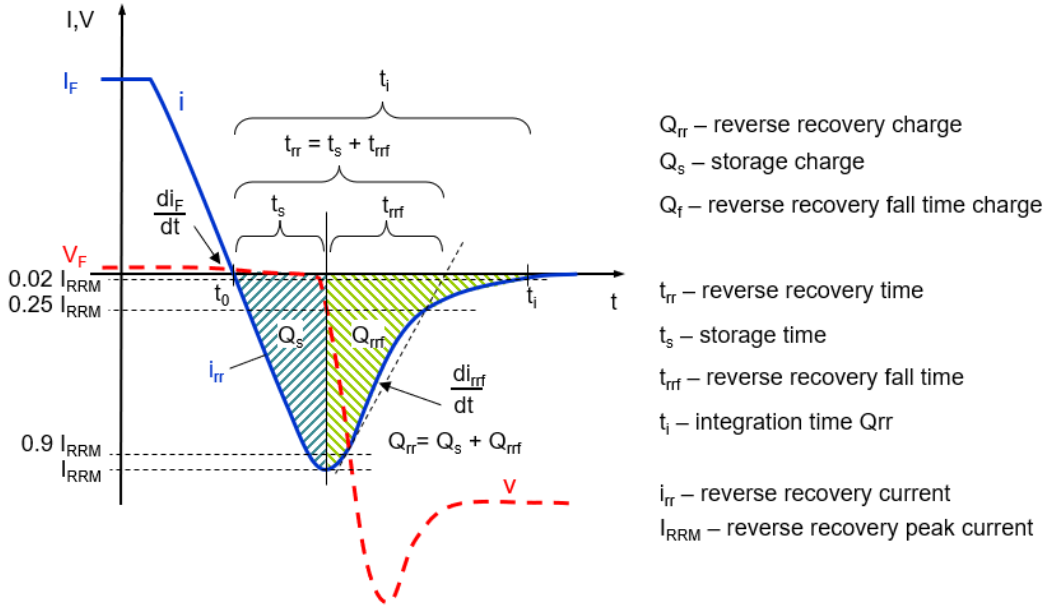


Figure 2.3.9 Current and voltage characteristic during reverse recovery of a soft-recovery diode in a chopper circuit and definition of characteristics of the recovery behaviour

The rate of change during commutation di_F/dt (Figure 2.3.9) is determined either by the switching speed of an active switch (IGBT, MOSFET) or by the commutation inductance. It is measured at t_0 during the zero crossing of the current. At the instant at which the pn-junction becomes free of charge carriers the diode starts to pick up voltage. At I_{RRM} the reverse current reaches its maximum. After I_{RRM} has elapsed, the current declines to the reverse current. The current characteristic depends solely on the diode. A steep decline in current is referred to as snappy recovery behaviour. A slow decline in current is referred to as soft recovery behaviour. The di_{rrf}/dt during declining is measured in a $10\% \cdot I_{RRM}$ window to determine the maximum value. It is responsible for the overvoltage at the diode, which is why soft recovery behaviour is aimed at. Reverse recovery time t_{rr} is defined as the period between t_0 and the moment where a tangent between 90% and 25% of the maximum I_{RRM} intersects the zero axis again. The integration interval for Q_{rr} is between t_0 and t_i at 2% of I_{RRM}.

$$Q_{rr} = \int_{t_0}^{t_i} i_{rr} dt$$

Soft recovery behaviour (pin) diode

As shown in Figure 2.3.9, differentiating between t_{rrf} and t_s for t_{rr} helps to define a "soft factor" as a quantitative characteristic for recovery behaviour:

$$\text{Soft factor} \quad s = \frac{t_{rrf}}{t_s}$$

The soft factor should be greater than 1 in order to minimise switching overvoltage. However, this definition is imprecise. For example, the current characteristic shown in Figure 2.3.10 a) would be regarded as snappy, whereas the current characteristic as in Figure 2.3.10 b) would be considered soft.

Despite s > 1, there is a steep edge in a part of the reverse current flow. A definition that refers to the maximum di_{rrf}/dt during the fall time t_{rrf} would be better.

$$\text{Soft factor} \quad s = \frac{\frac{di_F}{dt}}{\frac{di_{rrf}}{dt}}$$

For a soft recovery diode, di_{rrf}/dt is within the range of di_F/dt.

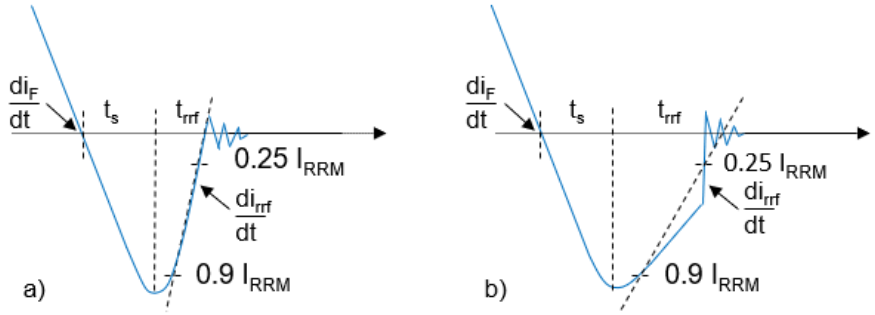


Figure 2.3.10 Current characteristic for two different possibilities of snappy reverse recovery behaviour

Specifying the recovery behaviour at the nominal operating point only is likewise not sufficiently meaningful. It varies as a function of different circuit parameters.

- Current: Measurements have to be taken at a current flow of less than 10% and at 200% of the specified current. This approach gives proper consideration to the fact that small currents are particularly critical for the reverse recovery behaviour.
- Temperature: High temperatures are often more problematic for the recovery behaviour at high currents. At low currents, the recovery behaviour will deteriorate at room temperature or below.
- Voltage applied: Higher voltage results in poorer reverse recovery behaviour.
- Rate of fall for di_F/dt: The dependency of di/dt varies greatly in diodes made by different manufacturers. One type of diode will become "softer" when the di/dt increases, while another will become "snappier".
- Pulse length: with very short pulses (1…3µs) the diode is not fully flooded by holes; the missing charge leads to a snappier behaviour (see chapter 9.2.3.4)

The best way to characterise soft recovery behaviour is to measure the turn-off overvoltage under different operating conditions (I_F, T_j, V_{CC}, di/dt). In a typical application, where the chopper is in a semiconductor module, the parasitic inductance of the commutation loop L_s is in the range of some 10nH. This reduces the overvoltage generated. Due to a lack of ideal switches, the voltage applied to the IGBT will drop to a certain degree during the reverse recovery phase. The voltage measured becomes

$$-V(t) = -V_{CC} - L_s \cdot \frac{di}{dt} + V_{CE}(t)$$

where $V_{CE}(t)$ is the voltage across the IGBT at the given moment in time. In a 100A soft recovery diodes with moderate rates of rise of up to 1500A/µs and minimum parasitic inductances, V(t) will very often be smaller than V_{CC} at any time and no voltage spikes will occur.

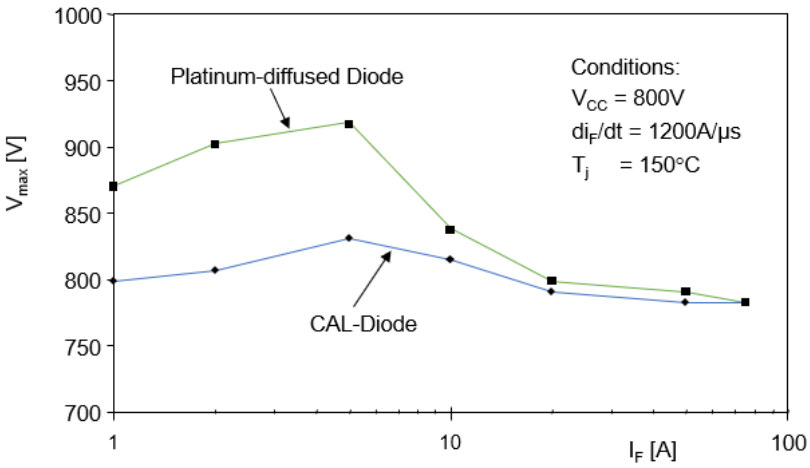


Figure 2.3.11 Peak voltage during commutation in dependence of the forward current as a parameter for diode switching behaviour

Figure 2.3.11 compares the overvoltage of a CAL diode to that of a platinum-diffused diode with reduced p-emitter efficiency. At rated current (75A), the platinum-diffused diode is just as soft as the CAL diode. For lower currents, however, overvoltage caused by snappy switching behaviour will be present in the diode. The maximum overvoltage at 10% rated current will be as over 100V. The IGBT used will switch even lower currents more slowly, and the overvoltage will decrease. By way of contrast, CAL diodes don't display significant overvoltage under any condition. Considered from the point of view of semiconductor physics, Figure 2.3.12 a) shows the concentration of charge carriers in the cross section of the semiconductor material during turn-off in a snappy diode and Figure 2.3.12 b) depicts the same for a soft recovery diode.

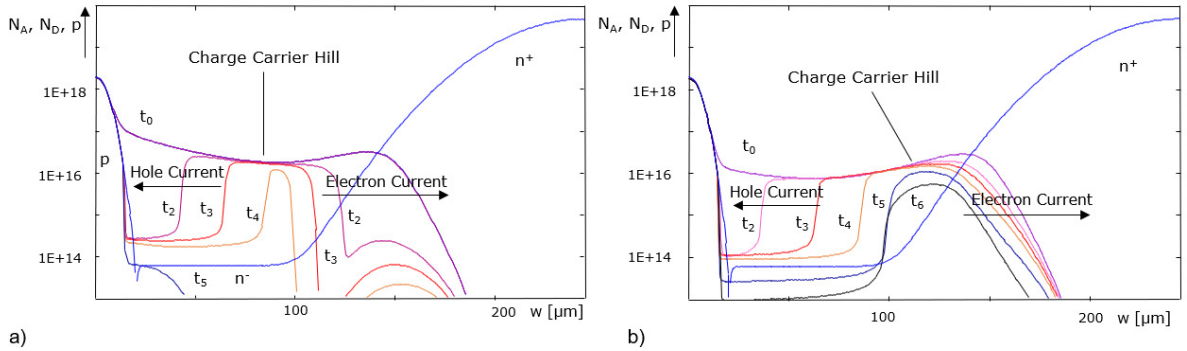


Figure 2.3.12 Diffusion profile and simulation of the decline in charge carriers (hole density) in a a) snappy diode and b) soft recovery diode

Under on-state load, the n^--region of the diode is flooded by > $10^{16}cm^{-3}$ of electrons and holes; the concentration of electrons (n) and holes (p) may be assumed to be equal. During the switching operation, a charge carrier hill is formed between t_2 and t_4 in the n^--region; at the same time n ≈ p. Charge carriers are reduced toward the cathode as a result of the electron flow and toward the anode owing to the hole flow, which appears as reverse current in the outer circuit. In the case of the snappy diode, the charge carrier hill will have been consumed shortly after t_4 has elapsed. Between t_4 and t_5 no charge carriers left to support current flow; the diode reverse current will suddenly snap off.
In a soft-recovery diode is a charge carrier hill present which feeds the reverse current throughout the entire process. At t_5, the diode will already have picked up the voltage applied. The dynamic behaviour described results in a tail current, as shown in the measurement in Figure 2.3.14. Whether soft recovery behaviour will be achieved depends on how successfully this charge carrier reduction is managed. The following measures will result in softer recovery behaviour:

- The width w_B in the n^--region is enlarged, NPT dimensioning is used, and a region is also integrated into the diode which cannot be reached by the field at nominal voltage. This, however, will result in a stark increase in on-state voltage or in the V_F/Q_{rr} relation.
- In order to restrict the increase in w_B somewhat, a two-stage n^--region can be used [2.18] with increased doping close to the n^-n^+-junction. Figure 2.3.12 demonstrate how a similar

effect is achieved by a flat gradient at the n^--n^+-junction. This measure alone, however, will not be enough to achieve soft recovery behaviour.
- Charge carrier distribution is inverted by a low-efficiency p-emitter (see 2.3.2.4).
- An axial charge carrier lifetime profile according to the CAL concept, providing for a low charge carrier life at the pn-junction, and a longer charge carrier life at the n^--n^+-junction.

To ensure soft recovery behaviour under any conditions, several of these measures normally must be taken at the same time. That said, the achievements made in this respect must always be assessed with a view to the extent to which a higher on-state voltage or a higher Q_{rr} is accepted.

Switching losses

The easiest way to characterise turn-on and turn-off behaviour is to use a step-down converter (chopper) circuit as shown in Figure 2.3.13 a). The IGBT T_1 is turned on and off twice by means of a double pulse. The current level is set with the first pulse. The turn-off time (conduction of the diode) should be long enough to guarantee full conduction but short enough to keep the current almost constant (several 10µs). The di_F/dt during switching is set by the gate resistor R_{Gon}. V_{CC} is the DC link voltage. Parasitic inductances $L_{s1...3}$ are unavoidable in the connections between capacitors, IGBT and diode but should be as small as possible.

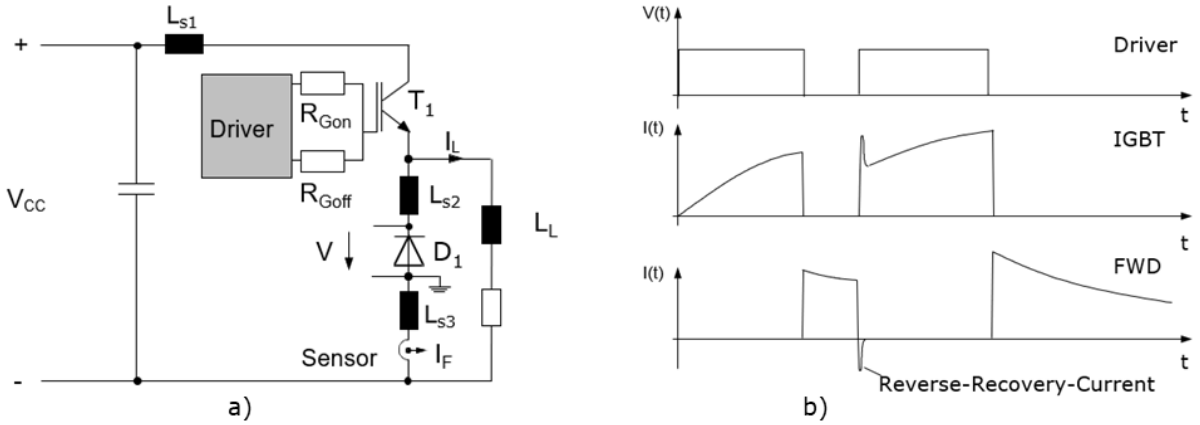


Figure 2.3.13 a) Reverse recovery test circuit; b) Driver control signal, current of IGBT and freewheeling diode during double-pulse operation

Figure 2.3.13 b) shows the IGBT control signals ("driver") and the current flow in the IGBT and diode during double-pulse operation. By turning off the IGBT, the load current in the inductance L_L will be taken over by the freewheeling diode. As soon as the IGBT is turned on next time, the current commutates from the diode into the IGBT and at that very moment the recovery behaviour will be characterised. In addition, the IGBT takes over the reverse current of the freewheeling diode during turn-on. This process is depicted at a higher time resolution in Figure 2.3.14 for a soft recovery diode.

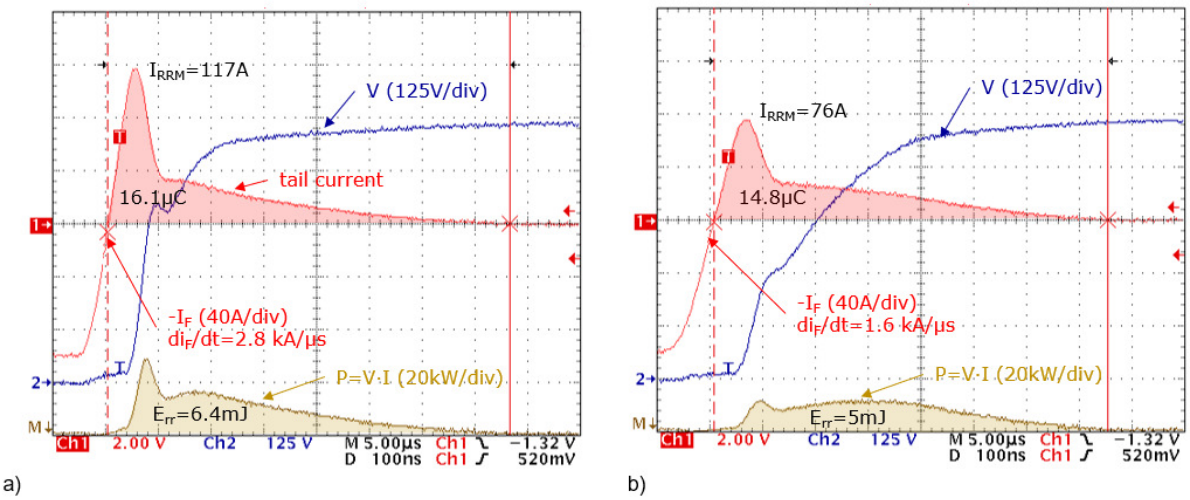


Figure 2.3.14 Current, voltage and power losses during recovery behaviour measurements of a 100A/1200V-CAL diode a) at 0.5Ω and b) at 8.2Ω

The diode reverse recovery characteristic can be divided into two phases: The phase of increase up to the reverse peak current and the subsequent drop in reverse current with di_r/dt.
The second part is the tail phase where the reverse current slowly declines to zero. A t_{rr} can no longer be reasonably defined. The tail phase causes the greatest losses in the diode, since voltage is already applied to the diode. A snappy diode without tail current generates less switching losses in the diode but also high overvoltage during turn-off. The tail-phase is less harmful to the IGBT, since the applied voltage has already decreased at this time.
For the overall power losses of both IGBT and diode, it is important to keep the peak reverse current low and to have the main part of the storage charge discharged during the tail phase. The trend towards increasingly faster switching - thus reducing the switching losses in the IGBT - results in ever increasing stresses on the diode. Depending on the type of application, it may be useful regarding the total losses to switch more slowly than recommended in the datasheet ratings.
Switching losses largely depend on 4 parameters:

- The rate of rise of commutation current di/dt or the gate resistance of the switching IGBT (Figure 2.3.15 a): switching losses tend to fall in proportion to the increase in resistance; with a very small gate resistance, the existing stray inductance will limit di/dt. The range shown corresponds to a gate series resistor of 0.5Ω up to 8.2Ω.
- The blocking voltage (DC link voltage V_{CC}; Figure 2.3.15 b), which builds up in the component after turn-off. The dependency can be approximately calculated using an exponent of 0.6:

$$E_{rr}(V_{CC}) = E_{rr}(V_{ref}) \cdot \left(\frac{V_{CC}}{V_{ref}}\right)^{0.6}$$

- Forward current I_F (Figure 2.3.16 a): The higher the current, the greater the losses. However, this dependency is not linear and can be approximated using an exponent between 0.5 and 0.6:

$$E_{rr}(I_F) = E_{rr}(I_{ref}) \cdot \left(\frac{I_F}{I_{ref}}\right)^{0.6}$$

- Junction temperature T_j (Figure 2.3.16 b): Switching losses initially rise linear to the temperature. Only above 125°C does the increase become slightly disproportionate. Using a temperature coefficient of 0.0055…0.0065, the switching losses can be calculated as a function of the temperature:

$$E_{rr}(T_j) = E_{rr}(T_{ref}) \cdot \left(1 + TC_{Err} \cdot (T_j - T_{ref})\right)$$

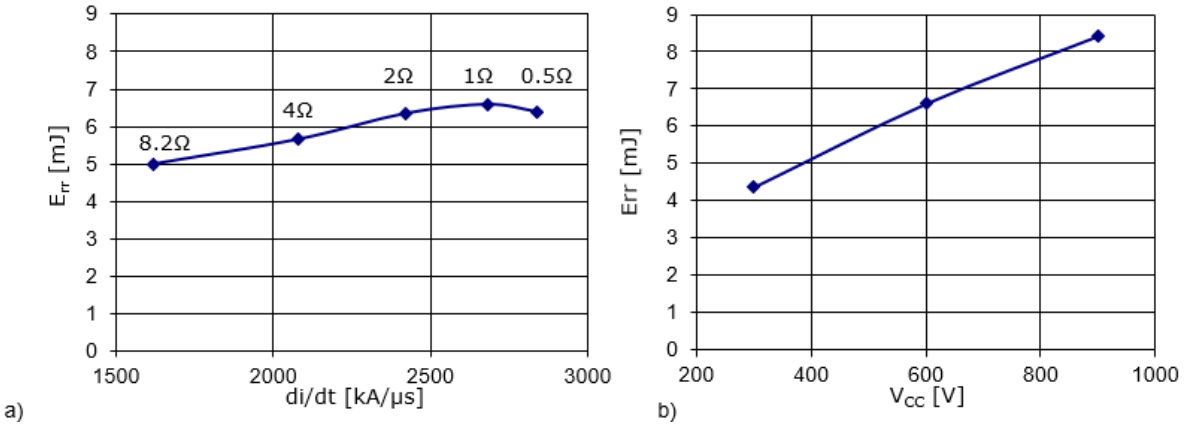


Figure 2.3.15 Dependencies of E_{rr} of a 100A/1200V CAL diode; a) on di/dt (@100A, 600V, 150°C); b) on V_{CC} (@100A, R_G=1Ω → 2700A/µs, 150°C)

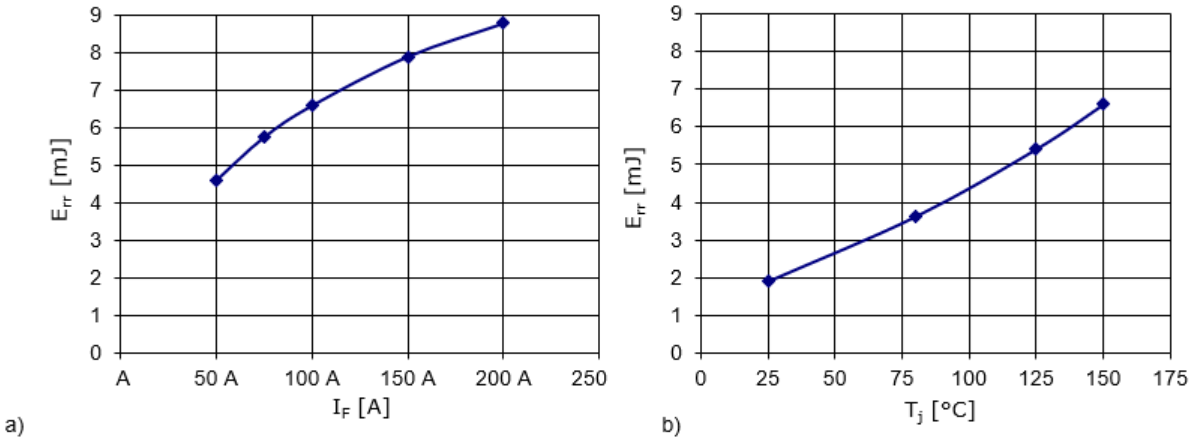


Figure 2.3.16 Dependencies of E_{rr} of a 100A/1200V CAL diode; a) on I_F (@ R_G=1Ω, 600V, 150°C); b) on T_j (@ 100A, 600V, R_G=1Ω)

Dynamic ruggedness

Apart from soft switching behaviour, an equally important requirement for freewheeling diodes for a voltage of 1000V and above is dynamic ruggedness. Figure 2.3.14 a) shows that almost the entire DC link voltage is taken up by the diode while it is still conducting a substantial tail current. If the IGBT is switched very steeply (low gate resistance R_G, small Miller capacitance C_{GC}) the reverse peak current and tail current will rise, at the same time causing a faster decrease in V_{CE} at the IGBT, which is then present in the diode with a correspondingly higher dv/dt. The electric field can only spread within the depleted area (t_2 – t_4 in Figure 2.3.12); here, extreme field intensities occur and avalanche breakdown in the semiconductor at voltages far below reverse voltage level (dynamic avalanche) are inevitable. Dynamic ruggedness is the ability of a diode to manage high rates of rise of commutation current di/dt and a high DC link voltage at the same time. An alternative to dynamic ruggedness would be to limit the di/dt and dv/dt of IGBT or to limit the maximum peak reverse recovery current of the diode, which amounts to the same. This will inevitably result in higher switching losses and a restricted area in the RBSOA of the diode.
While the space charge region spreads, the empty part of the n^--region will have a current I_R flowing through it. Electrons and holes are generated at the pn-junction by dynamic avalanche. The holes move through the highly doped p-region. The electrons, however, move though the n^--region, resulting in the following effective doping:

$$N_{eff} = N_D + p - n_{av}$$

Here, n_{av} is the density of the electrons generated by dynamic avalanche, moving from the pn-junction through the space charge region. The electrons partly compensate the hole density, thus counteracting the avalanche effect. With small forward currents, the reverse current will also decrease and consequently the hole density p. However, since the switching components have a higher dv/dt at low currents, the stress caused by dynamic avalanche may be higher, especially for small currents.

Silicon carbide (SiC)-Schottky diodes

If a Schottky barrier diode is used, the measured current during diode turn-off (I_f) consists of only capacitive current caused by C_j [2.19]. A hybrid IGBT + SBD module in the SEMITRANS 3 package (SKM200GB12T4SiC2) was used for the measured curves in Figure 2.3.17.

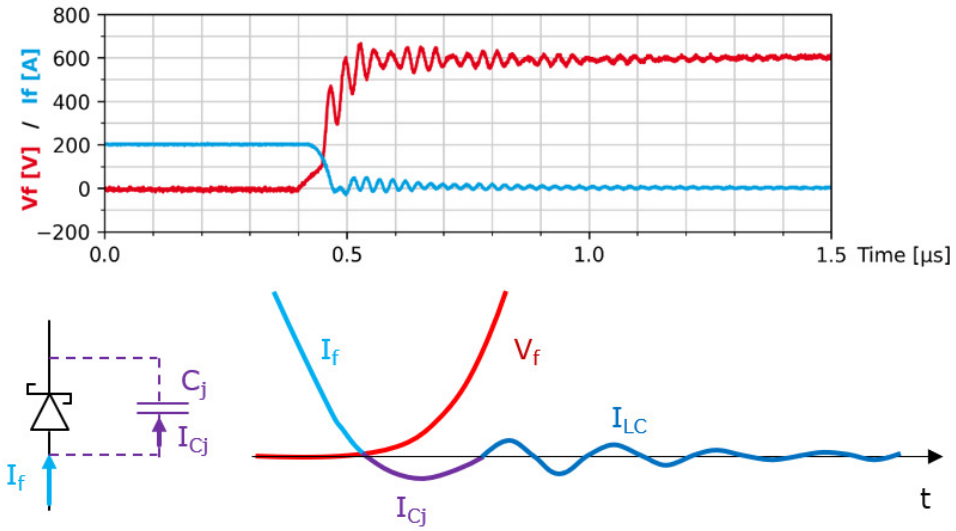


Figure 2.3.17 Turn-off of a Schottky diode with pure capasitive current [2.19]

Only the Schottky diode is used during diode turn-off. The parallel IGBT is kept off safely by negative gate voltage. Some current caused by the recharging of the junction capacitances of the IGBT and SBD is still present and some ringing due to the capacitance in series to stray inductances. This ringing is simply a product of the parasitics and is not caused by recombination within the chip. Therefore, no E_{rr} can be specified in datasheets. These oscillations do not generate heat within the diode, aside from the resistive losses in the conductors of the circuit (damping resistivity of the RLC network).

2.4 IGBT

2.4.1 Structure and functional principle

IGBT (**I**nsulated **G**ate **B**ipolar **T**ransistors) are typically designed in unit cell structures which where parallelized. Until generation 4 these units were for instance built as diamond structures in a density of up 50.000 cells per mm^2 (1200V IGBT) with a chip surface of 0.1 to 1.5cm^2 (Figure 2.4.1).

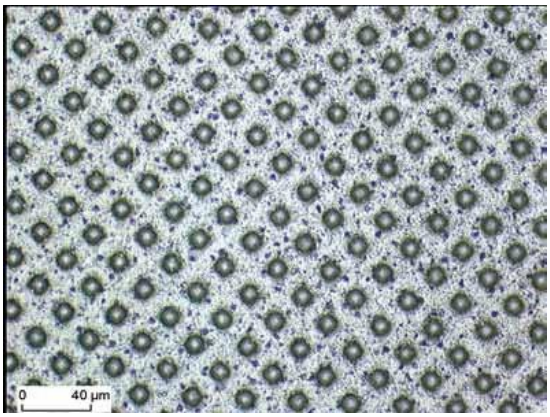


Figure 2.4.1 Cell structure (emitter metallisation) of a Trench IGBT3

For transistors based on the same technological concepts, the control regions of IGBT cells have an almost identical structure. As shown in Figure 2.4.2, p-doped wells are embedded in an n^--region which has to take up the space charge region during off-state. Their doping is low in the edge areas (p^-) and high in the centre (p^+). These wells contain areas which are n^+ doped, they are connected to the aluminium-metallised emitter (IGBT) electrode. A control region (gate) is embedded in a thin SiO_2 insulation layer above the n^+ regions, typically a n^+ doped polysilicon layer.
In power electronics, the vertical structure depicted in Figure 2.4.2 is used. Here, the load current of each cell is conducted vertically through the chip outside the channel. This manual only describes transistors of the n-channel enhancement type used almost exclusively), where a

conducting channel with electrons as charge carriers (majority carrier) is formed in a p-conducting silicon material when a positive control voltage is applied. Without a control voltage, these components would block (self-blocking transistors).

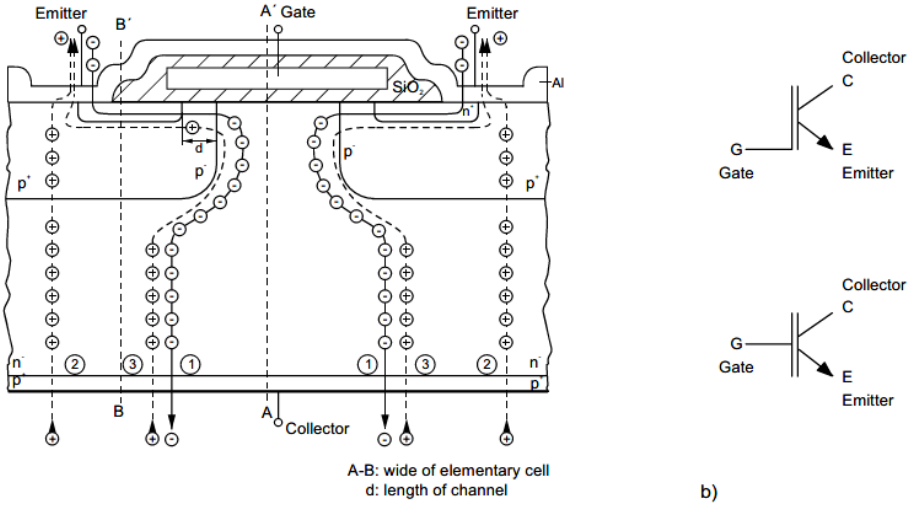


Figure 2.4.2 IGBT with vertical structure and planar gate; a) Charge carrier flow in on-state; b) Circuit symbols

When a sufficiently high positive control voltage is applied between gate and emitter at the IGBT, an n-conducting channel is formed within the p-region below the gate terminal. This channel conducts electrons from the source or emitter through the n^--drift area to the bottom terminal, where they deplete the charge carrier region.
While the structure of an IGBT is based in principle on a power MOSFET besides the n^--region, the lower side of the IGBT consists of a p^+-conducting area carrying the collector terminal. The effect of this additional n^+ field stop layer located (in most IGBT concepts) between the n^-- and p^+ region will be discussed in more detail later.
As soon as electrons enter the p^+ area of the collector region, positive charge carriers (holes) will be injected from the p^+ area to the n^- area. The injected holes will flow directly from the drift area to the emitter-p-contact, as well as laterally below the channel and the n^+-well to the emitter. Thus, the n^--drift area is flooded with holes (minority carriers); this charge carrier enhancement conducts the biggest part of the main current (collector current). The main current depletes the charge carrier region, which results a decline in collector-emitter voltage. This means that IGBTs are bipolar components.
The flood of minority carriers in the high-resistance n^- region causes a lower on-state voltage of the IGBTs compared to power MOSFETs. For this reason, IGBTs can be designed for much higher currents at higher blocking voltages. On the other hand, the minority carriers must be dissipated from the n^- drift area again during turn-off, or they must recombine there (switching losses).
The p-storage charges Qs, which recombine during turn-off in the n^- region, have an almost linear characteristic in the low-current range and rise with a square root function in the rated current and overcurrent range in accordance [2.20].

$Qs \sim I^{0.8...1}$	in the lower on-state current range
$Qs \sim I^{0.5}$	in the rated and overcurrent range
$Qs \sim V_{(BR)CE}{}^{2...2.7}$	

Storage charge enhancement and depletion processes cause switching losses, storage effects (storage time) and a collector "tail current" during turn-off. In practice, IGBT properties are strongly influenced by the parasitic elements in the real IGBT structure. To understand these real properties and possible failure mechanisms, it is therefore indispensable to look at the equivalent circuit diagram of the IGBT (Figure 2.4.3).

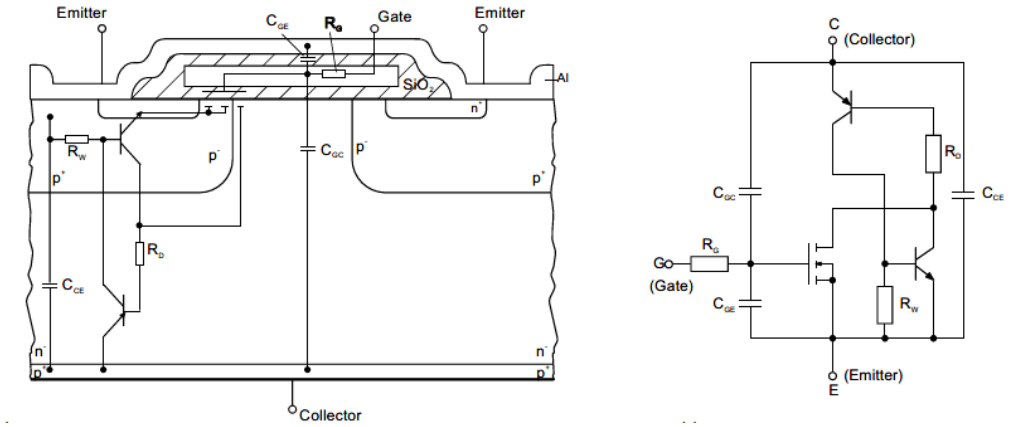


Figure 2.4.3 IGBT cell (NPT structure, planar gate) including the key parasitic elements; a) Parasitic elements in the cellular structure; b) Equivalent circuit diagram with parasitic elements

The physical causes and designations of the parasitic capacitances and resistances shown in the Figure above are evident in Table 2.4.1

Symbol	Designation	Physical Description
C_{GE}	Gate-emitter capacitance	Overlapping gate and source metallisation; dependent on gate-emitter voltage; independent of collector-emitter voltage
C_{CE}	Collector-emitter capacitance	Junction capacitance between n^--drift area and p-well; dependent on cell surface, breakdown voltage and drain source voltage
C_{GC}	Gate-collector capacitance	Miller capacitance; generated by overlapping of gate and n^--drift area
R_G	Internal gate resistance	Polysilicon gate resistance; additional series resistors are often needed in modules with several transistor chips to minimise oscillations between chips
R_D	Drift resistance	Resistance of the n^--region (base resistance of the PNP transistor)
R_W	Lateral resistance of the p-well	Base-emitter resistance of the parasitic bipolar NPN transistor

Table 2.4.1 Physical causes and designations of IGBT parasitic elements

Apart from internal capacitances and resistances, the equivalent circuit diagram of the IGBT also shows an "ideal MOSFET", an NPN transistor at the gate side: n^+ emitter region (emitter) / p^+ well (base) / n-drift area (collector) with the lateral resistance of the p^+ well below the emitters as base/emitter resistance R_W and - in the sequence p^+-collector area (emitter) / n^- drift area (base) / p^+ well (collector) - a PNP transistor, which, in combination with the NPN transistor, forms a thyristor circuit. This parasitic thyristor will latch up as soon as the following latch-up condition is met:

$M \cdot (\alpha_{npn} + \alpha_{pnp}) = 1$ where $\alpha_{pnp}, \alpha_{npn} = \alpha_T \cdot \gamma_E$

M: multiplication factor;

$\alpha_{npn}, \alpha_{pnp}$: current amplification in the individual transistors in the base circuit;

α_T: base transport factor;

γ_E: emitter efficiency

This would lead to a loss of IGBT controllability and, consequently, to its destruction. In principle, this can happen during stationary operation (when a critical current density is exceeded, which decreases as the chip temperature rises) or even during turn-off (dynamic latch-up due to the increased hole current compared to stationary on-state operation). Appropriate design measures will reliably prevent latch-up in all modern IGBT types under any permissible static and dynamic operating conditions; latch-up would only happen during turn-off if the rated current density was multiplied in value.

Suitable design measures are, for example, the reduction of the base-emitter resistance R_W of the npn-subtransistor by way of high doping of the p^+ well directly below the n-emitters and shortening of the n-emitter length to such an extent that the threshold voltage of the base-emitter diode of the

npn-transistor cannot be reached under any permissible operating condition. Furthermore, the hole current (npn-transistor base current) is kept at a minimum by setting a low-current amplification in the pnp-transistor. In the end a compromise has to be found between switching behaviour and ruggedness, as well as the on-state behaviour.

2.4.2 Static behaviour

Figure 2.4.4 shows the output characteristics of an IGBT with an anti-parallel freewheeling diode and its transfer characteristic.

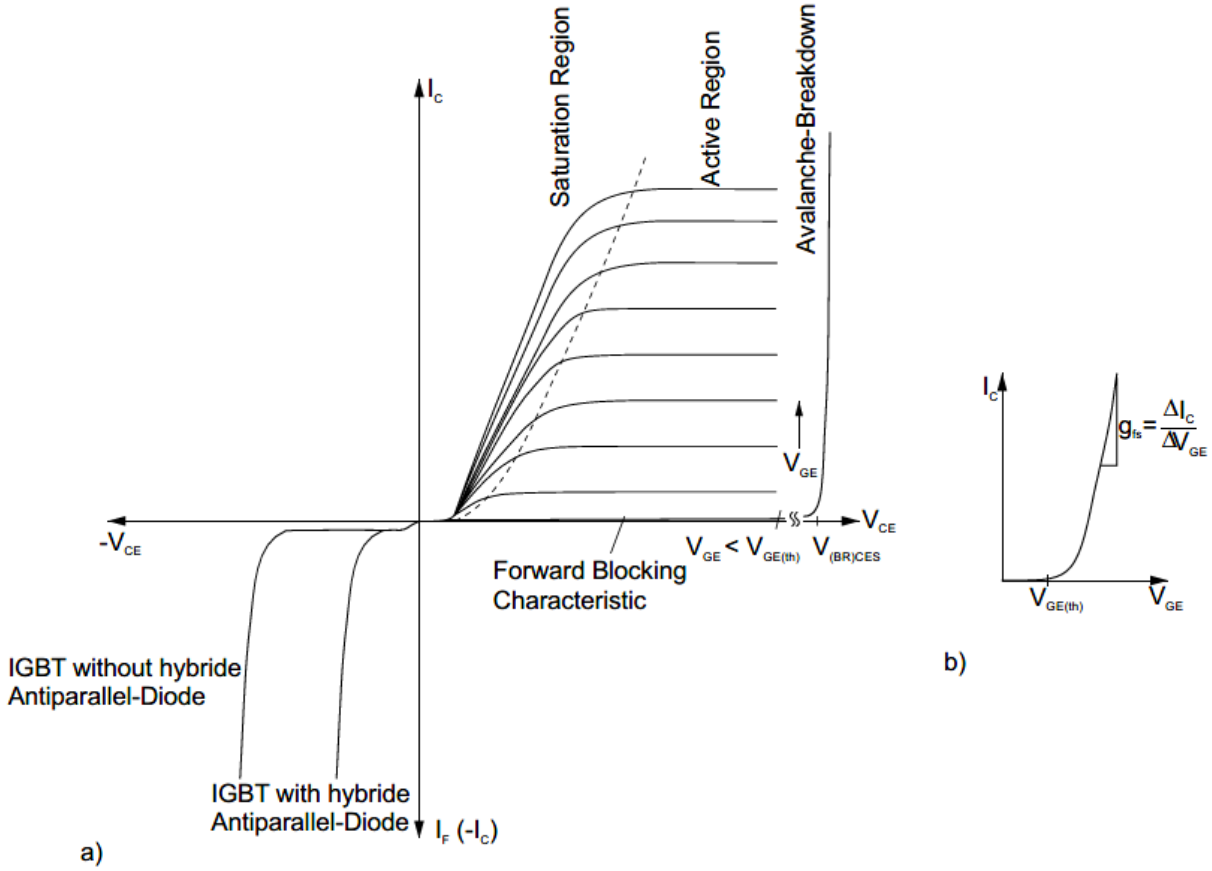


Figure 2.4.4 a) Output characteristics of an IGBT (n-channel enhancement type); b) Transfer characteristic $I_C = f(V_{GE})$

The stationary switching states are as follows:

Forward off-state and avalanche breakdown

If a positive collector-emitter voltage V_{CE} and a gate-emitter voltage V_{GE} is applied below the gate emitter threshold voltage level $V_{GE(th)}$, only a very small collector-emitter cut-off current I_{CES} flows between the collector and emitter terminal.
When V_{CE} rises, I_{CES} increases slightly at first. Above a specified, maximum rated collector-emitter voltage V_{CES}, there will be an avalanche breakdown of the pin-junction p^+-well / n^--drift area / n^+-epitaxy layer (collector-emitter breakdown voltage $V_{(BR)CES}$). $V_{(BR)CES}$ roughly corresponds to the breakdown voltage V_{CER} of the bipolar pnp-transistor in the IGBT structure. The multiplication current generated during avalanche breakdown in the collector-base diode can lead to IGBT destruction as a result of bipolar transistor turn-on. Base and emitter regions are almost shorted by emitter metallisation; between them there is nothing but the lateral resistance of the p^+-well.

On-state (1st quadrant)

The forward on-state at a positive collector-emitter voltage V_{CE} and positive collector current I_C comprises two characteristic curve areas:

Active region
With a gate-emitter voltage V_{GE} that hardly exceeds the gate-emitter threshold voltage $V_{GE(th)}$, a relatively high voltage share will be depleted through the channel, due to current saturation (horizontal part of the output characteristics). The collector current I_C is controlled by V_{GE}.

As a measure for the transfer behaviour as described in Figure 2.4.4 b) the forward transconductance g_{fs} is defined as

$$g_{fs} = \frac{\Delta I_C}{\Delta V_{GE}} = \frac{I_c}{V_{GE} - V_{GE(th)}}$$

Forward transconductance rises in proportion to the collector current I_C and the collector-emitter voltage V_{CE} and falls as the chip temperature increases. In the switching mode that is exclusively permissible for power modules working with several IGBT chips connected in parallel, the active region is only run through during turn-on and turn-off. Stationary module operation in the active region is not permissible, because $V_{GE(th)}$ falls when the temperature rises, meaning that even small differences between the individual chips may cause thermal instability.

Saturation region
The saturation region, which corresponds to ON-state during switching operations (steep part of the output characteristics) has been reached when I_C is solely determined by the outer circuit. The on-state behaviour is characterised by the residual voltage $V_{CE(sat)}$ (collector-emitter saturation voltage) of the IGBT. Flooding the n^- drift area with minority carriers causes the saturation voltage of an IGBT - from a certain reverse voltage level on - to be far lower than the on-state voltage of a comparable MOSFET. In the majority of modern IGBT structures, $V_{CE(sat)}$ rises in proportion to the temperature; only for IGBT designed according to the PT concept will $V_{CE(sat)}$ decline in the rated current range as the temperature increases.

Inverse operation (3rd quadrant)

In inverse operation, the pn-junction at the collector side of a standard IGBT is poled in reverse direction. The permissible blocking voltage of this PIN diode is no more than a couple of 10 volts due to various design conditions and the design of the chip edges. Existing reverse blocking RB-IGBT use a special p+ layer and p+ isolation barrier to achieve higher blocking voltages. In the past reverse-blocking IGBT modules had been equipped with fast diode in series-connection. This type of IGBT are often used antiparallel as bidirectional switches e.g. in Matrix converters or AC switches. Reverse-conducting IGBT modules used in standard applications are equipped with fast, anti-parallel diodes (inverse diodes). Thus, the on-state features of IGBT modules in inverse operation exclusively result from the properties of these hybrid inverse diodes. Chapter 2.4.4 contains information on the in reverse-conducting RC-IGBT chips with included diode structure in one chip.

2.4.3 Dynamic behaviour

The dynamic or switching behaviour of IGBT power modules is determined by their structural, internal capacitances and the internal and outer resistances. Contrary to the ideal of powerless voltage control via the MOS-gate, frequency-dependent control power is required because of the recharge currents of the internal capacitances which are needed for switching.
Furthermore, the commutation processes are affected by the parasitic inductances present in the components and connections and generated by connecting transistor chips in power modules; they induce transient overvoltage and may cause oscillations due to the circuit and transistor capacitances, cf. chapter 9.
The switching behaviour of IGBT can be described as resulting from the transistors internal capacitances and resistances:
When the IGBT is turned off, C_{GC} is low and approximately equal to C_{CE}. During on-state, C_{GC} will increase rapidly as soon as the gate-emitter voltage has exceeded the collector-emitter voltage; this rapid increase is due to inversion in the enhancement layer below the gate regions.
The datasheets normally list the input and output capacitances C_{ies}, C_{res} and C_{oes} (low-signal capacitances) of the transistor in OFF state (see Table 2.4.2).

	IGBT
Input capacitance	$C_{ies} = C_{GE} + C_{GC}$
Reverse transfer capacitance (Miller capacitance)	$C_{res} = C_{GC}$
Output capacitance	$C_{oes} = C_{GC} + C_{CE}$

Table 2.4.2 Definition of the low-signal capacitances of an IGBT

To calculate the switching behaviour, this data can only be utilised to a very limited extent, since the input and reverse transfer capacitance ($V_{CE} < V_{GE}$) will increase enormously in a fully switched transistor, for example. To determine switching times and the gate charge by approximation, the

gate charge diagram included in the datasheets, as shown in Figure 2.4.6, is used (for explanations please refer to chapter 7.3.3).
Below, the IGBT switching behaviour when "hard" switching ohmic-inductive loads with continuous load current - i.e., the time constant of the load L/R is far greater than the cycle 1/f of the switching frequency - is looked at from a qualitative point of view.
Figure 2.4.5 a) shows the typical waveforms of collector current and collector-emitter voltage as a function of the gate control voltage V_{GE}, Figure 2.4.5 b) shows the typical waveform of the operating point for hard turn-on and turn-off as a graph $i_c = f(v_{CE})$. Since the behaviour of power MOSFET deviates from this in very few respects only, Figure 2.4.5 b) refers to both components.
Typical for "hard switching" mode is that during turn-on and turn-off, both transistor current and transistor voltage are high for a short time; this is since a freewheeling diode in the load circuit prevents the current from cutting off because of the load inductance:

- When the transistor is turned on, the freewheeling diode can only pick up reverse recovery voltage (turn off) once the load current has completely commutated to the transistor. The collector current therefore has to reach the load current level before the collector-emitter voltage can fall to the on-state value.
- When the transistor is turned off, the freewheeling diode can only take the load current (turn on) once it has reached on-state voltage polarity. To this end, the collector-emitter voltage has to exceed the commutation voltage level before the collector current can drop to the cut-off current value.

In contrast to thyristors of any type, transistors can handle such modes of operation without passive snubber circuits thanks to the "dynamic" junction which is generated in the drift area during switching operations.
In a transistor, however, a considerable amount of switching energy is dissipated:

$$E_{on}, E_{off} = \int_{t_{on}, t_{off}} v \cdot i \, dt$$

By means of passive snubber circuit (which are rarely used nowadays), the operating point curve can be brought closer to the axes. Switching losses are "shifted" from the transistor to the snubber, causing the total efficiency to decrease in most cases.
Since the "widest" possible operating point waveform is influenced by many (non-ideal) effects in the transistor and not just by current/voltage markers and switching time, the SOA (Safe Operating Area) is given in the datasheets for different operating conditions (cf. chapter 7.3.4).
Apart from the non-ideal properties of transistors and diodes, passive circuit components also influence switching losses and operating point waveforms to a high degree. Their impact will be discussed in chapter 9 in more detail.

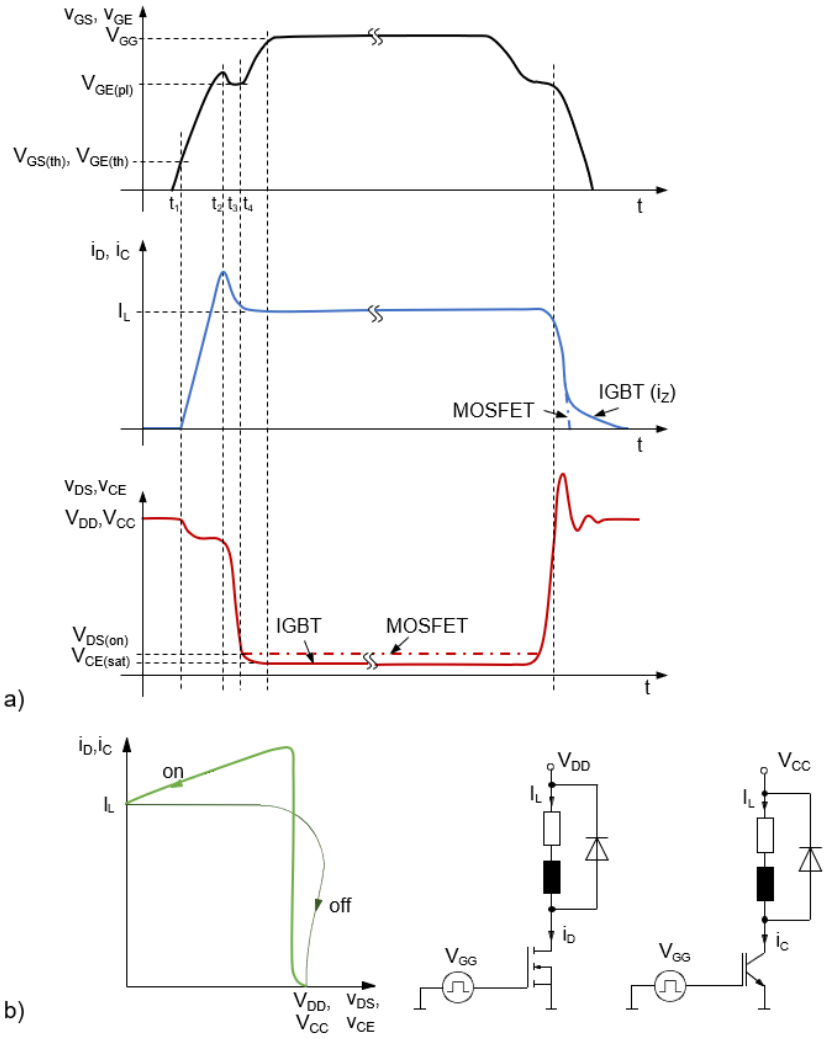


Figure 2.4.5 Typical "hard" switching behaviour of power MOSFET and IGBT (ohmic-inductive load with freewheeling circuit); a) Current and voltage waveforms; b) Operating point waveforms and measurement circuit

As shown in Figure 2.4.5, the collector-emitter voltage declines within some 10ns to a value that is equivalent to the voltage drop over the n^--drift area when the IGBT is turned on. Then the n^--area is flooded by positive charge carriers from the p-collector region; after a period ranging from several hundred ns to some µs, the dynamic saturation voltage $V_{CE(sat)dyn}$ will have dropped to the value of the on-state voltage $V_{CE(sat)}$.

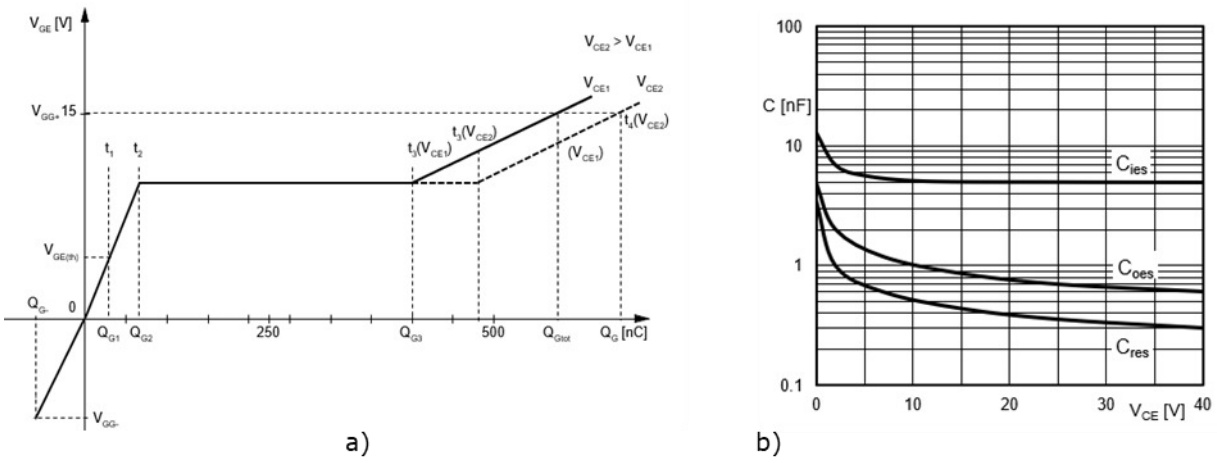


Figure 2.4.6 a) Gate charge diagram of an IGBT; b) IGBT low-signal capacitances

Turn-on: switching interval 0...t_1 (blocked transistor)

The gate current i_G starts flowing when the control voltage is applied.
At first, i_G charges only the gate capacitance C_{GE} until it reaches the charge quantity Q_{G1}; the gate-emitter voltage V_{GE} rises in line with the time constant determined by the input capacitance of the IGBT and the gate resistance. Since V_{GE} is still below the threshold voltage $V_{GE(th)}$, no collector current will flow during this period.

Turn-on: switching interval t_1...t_2 (collector current rise)

After the threshold voltage $V_{GE(th)}$ (t_1) has been reached, the collector current will start to rise. In the same way, V_{GE}, which is coupled to the collector current in the active IGBT operating area by means of the transconductance g_{fs} with $I_C = g_{fs} \cdot V_{GE}$, increases until it reaches $V_{GE1} = I_C/g_{fs}$ (time t_2). Since the freewheeling diode can only block the current at t_2, V_{CE} does not drop significantly before t_2. At $t = t_2$, charge Q_{G2} will have flowed into the gate.
During this time interval, most of the turn-off losses are generated in the IGBT. This is because, as long as i_C is below the load current I_L, a certain share of I_L must continue to flow through the freewheeling diode. This is why, the collector-emitter voltage v_{CE} cannot drop noticeably below the operating voltage V_{CC}. The difference between V_{CC} and V_{CE} outlined in Figure 2.4.5 is mainly caused by transient voltage drops across the parasitic inductances of the commutation circuit.

Turn-on: switching interval t_2...t_3 (transistor fully switched on in the active operating area, flat phase)

When the freewheeling diode is turned off, V_{CE} will almost drop to its on-state value $V_{CE(sat)}$ by t_3. Between t_2 and t_3, the collector current and gate-emitter voltage are still coupled through the transconductance; v_{GE} therefore remains roughly constant. While v_{CE} drops, the gate current i_G recharges the Miller capacitance C_{CG} with the charge (Q_{G3}-Q_{G2}). By $t = t_3$, an amount of charge equal to Q_{G3} will have flowed into the gate.
After the entire load current I_L has been commutated to the IGBT, the freewheeling diode will start to block. Due to the reverse recovery time of the freewheeling diode, however, the IGBT collector current i_C initially continues to rise above I_L during turn-off of the freewheeling diode by a value equal to I_{RRM} and dissipates the reverse recovery charge Q_{rr} of the freewheeling diode (cf. definitions on switching times and explanations on characteristics I_{RRM}, Q_{rr} and E_{rr} relating to inverse diodes, as provided in chapter 7.3).

Turn-on: switching interval t_3...t_4 (saturation area)

At t_3, the IGBT is now turned on, its operating point has passed through the active operating area and has reached the border of the saturation area. V_{GE} and I_C are no longer coupled by g_{fs}. The charge quantity (Q_{Gtot} -Q_{G3}) now supplied to the gate, causes the further rise in V_{GE} up to the level of the gate control voltage V_{GG}. Immediately after its steep drop, the collector-emitter voltage v_{CE} has not yet reached its static on-state value V_{CEsat}. Depending on V_{GG} and I_C, this value will be reached as soon as the n- drift area starts to be flooded after several hundred nanoseconds or several microseconds. This "dynamic saturation phase $V_{CE(sat)dyn} = f(t)$" is the period required for (bipolar) minority charge carrier flooding (conductivity modulation) of the wide n^--region of the IGBT.

Turn-off

During the turn-off operation, the processes described above are reversed: charge Q_{Gtot} must now be dissipated from the gate with the aid of the gate current. In this process, the internal capacitances are recharged to such an extent that the charge carrier influence in the channel area will vanish. This helps to quickly reduce any neutrality interference in this area; the collector current drops steeply to begin with. After the emitter current has stopped, however, many p-charge carriers generated by injection from the IGBT collector area are still present in the n-drift area. They must now recombine or be reduced to zero by backward injection, which causes a collector tail current. Since this current tail will only decline within µs after the collector emitter voltage has started to rise, its shape and length significantly determine the turn-off losses of the IGBT during hard switching.
Overshooting of v_{CE} over V_{CC}, which was indicated in Figure 2.4.5, results mainly from the parasitic inductances in the commutation circuit. It grows in proportion to the increasing turn-off speed–di_C/dt of the IGBT. The more the transistor application deviates from the "ideal" case of a "hard switch" discussed here (e.g., due to parasitic components in the commutation circuit), the more "blurry" the step-form of the gate-emitter curve becomes. The intervals "decoupled" during hard switching will then merge more and more, and any description of the switching behaviour becomes more complex.

2.4.4 Technologies, trends and development

Since the IGBT basic concept was invented, the principles have been utilised in different novel concepts. IGBTs have therefore been further developed in separate ways, pursuing the objectives and taking the directions outlined for chip technology in chapter 1.2. In order to both reduce costs by reducing (shrinking) chip area and to get even closer to the physical limits, three main paths have been followed in the further development of IGBT:

- Finer cell structure / chip area reduction / increase in max. current density
- Reduced chip thickness
- Increase in permissible chip temperature

Every IGBT concept must – adapted to its main applications – achieve a balance between various conflicting component properties, as shown in the example in Figure 2.4.7:

- Between on-state voltage $V_{CE(sat)}$ and turn-off power loss E_{off},
- Between on-state voltage $V_{CE(sat)}$ and short-circuit behaviour).

The limits for a) are pushed further in the latest IGBT concepts, e.g., IGBT7 (Infineon), RGA (Rohm) and M7 (Mitsubishi), by increasing the concentration of free charge carriers among the n-emitter cells. One negative consequence, however, is often the very steep decline in collector current during turn-off with the resultant side-effects as regards EMC, for instance. The trade off in b) is improved by a continuous reduction in chip thickness and the introduction of weakly doped field stop layers. The IGBT cell pitch has a crucial impact on its properties. This determines, among other things, the influence the MOS channel has on conductivity modulation.
Figure 2.4.7 [2.21] shows, using the example of a 1200 V IGBT in Trench-Gate technology, how $V_{CE(sat)}$ or collector current density $J_{C(sat)}$ depend on the cell pitch (distance between adjacent gate centres) for T_j = 125°C.

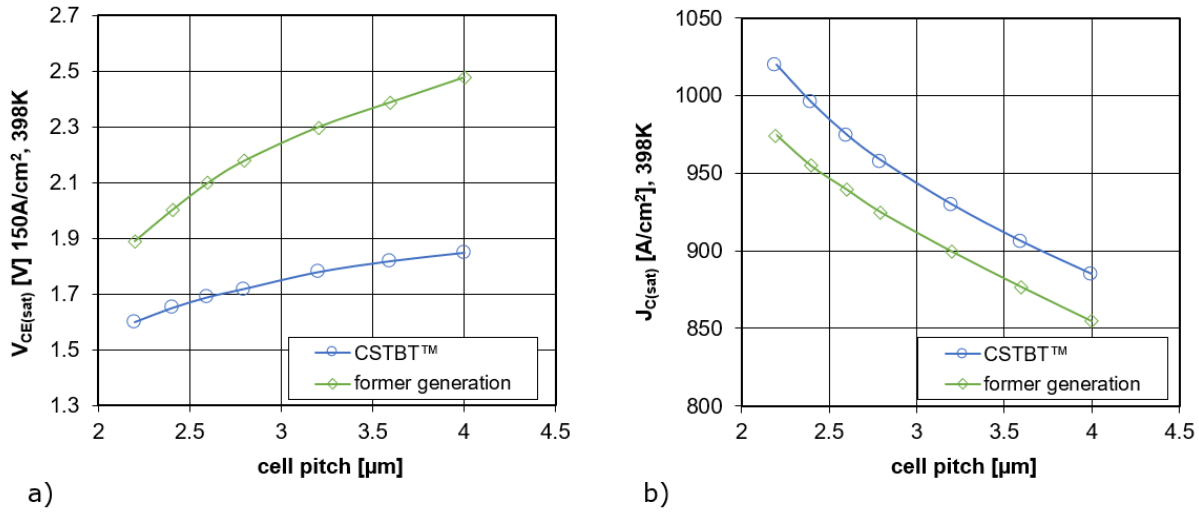


Figure 2.4.7 a) Dependency of the on-state voltage $V_{CE(sat)}$ of a 1200 V IGBT on the cell pitch for T_j = 125°C; b) Dependency of the collector current density $J_{C(sat)}$ of a 1200 V IGBT on the cell pitch for T_j = 125°C [2.21]

Figure 2.4.8 shows the development of chip size and on-state voltage for different component generations using 1200 V / 75 A IGBT chips from Infineon as an example.

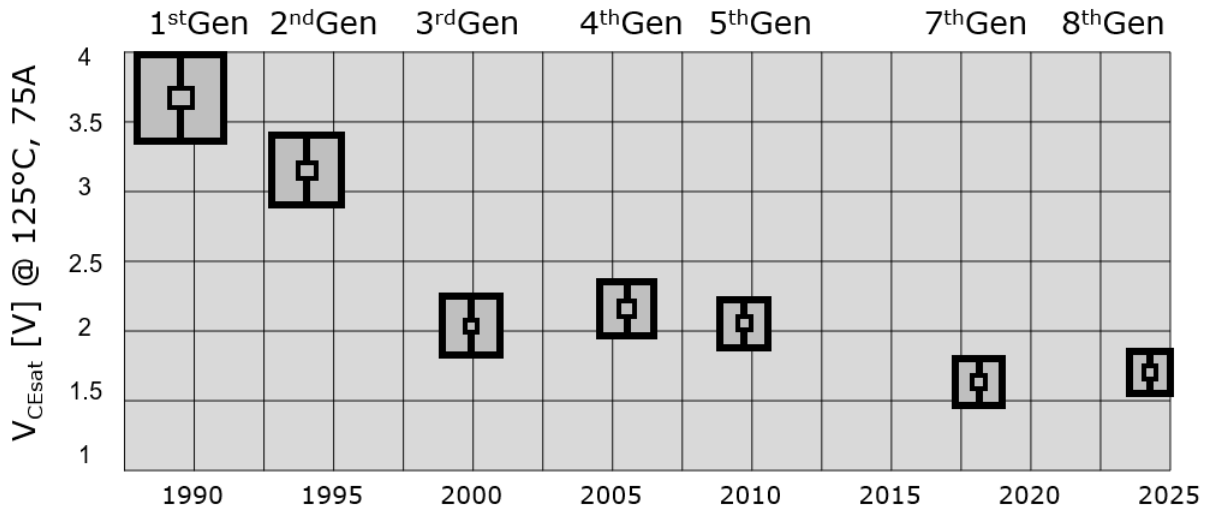


Figure 2.4.8 Development of chip size and on-state voltage of 1200 V / 75 A IGBT chips from Infineon (see also [2.22])

To enable system costs (cooling, chip area) to be reduced, a crucial development target is to increase the permissible chip temperature. This was achieved by Infineon, for example, for IGBT up to 1700 V in the IGBT4 chip generation, raising the temperature from 150°C to 175°C; 200°C is planned for future IGBT generations. An increase in the IGBT operating temperature, however, means that the freewheeling diode (inverse diode), too, has to be suitable for this temperature; this is increasing the requirements that IGBT module packaging has to fulfil.
The pictures below illustrate the most important IGBT concepts in development history, which shall be briefly described below. Detailed explanations on the physical correlations are provided in [2.16].

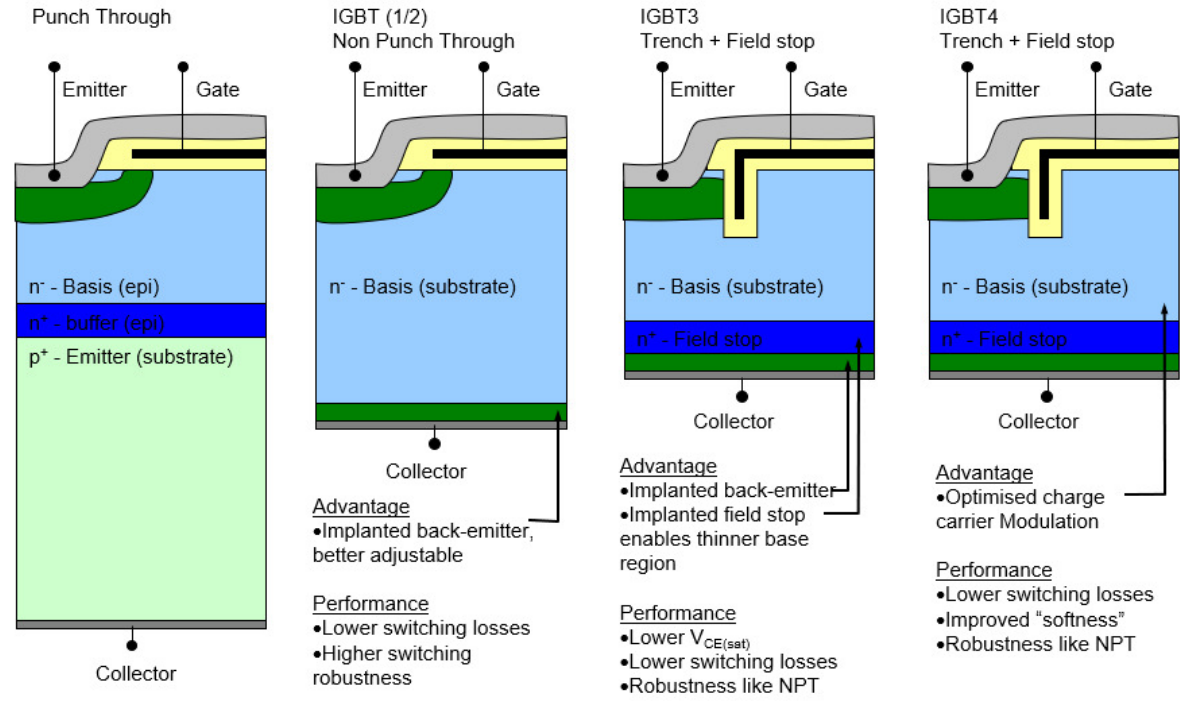


Figure 2.4.9 IGBT concepts, basic properties and off-state field intensity characteristics (acc. to [2.23])

PT concept

The first "Punch Through" (PT) concept, which is still used today as a result of continuous developments, uses a p^+-substrate as a base material, n^+ and n^- region being applied by means of epitaxy. Today, PT-IGBT can also have a trench-gate structure, as shown in Figure 2.4.9. In forward

off-state, the space charge region comprises the entire n^--region. In order to keep the epitaxy layer as thin as possible even for high blocking voltages, the field at the end of the n^- drift area is reduced by a highly doped n^+ buffer region.
PT-IGBT have a high emitter efficiency for holes in the p^+ layer drifting into the n^- drift area, because the substrate is relatively thick and highly doped. The PNP current gain has to be reduced via the base transport factor (n^- drift area, n^+ buffer), which is achieved by reducing the charge carrier lifetime in the n^+ layer by increasing the recombination centres (e.g., gold doping or electron beam radiation). The hole current amounts to 40...45% of the total current.

NPT concept

The basis of "Non Punch Through" (NPT) IGBT, which was utilized by numerous manufacturers, is a thin, weakly doped n^- wafer; the collector-side p^+ zone is created by way of back implantation. Here, the n^- drift area is so wide that in forward off-state, the electric field is fully depleted in the n^- drift area up to the maximum permissible off-state voltage and cannot – in contrast to the PT concept – spread over the entire n^- region.
NPT-IGBTs have a very thin collector-side p^+ emitter region, which results in a low emitter efficiency ($\gamma_E = 0.5$) of the pnp-subtransistor - it is not necessary to lower the base transport factor by reducing charge carrier lifetime. The hole current amounts to 20...25% of the total current. In contrast to PT-IGBT, the saturation voltage of NPT-IGBT has a positive temperature coefficient, improving both the current symmetry between the cells in single chip and between chips connected in parallel. Switching times for hard switching are comparatively shorter and less dependent on temperature; overcurrent can be better cut off as a result of improved internal current limiting. An example for this technology node is IGBT2 generation, which was used in older NPT-IGBT product series.

NPT concept with field stop layer and trench-gate structure

For these very common IGBT chips, a field stop layer was added to the NPT concept and the planar gate was replaced by a vertical trench-gate structure (Figure 2.4.9).
The basis here continues to be a thin, weakly doped n^- wafer into which an additional n^+ region has been implanted as a field stop layer on the back above the p^+ region of the collector. This reduces the thickness of the drift area – like the highly doped n^+ buffer layer in the PT-concept – by diminishing the electric field at the end of the n^- drift area in front of the collector region. Since this layer needn't curb the high emitter efficiency as is the case in the PT-IGBT, but has to reduce the field intensity only, it is less highly doped than the n^+ buffer of the PT-IGBT.
With the same forward off-state voltage, the thickness w_B of the n^- drift area can be significantly reduced in comparison to an NPT-IGBT; this also considerably cuts the on-state voltage ($\sim w_B$) of the drift area. The positive temperature coefficient of the on-state voltage and the high component ruggedness are maintained. During turn-off, the tail current is initially somewhat higher than for an IGBT without field stop layer, but then it drops faster.
The vertical gate arrangement in the shape of a trench inside every IGBT cell allows for a vertical channel track in the p-well. Since the active silicon area is enlarged, better control of the channel cross-section is possible and thus a lower channel resistance can be obtained. For a given silicon area, the cell area can be reduced even further. This is why higher current densities, lower forward losses, a higher latch-up strength, lower switching losses and higher breakdown voltages can be obtained than in IGBT with planar gate structures.
In the IGBT4 generation from Infineon the cell pitch (i.e., the distance between the gates of neighbouring cells) was further reduced compared to its predecessor generation IGBT3, meaning that the cells were shrunk in size. Cell optimisation and chip thickness reduction has helped to improve the static and dynamic properties. However, smaller chips also mean a higher thermal contact resistance $R_{th(j-c)}$ or $R_{th(j-s)}$. The performance increase achieved in comparison to the IGBT3 therefore largely results from the higher permissible chip temperature of 175°C as compared with 150°C for IGBT3. Chips are available with different settings (“flavours”) between static and dynamic properties for different requirements:

- IGBT4 T4: particularly short switching times for modules with rated currents between 10A and 300A
- IGBT4 E4: low forward and switching losses for modules from 150A to 1000A
- IGBT4 P4: "soft" switching behaviour and particularly low forward losses for high-current IGBT modules above rated currents of 900A.

Plugged cells

Rather than bonding individual trench cells but short-circuiting the polysilicon in the gate area with the emitter metallisation instead (plugged cells) a further improvement in IGBT features can be achieved. Increasing the cell spacing and reducing the p-areas increases charge carrier concentration at the emitter, affecting the on-state voltage to a greater extent than the increased voltage drop over the channel area as a result [2.24]. Another advantage of plugged cells is the lower collector current in the event of a short circuit as compared to conventional Trench-IGBT.

RC-IGBT

Various manufacturers are developing reverse-conducting IGBTs which can be loaded with the same current density in IGBT and diode mode. These are known as Reverse Conducting IGBT (RC-IGBT). The aim is to reduce the use of anti-parallel freewheeling diode chips (hybrid connected in the module), which has the following advantages:

- Improved performance per module area
- Increased overload capability (surge withstand strength)
- Improved parallel switching capability
- Increased $R_{th(j-c)}$ diode/IGBT ratio
- Reduction in temperature ripples per chip
- Improved flexibility for optimum thermal properties in power module

Figure 2.4.10 shows the basic structure of an RC-IGBT using the SPT concept from ABB. In its basic structure, n^+ shorts have been integrated into the p^+ collector region. This enables the reverse conductivity of the integrated MOSFET to be used as an inverse diode.

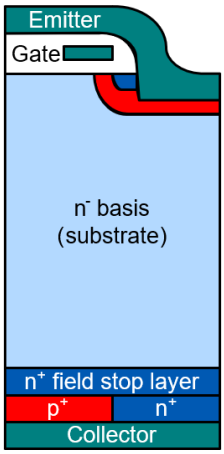


Figure 2.4.10 Structure of an RC-IGBT from ABB [2.25]

Hole injection from the p^+ collector region into the IGBT section also has to be ensured when voltages and currents are low. Various structural measures help to attain low turn-off losses and soft recovery behaviour in the diode across the entire temperature range; IGBT latch-up is prevented. For this purpose, it is necessary to set very precise doping profiles for the p-emitter regions and the p^+/n^+ collector regions. The cells are thus not designed with highly doped p^+ regions but a fine structure of p-regions in order to obtain a lower injection efficiency. Local control of the p-charge carriers by means of implantation or proton irradiation allows for diode turn-off losses to be reduced without affecting the blocking voltage and the IGBT losses too much. Another way of reducing diode turn-off losses is to introduce a MOS-controlled diode (Bimode Insulated Gate Transistor BIGT). Nowadays, RC-IGBT with blocking voltages of between 600 V and 3300 V are set to go into production. There is still a lot of room for improvement, especially in diode turn-off behaviour.

MPT (Micro Pattern Trench) Technology

The latest generation of IGBTs, i.e. generation 7 and 8 are taking benefit of the so called MPT (**M**icro **P**attern **T**rench) technology. The design concept is no longer based on small square singular IGBT cells, in fact it is utilizing long trench gate structures, as depicted in Figure 2.4.11.

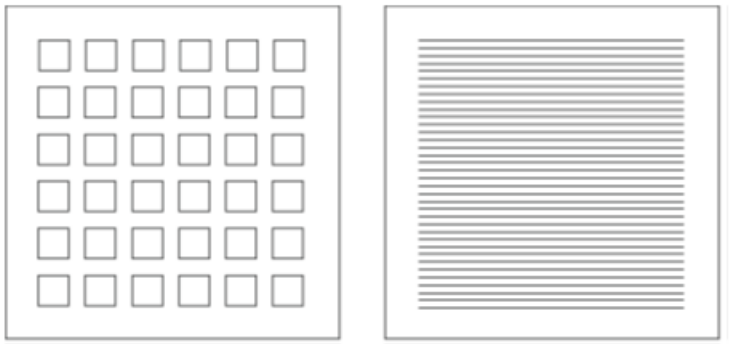


Figure 2.4.11 Schematic of a) square cell concept and b) Micro Pattern Trench (MPT) cell concept [2.27]

One of the core principles to support the MPT concept is the IE (**I**njection **E**nhancement) principle. This principle was first introduced in the early 1990s [2.26]. The aim was to improve the carrier distribution in the IGBT similar to a Thyristor. The potential was shown directly to improve the forward current density by a factor of 10. The idea was to suppress the flow holes near the emitter side of the IGBT. Therefor a deep trench gate topology (D) under the channel is needed and the distance to the next cell (w/2) has to be as small as possible (see Figure 2.4.12).

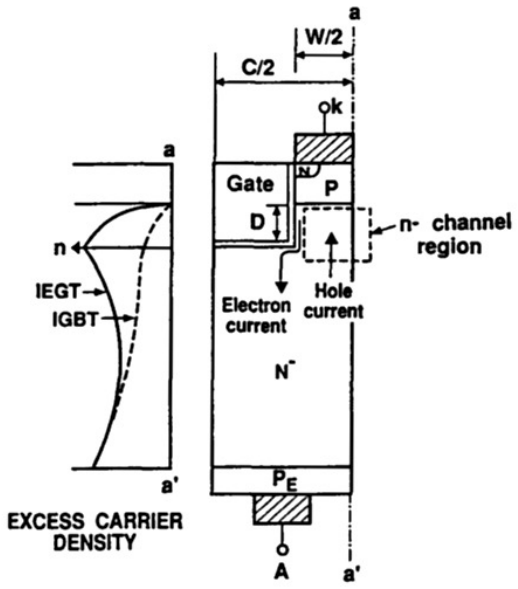


Figure 2.4.12 Sketch of the basic structure with design parameters [2.26]

The influence of the design parameters on the hole current is described in the following relation:

$$J_h = 2 \cdot k \cdot T \cdot \mu_h \cdot n_k \cdot \left(\frac{W}{D}\right)$$

Besides the before explained design parameters W and D, is n_k the carrier density at the emitter (cathode) side and μ_h the hole mobility. On the other hand the electron flow is not restricted by geometry. The injection efficiency $\Gamma_{h,K}$ of the holes can be described via the following equation:

$$\Gamma_{h,K} = \frac{J_h}{J \cdot C} = \frac{2 \cdot k \cdot T \cdot \mu_h \cdot n_k \cdot W}{D \cdot C \cdot J}$$

$$\text{with } J = \frac{J_h + J_e}{C}$$

Here the design parameter C, which is the cell width (see Figure 2.4.12), plays together with W and D an important role. If these three design parameters are adjusted that way, that (1- $\Gamma_{h,K}$) is near unity, a carrier distribution similar to a thyristor can be achieved [2.26].
The IE principle was partly used in generation 4, but is consequently utilized since generation 7, see Figure 2.4.13.

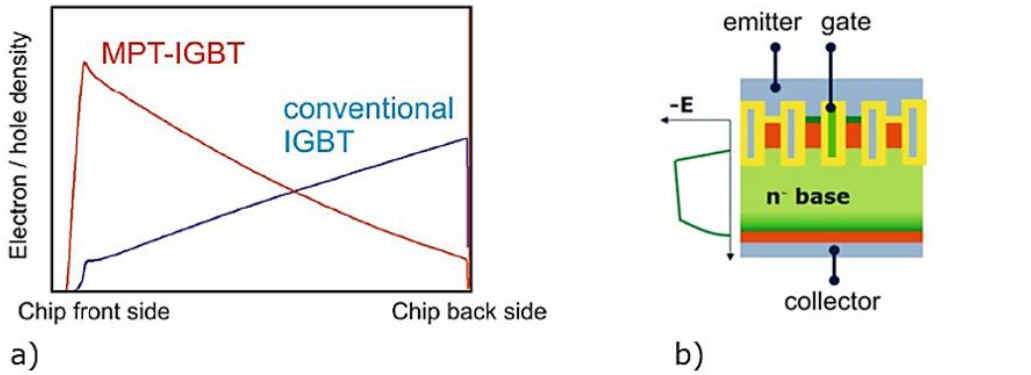


Figure 2.4.13 a) comparison of carrier densities in a MPT and in a conventional IGBT, b) sketch of a MPT cell in cross section [2.27]

Due to the fact that the design parameter D can only be realized in a limited economical way and has also an influence on other device parameters, as short-circuit ruggedness or the trade-off between voltage slope (dv/dt) and switching losses [2.27], additional building blocks can be utilized. These are so called "dummy gates", which do not have a contribution to the channel current and therefore only have passive influence on the device characteristics, i.e. via Gate/Drain and Gate/Source capacitance. A second additional building block is the source trench, see Figure 2.4.14 [2.27].

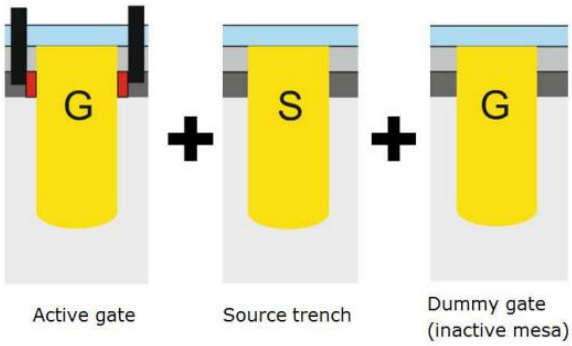


Figure 2.4.14 Building blocks for MPT optimization [2.27]

Typical values for a cell pitch are in the range of some µm, which is depending on the full device concept and the vendor. Trench depths are in the range of 5µm. These parameters were already proposed in [2.26].
In Figure 2.4.15 two SEM chip cross-sections of different chip vendors are depicted, which show the typical stripe design for this technology.

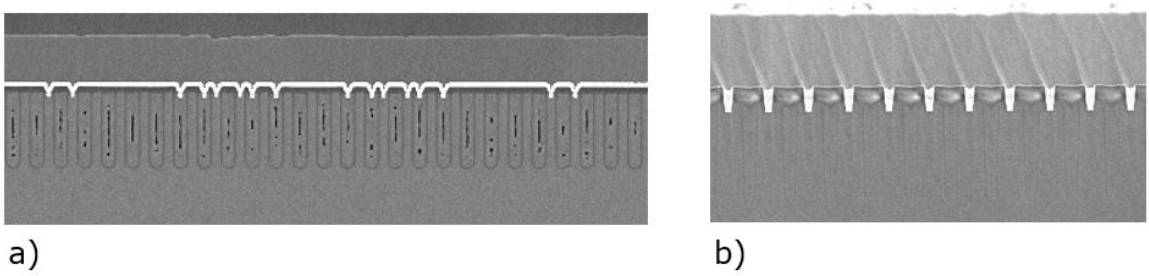


Figure 2.4.15 Two SEM chip cross-sections which are representative for two different MPT designs

One major benefit of the MPT technology utilizing the IE principle is a significant increase in forward characteristics. In literature [2.26], it has been shown that there is a potential of an order of magnitude increasing the forward current at same forward voltage, see Figure 2.4.16 a). In real devices other factors besides play an important role (e.g., short circuit robustness), so that a holistic design is needed which means an increase in forward current of 30% compared to generation 4, with still maintaining sufficient short circuit ruggedness and dynamic robust behavior.

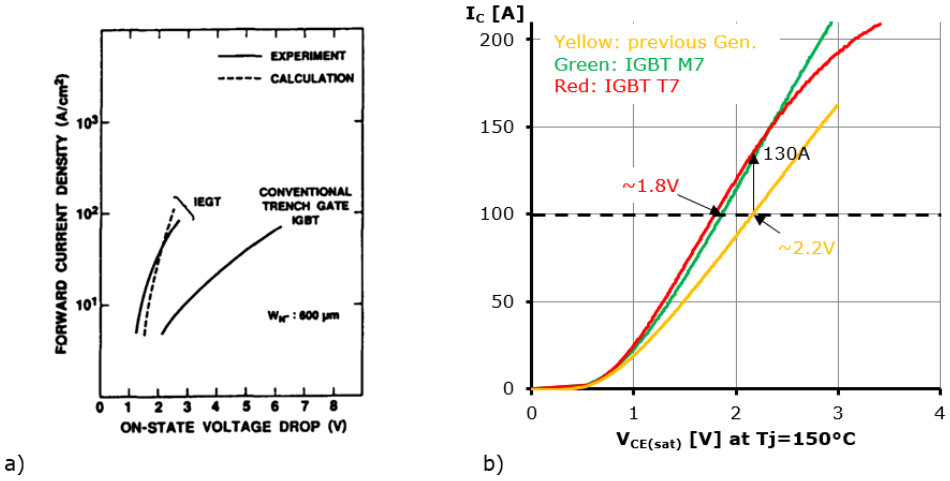


Figure 2.4.16 a) Potential to increase forward current via Injection Enhancement (IE) [2.26] and b) measurement comparison of forward characteristics of generation 7 vs. generation 4

As mentioned before there is also an influence of the design parameters, i.e. cell pitch, on short-circuit behavior. This influence is exemplarily shown in Figure 2.4.17 [2.28]. Simulation wise it was shown that for the chosen device structure using a cell pitch of 1µm nearly no short-circuit ruggedness was given and it can be significantly improved for slightly bigger cell pitches.

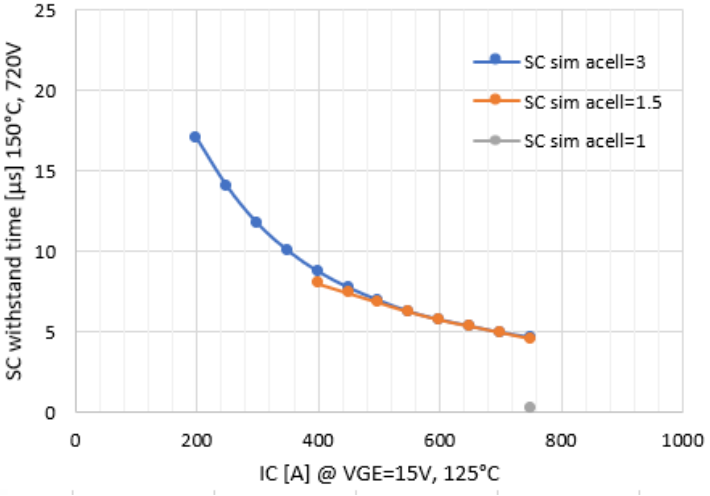


Figure 2.4.17 Potential to increase short-circuit ruggedness via design adaption [2.28]

Having a look at the trade-off curves of two IGBT designs of different vendors, generation 7 shows a clear improvement compared to the previous generation and both seem to lie on the same curve, with slightly different focus in device design, see Figure 2.4.18.

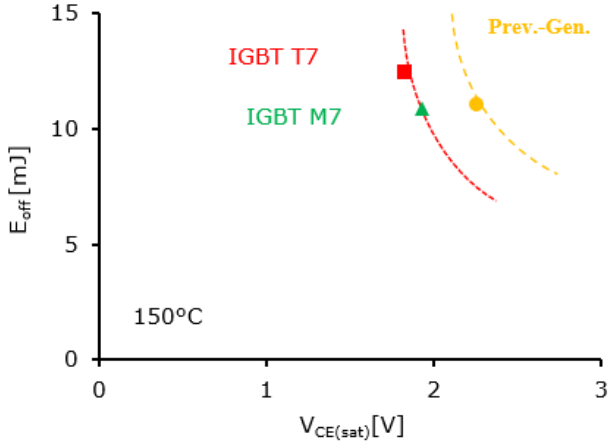


Figure 2.4.18 Comparison of trade-off curves for IGBTs of generation 7 vs generation 4

2.5 Si and SiC Power MOSFET

2.5.1 Structure and functional principles

While the drain-source ON-resistance $R_{DS(on)}$ of low-voltage MOSFET is composed of individual cellular resistances with shares of approx. 5% to 30%, some years ago more than 90% of the $R_{DS(on)}$ of MOSFET using higher reverse voltages resulted from the n^- epitaxial area resistance. For the dependency of $R_{DS(on)}$ on the power MOSFET drain-source breakdown voltage $V_{(BR)DSS}$, the following equation applied:

$$R_{DS(on)} = k \cdot V_{(BR)DSS}^{2.4...2.6}$$

k: material constant, e.g. k = $8{,}3 \cdot 10^{-9}$ A^{-1} for 1 cm^2 chip area i.e. the on-state voltage

$$V_{DS(on)} = I_D \cdot R_{DS(on)}$$

I_D: drain current

It was far higher for transistors with a blocking voltage above around 400V than that of a comparable IGBT.
The compensation principle in new MOSFET concepts developed as of 1999 (Superjunction MOSFET, see chapter 2.5.3) enabled the link between blocking voltage and doping of the n^- region to be broken, thus drastically reducing its resistance. According to [2.29], for such power MOSFET, the equation

$$R_{DS(on)} = k \cdot V_{(BR)DSS}^{1.3}$$

now represents a far lower dependency of the on-state voltage on the blocking voltage. For MOSFET applications in practice, it's purely ohmic output characteristic is advantageous without the threshold voltage of bipolar components. The essential advantage that the unipolar MOSFET has compared to bipolar components is that there are no storage effects, because the majority charge carriers are exclusively responsible for charge transfer; extremely short switching times can be achieved.
In practice, power MOSFET properties are strongly influenced by the parasitic elements in the real structure. To understand these real properties and possible failure mechanisms, the equivalent circuit diagram of the power MOSFET (Figure 2.5.1) must be considered.

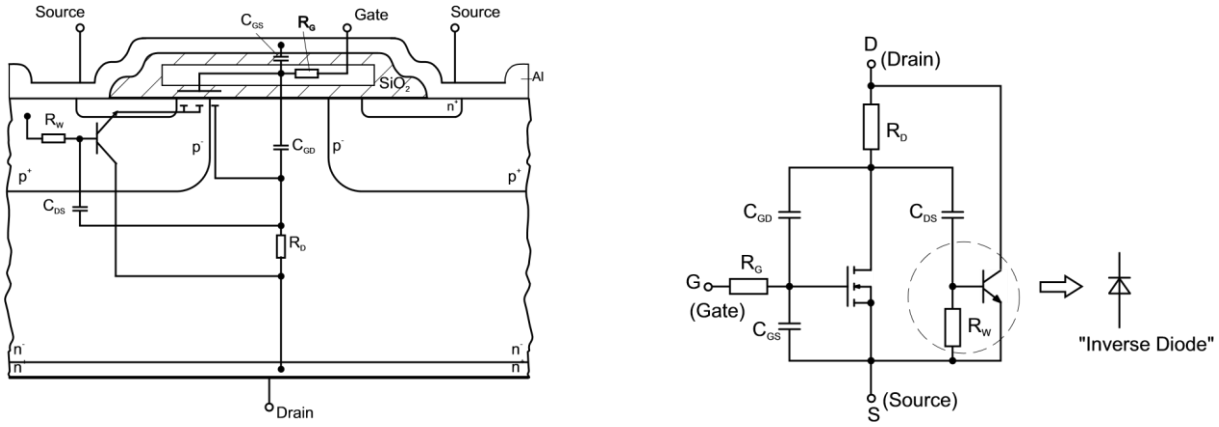


Figure 2.5.1 Power MOSFET cell including the key parasitic elements a) Parasitic elements in the cellular structure; b) Equivalent circuit diagram with parasitic elements

The physical causes and designations of the parasitic capacitances and resistances shown in Figure 2.5.1 are evident in Table 2.5.1.

Symbol	Designation	Physical Description
C_{GS}	Gate-source capacitance	Overlapping gate and source metallisation; dependent on gate-source voltage; independent of drain-source voltage
C_{DS}	Drain-source capacitance	Junction capacitance between n^- drift area and p-well; dependent on cell surface, breakdown voltage and drain-source voltage
C_{GD}	Gate-drain capacitance	Miller capacitance; generated by overlapping of gate and n^- drift area
R_G	Internal gate resistance	Polysilicon gate resistance; additional series resistors are often needed in modules with several transistor chips to minimise oscillations between chips
R_D	Drain resistance	Resistance of n^- region; often the main part of MOSFET on-state resistance
R_W	Lateral resistance of the p-well	Base-emitter resistance of the parasitic bipolar NPN transistor

Table 2.5.1 Physical causes and designations of MOSFET parasitic elements

Apart from internal capacitances and resistances, the equivalent circuit diagram of the power MOSFET also shows an "ideal MOSFET", an NPN transistor at the gate side: n^+ source region (emitter) / p^+ well (base) / n^-drift area (collector) with lateral resistance of the p^+-well below the emitters as base-emitter resistance R_W. R_W and the base-to-collector connection of the parasitic bipolar transistor form the inverse diode, which makes the power MOSFET reverse-conducting.

2.5.2 Static behaviour

Figure 2.5.2 shows the output characteristics of a power MOSFET with structural reverse conductivity ("inverse diode"), freewheeling diode and its transfer characteristic.

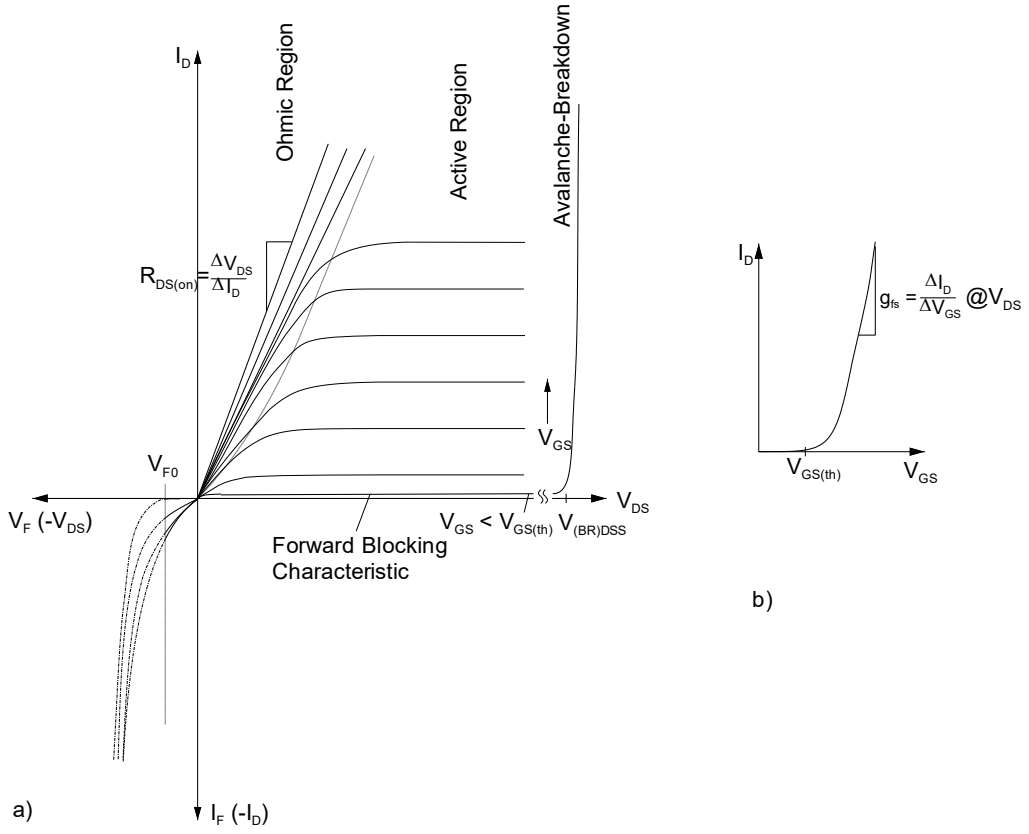


Figure 2.5.2 a) Output characteristics of a power MOSFET (n-channel enhancement type); b) Transfer characteristic $I_D = f(V_{GS})$

The stationary switching states are as follows:

Forward off-state and avalanche breakdown

If a positive drain-source voltage V_{DS} and a gate-source voltage V_{GS} below the gate-source threshold voltage level $V_{GS(th)}$ is applied, only a very small cut-off current I_{DSS} will flow between the drain and source terminal. When V_{DS} rises, I_{DSS} increases slightly at first. Above a specified, maximum rated drain-source voltage V_{DSS} there will be an avalanche breakdown of the PIN junction p^+-well / n^- drift area / n^+ epitaxy layer (drain-source breakdown voltage $V_{(BR)DSS}$). Physically speaking, $V_{(BR)DSS}$ corresponds roughly to the breakdown voltage V_{CER} of the parasitic bipolar NPN transistor in the MOSFET structure, generated by the following sequence of layers: n^+ source region (emitter) / p^+-well (base) / n^- drift area / n^+ epitaxy layer drain region (collector).
The multiplication current generated during avalanche breakdown in the collector-base diode can lead to MOSFET destruction caused by bipolar transistor turn-on. Base and emitter regions are, however, almost shorted by the emitter metallisation; between them there is nothing but the lateral resistance of the p^+-well. Various design-related measures, e.g., small MOSFET cells, a homogenous cell field, low-ohmic p^+-wells, optimum outer structures and very homogenous technological processes, can produce a very low breakdown current per cell which - under precisely specified conditions - will not yet trigger turn-on of the bipolar transistor structure. For these "avalanche resistant" MOSFETs, the datasheets specify a permissible avalanche energy E_A for single pulses or periodic load (limited by the maximum rated chip temperature).
Since absolute symmetry cannot be guaranteed for power modules working with several MOSFET chips connected in parallel, it is not permissible to use more than the maximum E_A value guaranteed for a single chip.

On-state (1st quadrant)

The forward on-state at a positive drain-source voltage V_{DS} and positive drain current I_D comprises two characteristic curve areas:

Active region (pinch-off area)
With a gate-emitter voltage V_{GE} that hardly exceeds the gate-emitter threshold voltage $V_{GE(th)}$, a relatively high voltage share will be depleted through the channel owing to current saturation (horizontal part of the output characteristics). The drain current I_D is controlled by V_{GS}. As a measure for the transfer behaviour as described in Figure 2.5.2 b) the forward transconductance g_{fs} is defined as

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{I_D}{V_{GS} - V_{GS(th)}}$$

Forward transconductance rises in proportion to the increase in drain current I_D and the drain-source voltage V_{DS} and falls as chip temperature increases. In the switching mode that is exclusively permissible for power modules working with several MOSFET chips connected in parallel, the pinch-off area is only run through during turn-on and turn-off. Stationary module operation in the pinch-off area is not permissible, because $V_{GS(th)}$ drops when the temperature rises, meaning that even small differences between the individual chips may cause thermal instability.

Ohmic characteristic area
The ohmic characteristic area (steep part of the output characteristics), which corresponds to ON-state during switching operations, is reached when I_D is determined by the outer circuit only. On-state behaviour is characterised by the drain-source on-resistance $R_{DS(on)}$ as a quotient of changing drain-source voltage V_{DS} and drain current I_D. The on-resistance $R_{DS(on)}$ is dependent on the gate source voltage V_{GS} and the chip temperature. In the operating temperature range of a MOSFET, $R_{DS(on)}$ is almost doubled in the range between 25°C and 125°C, cf. chapter 7.5.4.

Inverse operation (3rd quadrant)

In inverse mode, the MOSFET has a diode characteristic at $V_{GS} < V_{GS(th)}$ (continuous curve in Figure 2.5.2). This behaviour is caused by the parasitic diode in the MOSFET structure; the on-state voltage of the collector-(source)-base-(drain)-pn-junction ("inverse diode"). The bipolar current flow through this diode determines the on-state behaviour of the MOSFET in reverse direction, when the channel is closed (Figure 2.5.3 a)).

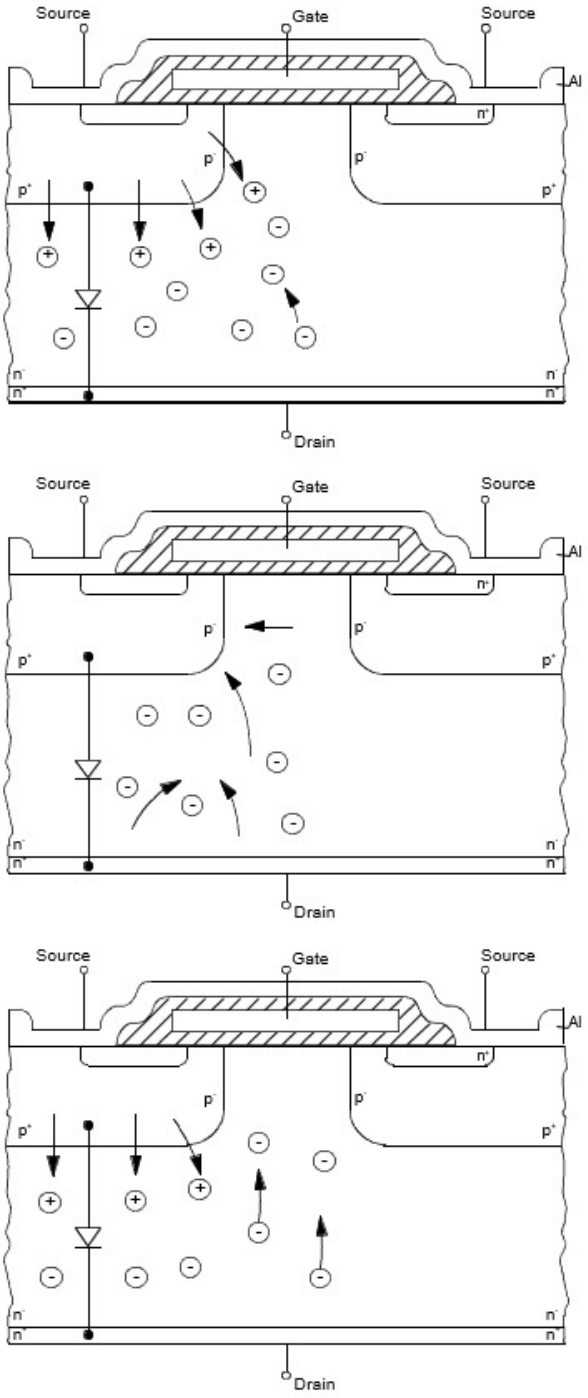


Figure 2.5.3 Inverse operation of a power MOSFET [2.30] ; a) Closed channel (bipolar current flow); b) Open channel and low negative V_{DS} (unipolar current flow); c) Open channel and high negative V_{DS} (combined current flow)

In general, the bipolar inverse diode can be utilised within the current limits specified for the MOSFET. Practice, however, often shows that

- inverse diodes cause relatively high on-state losses which must be dissipated together with the MOSFET losses and
- that the poor turn-off behaviour and relatively low dv/dt limits of these PIN diodes are responsible for the practical application limits of MOSFET bridge circuits in processes that require hard switching.

As shown in Figure 2.5.3, the MOSFET channel can also be conductively controlled when a negative drain-source voltage is present, provided that a gate-source voltage is applied above the threshold voltage level.

If the drain-source voltage is then externally limited - e.g., by connecting a Schottky diode in parallel - to values below the threshold voltage of the inverse diode, the inverse current will remain a unipolar electron flow (majority carrier flow) from drain to source. Consequently, the switching behaviour corresponds to that of MOSFET. The inverse current depends on $-V_{DS}$ and V_{GS} (Figure 2.5.3 b).
Operation according to Figure 2.5.3c occurs, if the channel is additionally controlled while the bipolar inverse diode is conducting (drain-source voltage above threshold voltage level). This results in a lower on-state voltage than for a simple parallel connection for diode and MOSFET, since the injected charge carriers laterally diffuse as well, thus improving MOSFET conductivity.
Today, this behaviour is made use of in low-voltage power supply systems, where "synchronous rectifiers" with integrated MOSFET can be used instead of conventional diode rectifiers. If MOSFETs are triggered during the conducting phase of their inverse diode, switch-mode power supplies with < 15V output voltage, for example, may substantially gain in efficiency owing to the extremely low on-state voltage (some 10mV) compared to conventional diode rectifying (on-state voltage several 100mV).

2.5.3 Dynamic behaviour

The switching behaviour (switching velocity, losses) of MOSFET power modules is determined by their structural, internal capacitances and the internal and terminal resistances. Contrary to the ideal of powerless voltage control via the MOSFET gate, frequency-dependent control power is required; this is owing to the recharge currents of the internal capacitances which are needed for switching. Furthermore, the commutation processes are affected by the parasitic connection inductances present in the components and connections and generated by connecting transistor chips in power modules; they induce transient overvoltage and may cause oscillations due to the circuit and transistor capacitances, cf. chapter 9.
The switching behaviour of power MOSFET can be described as resulting from the transistors internal capacitances and resistances:
When the MOSFET is turned off, C_{GD} is low and approximately equal to C_{DS}.
During on-state, C_{GD} will increase rapidly as soon as the gate-source voltage has exceeded the drain-source voltage; this is due to inversion in the enhancement layer below the gate regions.
Datasheets (cf. chapter 7.5.4) normally list the low-signal capacitances Ciss, Crss and Coss of the turned-off transistor, see Table 2.5.2.

	Power MOSFET
Input capacitance	$C_{iss} = C_{GS} + C_{GD}$
Reverse transfer capacitance (Miller capacitance)	$C_{rss} = C_{GD}$
Output capacitance	$C_{oss} = C_{GD} + C_{DS}$

Table 2.5.2 Definition of MOSFET low-signal capacitances

When calculating the switching behaviour, this data is of very limited use only, for reasons that have already been explained in detail for the IGBT. The "hard" switching behaviour of MOSFET when switching ohmic-inductive loads with continuous load current, i.e. the time constant of the load L/R is much greater than the cycle 1/f of the switching frequency, is looked at below. Figure 2.5.4 shows the basic waveforms of drain current and drain-source voltage in analogy to the IGBT described in the previous chapter.
Apart from the non-ideal properties of transistors and diodes, passive circuit components also influence switching losses and operating point waveforms to a high degree. Their influence will be discussed in more detail later in chapter 9.

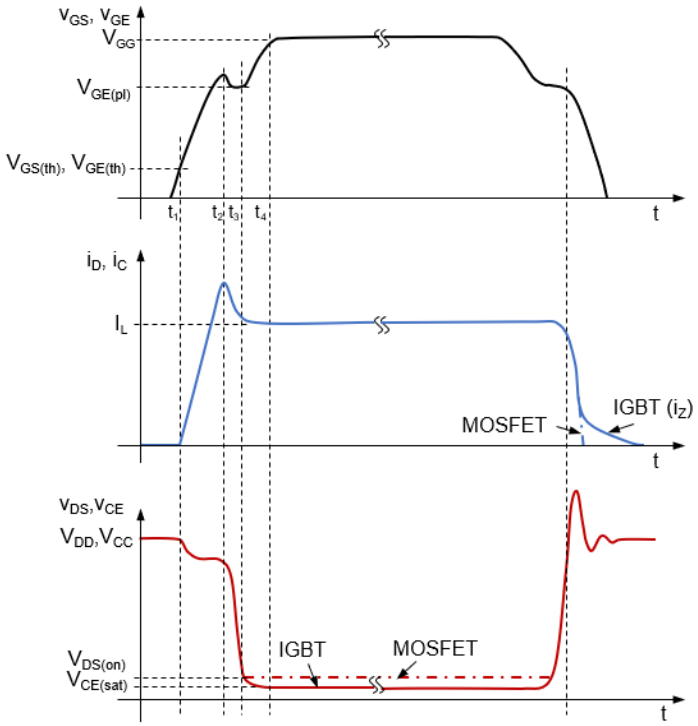


Figure 2.5.4 Typical "hard" switching behaviour of power MOSFET and IGBT when switching ohmic-inductive load with a freewheeling circuit (current and voltage waveforms)

Turn-on

As Figure 2.5.4 demonstrates, the drain-source voltage of the power MOSFET drops to the on-state voltage value within some 10 ns $V_{DS(on)} = I_D \cdot R_{DS(on)}$.
Turn-on: switching interval 0...t_1 (blocked transistor)
The gate current i_G starts flowing when the control voltage is applied. At first, i_G charges only the gate capacitance C_{GS} until it reaches the charge quantity Q_{G1}; the gate-source voltage V_{GS} rises in line with the time constant determined by the input capacitance of the MOSFET and the gate resistance. Since VGS is still below the threshold voltage $V_{GS(th)}$, no collector current will flow during this period.

Turn-on: switching interval t_1...t_2 (drain current rise)

After the threshold voltage $V_{GS(th)}(t_1)$ has been reached, the drain current will start to rise. Similarly, V_{GS}, which is connected to the drain current in the MOSFET pinch-off area by means of the rate of rise g_{fs} with $I_D = g_{fs} \cdot V_{GS}$, will increase up to the value $V_{GS1} = I_D/g_{fs}$ (time t_2). Since the freewheeling diode can block the current at t_2 only, V_{DS} will not drop significantly before t_2 is reached. At $t = t_2$, charge Q_{G2} will have flowed into the gate.
The largest amount of turn-on losses is generated in the MOSFET during this time interval. As long as the i_D value is still below I_L and part of I_L still has to flow through the freewheeling diode, the drain-source voltage v_{DS} cannot drop far below the operating voltage V_{DD} during this period. The difference between V_{DD} and V_{DS} outlined in Figure 2.5.4 is mainly caused by transient voltage drops across the parasitic inductances of the commutation circuit.

Turn-on: switching interval t_2...t_3 (transistor fully switched on in the pinch-off area)

When the freewheeling diode is turned off, V_{DS} drops to the on-state value until t_3
$V_{DS(on)} = I_D \cdot R_{DS(on)}$ has been reached. Between t_2 and t_3, drain current and gate-source voltage are still coupled through the transconductance: V_{GS} remains roughly constant. While v_{DS} drops, the gate current i_G recharges the Miller capacitance C_{DG} with the charge (Q_{G3}-Q_{G2}). By $t = t_3$, an amount of charge equal to Q_{G3} will have flowed into the gate. After the entire load current I_L has been commutated to the MOSFET, the freewheeling diode will start to block. Due to the reverse recovery time of the freewheeling diode, the MOSFET drain current i_D initially continues to rise above I_L during turn-off of the freewheeling diode (t_{rr}) by the amount I_{RRM} of the diode reverse current and dissipates the reverse recovery charge Q_{rr} of the freewheeling diode. For explanations of the characteristics I_{RRM}, Q_{rr} and E_{rr} for inverse diodes, see chapter 7.5.3.

Turn-on: switching interval t_3...t_4 (ohmic operating area)

At t_3, the MOSFET is now turned on and its operating point has passed through the pinch-off area and has reached the border of the ohmic operating area. V_{GS} and I_D are no longer coupled by g_{fs}. The charge quantity (Q_{Gtot} -Q_{G3}) now supplied to the gate causes the further rise in V_{GS} up to the level of the gate control voltage V_{GG}.

Turn-off

During turn-off, the processes described above run in reverse direction. Charge Q_{Gtot} has to be discharged from the gate with the aid of the gate current. In contrast to IGBT, power MOSFET do not use a negative gate voltage here but V_{GS} = 0V, see chapter 9.
During turn-off only the internal capacitances of the power MOSFET have to be recharged to such an extent that there is no charge carrier influence left in the channel area. From this point on, neutrality interference in this area will quickly be reduced and the drain current will drop rapidly. The overshoot of v_{DS} over V_{DD} indicated in Figure 2.5.4 results mainly from the parasitic inductances of the commutation circuit and increases in proportion to the turn-off speed -di_D/dt of the power MOSFET.
Likewise in the case of power MOSFET: the more the specific transistor application deviates from the "ideal hard switch" application described here, the more "blurry" the step-form of the gate-source voltage curve becomes. The intervals "decoupled" during hard switching will then merge more and more, and any description of the switching behaviour becomes more complex.

2.5.4 Technologies, trends and new developments

Power electronics largely use the vertical structure shown in Figure 2.4.3, where gate and source terminals are located on the chip surface and the drain terminal is on the backside of the chip. The load current is conducted vertically through the chip outside the channel. The VDMOSFET version (Vertical Double Diffused MOSFET) introduced at the beginning of the eighties is still being used today and is being continuously improved, e.g. reduction in cell dimensions. Depending on the application focus on "low" or "high" drain-source voltage, the key developments on the power MOSFET front have gone in two directions with significant structural differences:

Trench-Gate MOSFET

The example shown in Figure 2.5.5 illustrates the continuous development towards the Trench MOSFET, which was introduced around 1997.

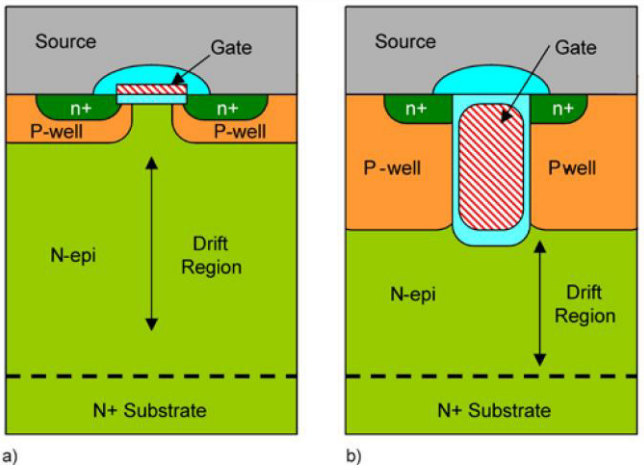


Figure 2.5.5 a) conventional VDMOSFET; b) MOSFET with trench-gate (Trench MOSFET) [2.31]

Similar to the development of the Trench IGBT, the insulated gate plates - and thus the channel area - are arranged vertically here; the distance to be covered by the electrons in the n-region is thus shorter. This enables a significant reduction in $R_{DS(on)}$ mainly in the lower voltage range compared to conventional structures.
As mentioned at the beginning of this chapter, the "breakthrough" achieved in the reduction of $R_{DS(on)}$ was initiated in 1999 by Infineon with the development of the CoolMOS™ as the first "Superjunction" power MOSFET on the market.
The compensation principle used in superjunction components was developed for MOSFET with blocking voltages between 500V and 1000V. Figure 2.5.6 demonstrates the layout and functional principle of a CoolMOS™.

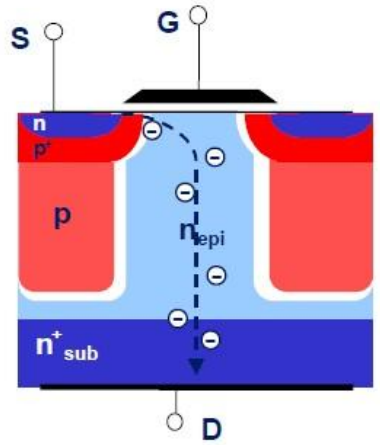


Figure 2.5.6 Layout and functional principle of a superjunction MOSFET (CoolMOS™) [2.29]

With the aid of several epitaxy steps or lateral diffusion from trenches, high-doped conducting columns are injected into the low-doped n^- drift area. These columns are connected with the p-wells. Column doping is dimensioned such that the n-doping of the drift area is compensated for, resulting in a very low effective doping level.
In blocking state, the field is almost rectangular and can take up the maximum voltage level in relation to the thickness of the n^-- region. Drift area doping can only be increased to such an extent that still allows for it to be compensated by the same amount of doping in the p-column ("compensation principle"). This overrides the interdependency of blocking voltage and doping density [2.16].
As a result, the thickness of the n^- drift area can be reduced substantially compared to conventional MOSFET, and drift area conductivity can be increased by way of higher doping. This means that the on-resistance $R_{DS(on)}$ will no longer increase to the power of 2.4...2.6, but almost linear to the breakdown voltage $V_{(BR)DSS}$; the on-state losses of high-blocking power MOSFET can be reduced significantly (to 1/3 - 1/5). Chip area, switching losses and gate capacitance / gate charge drop accordingly – for the same current capability. Figure 2.5.7 shows the differences in layout and properties for standard and superjunction power MOSFET.

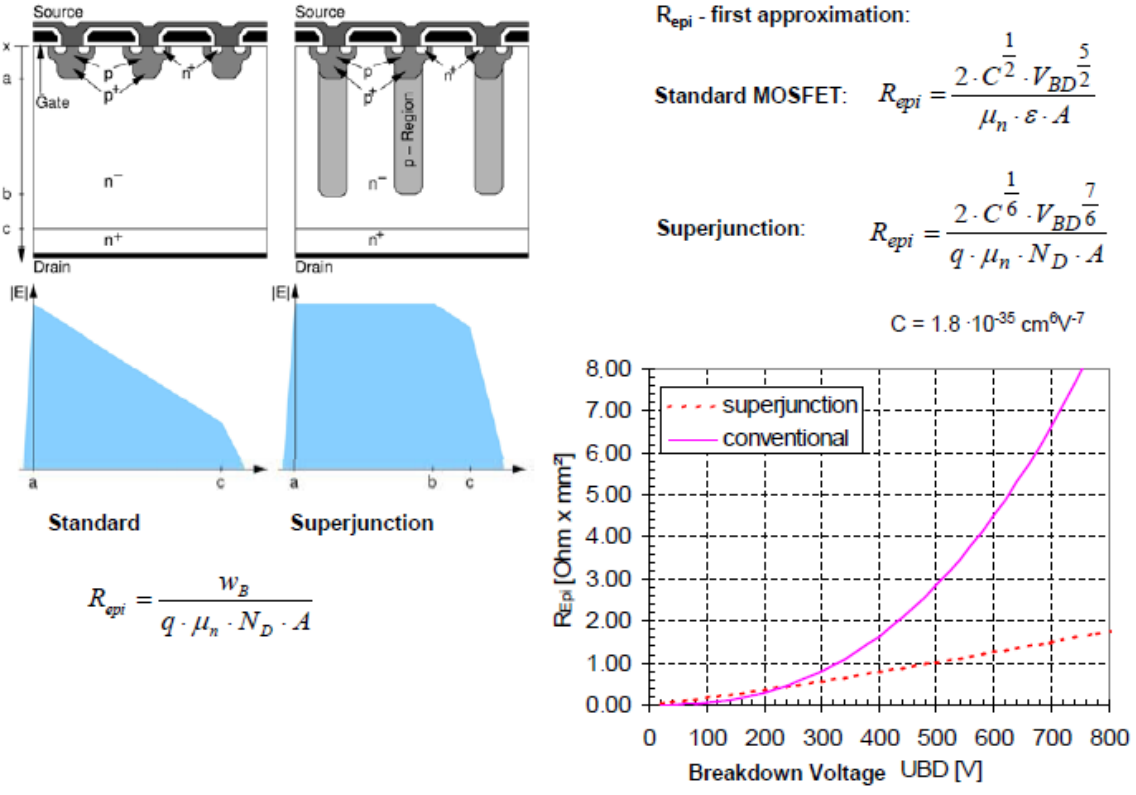


Figure 2.5.7 Comparison of standard and superjunction MOSFET [2.32]

Introduction of insulated field plates

In order to be able to transfer the superjunction principle to MOSFET for low voltages, technologies had to be developed that were much simpler and cheaper than those dealing with high-volt components. This challenge was met by Infineon, for example, with the product "OptiMOS™", which is suitable for blocking voltages up to 300V [2.33]. OptiMOS™ transistors have insulated field plates rather than p-columns built up in epitaxy processes. These field plates are arranged in trenches which are etched into the n^- drift area, insulated by a layer of silicon oxide and alternately connected to the source region and the polysilicon gate (Figure 2.5.8).

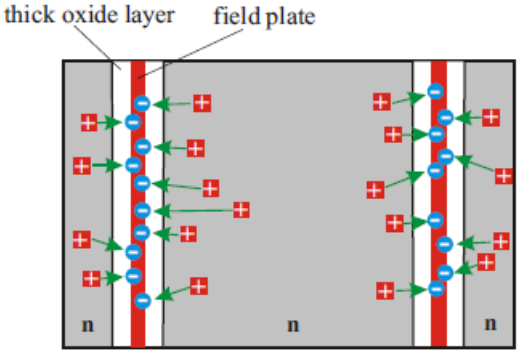


Figure 2.5.8 Principle layout of an OptiMOS™ [2.33]

Figure 2.5.9 shows the compensation effect of the field plates and the field intensity characteristics in y-direction compared to a conventional-type blocked pn-junction. The p-charge on the field plates compensates the doping of the n^- region so that it can be increased as described above. In off-state, the triangular field shape of the simple structure becomes almost rectangular, permitting the reduction of the n^- layer thickness. Higher doping and reduced n^- drift area thickness brings about the advantages that superjunction MOSFET have over conventional structures, as detailed above.

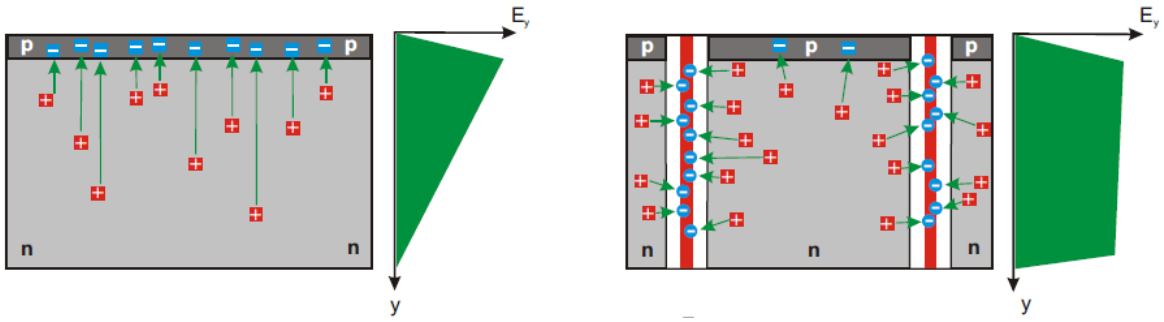


Figure 2.5.9 Field distribution in a conventional pn-junction and a pn-junction with field plates [2.33]

2.5.5 SiC MOSFET technologies, trends and new developments

Power devices based on wide band gap (WBG) material have the potential to outperform energy efficiency compared to devices based on silicon technology (Si). Gallium nitride (GaN) and silicon carbide (SiC) are the most promising WBG materials that allow to exceed significantly the performance limits of Si power devices. Devices based on WBG-material will be able to be faster switched, with lower power losses, which allows the development of components with higher power density to build power converters higher efficiency.
The reasons for this fact will be explained in the following chapters.
Despite it should be mentioned that at the moment of the edition of this version of this book the maturity level of both SiC and GaN devices is not on the level of Si based devices.

2.5.5.1 Si vs. SiC MOSFET

Si and SiC are two kinds of semiconductor material, which are widely used for manufacturing power MOSFET devices. Figure 2.5.10 shows an overview of Si and SiC based on physical material parameters which fundamentally affect the performance of any power switch in a power system [2.34].

Basic material parameters

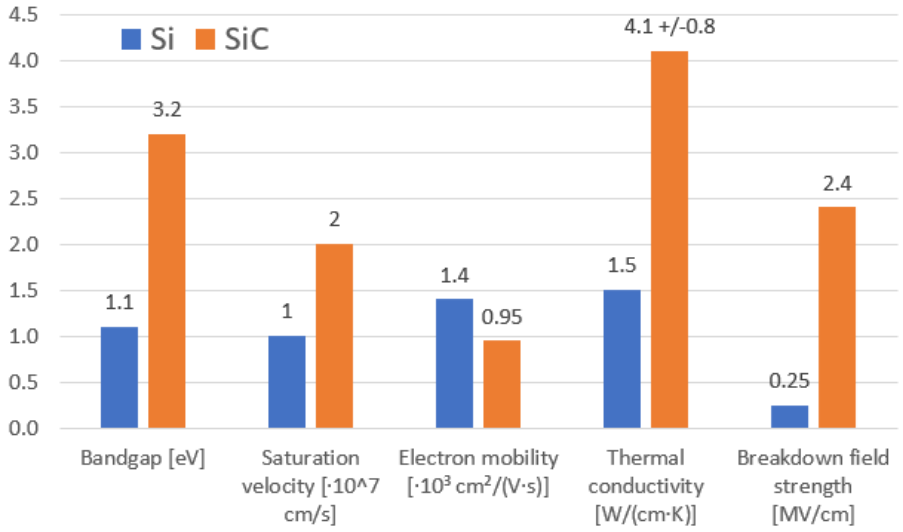


Figure 2.5.10 Si vs. SiC basic material parameters (see [2.34])

As can be easily seen in Figure 2.5.10 there are a lot of benefits using SiC as base material for power devices, besides electron mobility, which has an influence on the on-state behaviour. But on the other hand, the breakdown field strength, which is about an order of magnitude higher than for Si allows smaller drift zones, which means lower resistance in on-state, and therefore brings back benefits for this case. Overall, from a technical perspective using SiC looks very beneficial, but two drawbacks, higher material and manufacturing costs, as well as a lower maturity level, ensure still Si based devices a very important role in power electronics. Especially material related defects like dislocations and micropipes haven been for a long time limiting the forward blocking ability.

Processing differences between Si and SiC MOSFETs

SiC is the most promising candidate at the moment of the edition of this version of this book, because among WBG semiconductors its technology is most mature, e.g. compared with GaN. There is already a certain bandwidth of devices of different suppliers on the market available. The most important fact is that SiC is the only WBG semiconductor with nature SiO_2 as dielectric, which is used needed as insulator (e.g., gate oxide) and diffusion barrier. Just as the SiC substrate and epilayer growth technologies which had gone through decades of developments before power device quality level wafers are available. Also SiC processing technologies were improved during the last decades. But there is still plenty of room to be improved [2.35].
The basic process technology for SiC is based on processes which were already used for processing Si wafers. The main difference lies in the necessity of growing an epitaxial layer on top of a base wafer and the higher temperatures which are needed for all temperature relevant processes, especially annealing and diffusion processes after ion implantation.
Also, it is even more difficult to realize a proper ohmic contact for SiC, because the work functions of most metals used in power electronics are quite big compared with Si affinity, that is, an inherent energy barrier exists between metal/Si interfaces, preventing free carrier exchange. And due to a much lower affinity value, this barrier is only getting higher at a metal/SiC interface, which also explains why Schottky behaviour is typically observed for as-deposited metal contacts on 4H-SiC. To fabricate an ohmic contact, increasing the contact region local doping level (via thermal diffusion or ion implantation) is the most common way for both Si and SiC. To enhance the contact for SiC after metal deposition on even very highly doped SiC films, extra annealing step (1000–1200°C) is usually done to form a homogeneous silicide or carbide layer at the contact interface, which further lowers the Schottky barrier height, leading to a lower contact resistance [2.35].

Comparison of Si vs. SiC MOSFETs

On-resistance

Having a look on the performance of SiC vs. Si MOSFETs, two major topics are the on-resistance and the temperature characteristics. For MOS devices the on-resistance is the resistance between source

and drain in on-state. It typically is a summary of the resistance of the source well, the MOS-channel, accumulating layer, JFET region, drift layer and substrate, which is depicted in Figure 2.5.11 [2.34].

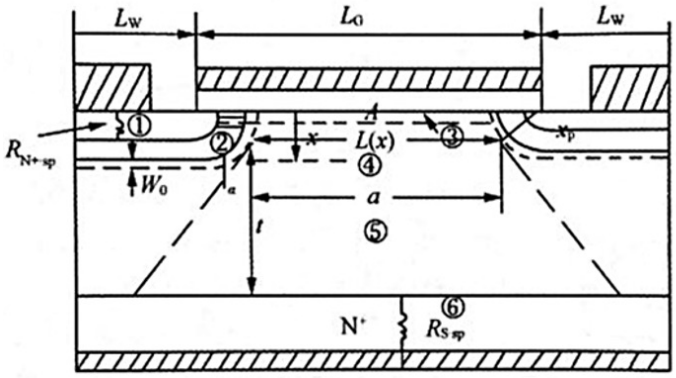


Figure 2.5.11 Principal sketch of MOSFET structure with on-resistance contribution parts [2.34]

Assuming the device as an ideal device, without electrical field disturbance, e.g. edge termination, all resistance parts could be assumed as zero, except the contribution of the drift region. Therefore the specific R_{on}-ideal can be expressed via the dependence of the parallel plane breakdown voltage V_{br} and material related parameters, as dielectric constant of semiconductor ε_s, mobility μ and critical field strength E_C [2.34].

$$R_{on,ideal} = 4 \cdot Vbr^2 / \varepsilon_s \cdot \mu \cdot E_C^3 \quad [2.34]$$

This correlation is shown in comparison for Si and SiC devices in Figure 2.5.12, which represents the theoretical limit for both materials.

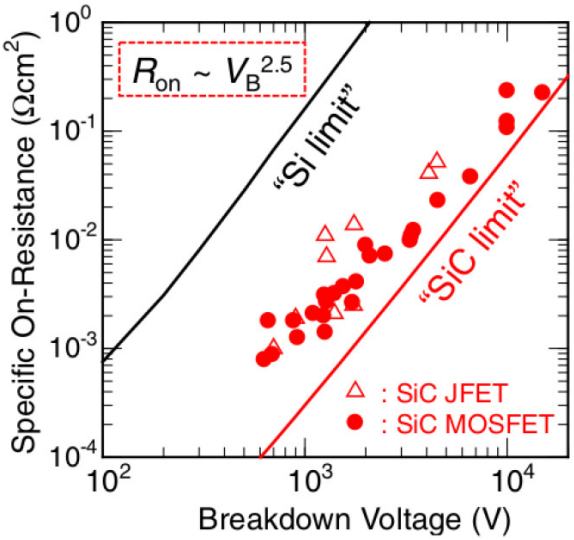


Figure 2.5.12 Comparison of the theoretical limit of R_{on} depending on breakdown voltage for Si and SiC [2.34]

In Figure 2.5.12 it is shown that there is a significant reduction in specific R_{on} in dependence to V_{br} for SiC compared to Si. This means that the power losses inside the device can be significantly reduced choosing SiC or otherwise the rated current per area can be raised or the chip area decreased and therefore the cost per chip can be reduced.

2.5.5.2 High temperature characteristics

Temperature influences various parameters of MOSFET devices, e.g., current conduction capability in on-state is decreasing with increasing temperature (R_{on} is increasing with temperature) due to decreasing mobility, threshold voltage is decreasing with increasing temperature, blocking capability in off-state (leakage current and breakdown voltage are increasing with temperature).
The thermal conductivity of SiC is about two times higher than that of Si, as shown in Figure 2.5.13.

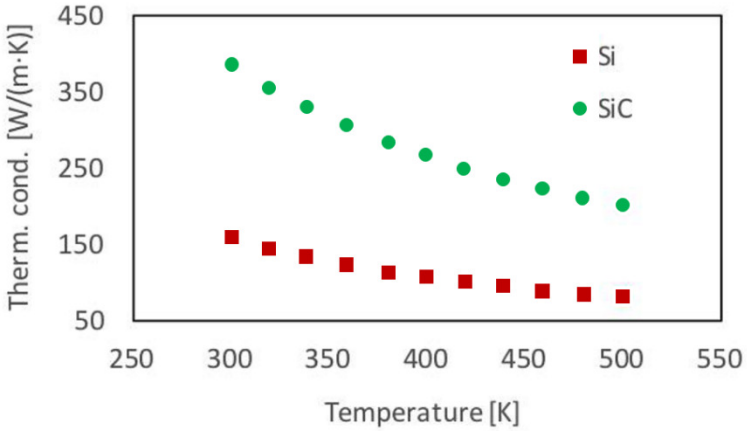
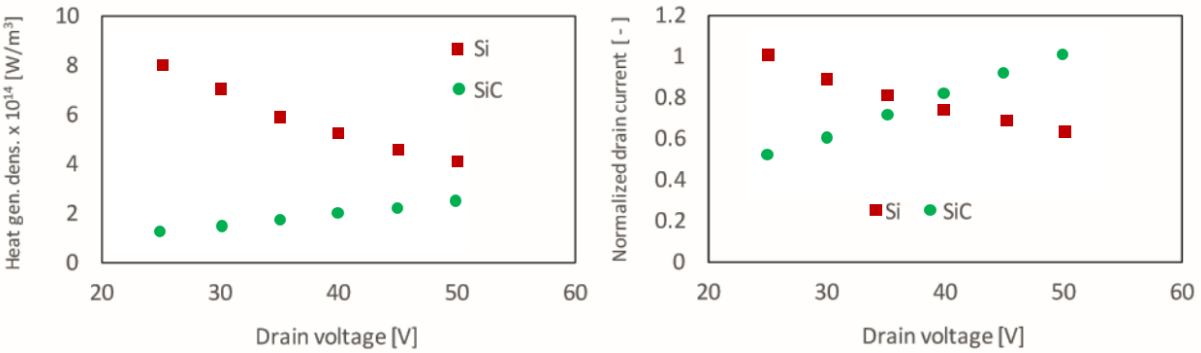


Figure 2.5.13 Comparison of thermal conductivity of SiC vs. Si depending on temperature [2.34]

This is due to the strong chemical bonds of Si and C atoms and leads to the better usability of SiC for higher temperature applications. Due to the fact that SiC has higher thermal conductivity, its temperature rises at lower speed. While Si power MOSFETs are in current saturation state at and beyond referring drain voltage, the drain current of SiC MOSFETs still rises with the drain voltage, because of the high saturation electron velocity of SiC. Therefore, SiC MOSFETs have a superior high-temperature operating capability compared to Si MOSFETs, see Figure 2.5.14 [2.34].



a) b)

Figure 2.5.14 Comparison of SiC and Si drain voltage vs. a) heat generation density around hot spot; b) normalized drain current [2.34]

2.5.5.3 Body diode and bipolar degradation

One intrinsic benefit using a SiC MOS device is that there is already a body diode existing, which can be used for current commutation. But running the SiC MOS without external diode two parameters have to be watched carefully. One is a forward voltage drift on the diode, which would indicate the presence of stacking faults in the substrate. The other is a potential drift in the gate threshold voltage, which might occur in some MOSFETs. This influences on the on-state resistance of the transistor. It is supposed to be driven by near-interfacial oxide traps, or the formation of additional interface charges. These mechanisms can be related to carrier injection in the oxide. The phenomenon is causing carrier injection, which are injection by tunnel effect, Fowler-Nordheim injection and hot carrier injection [2.36]. In Figure 2.5.15 a schematic cross-section of a SiC MOS device is shown, also with current paths of channel current I_{CH} and the body diode current I_{BD}, and equivalent circuits.

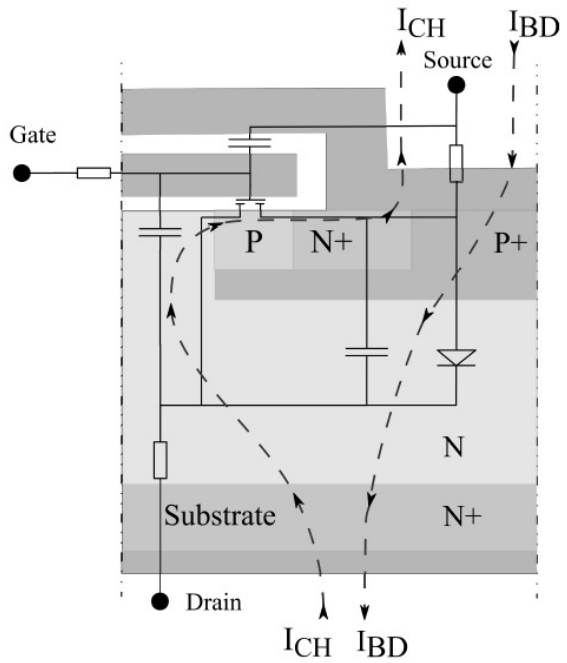


Figure 2.5.15 Sketch of internal structure of a SiC MOSFET, equivalent circuit and current paths I_{CH} and I_{BD} [2.36]

The most important reliability issue in 4H-SiC based devices is bipolar degradation. This degradation is caused by the expansion of single Shockley stacking-faults (1**SSF**s) from basal plane dislocations in the 4H-SiC crystal [2.37]. The degradation of the body diode in SiC power MOSFETs is caused by basal plane dislocation (**BPD**)-induced stacking faults in the drift region. This topic is related to the SiC epitaxial growth. A possibility to avoid a pn-junction degradation is to use an antiparallel Schottky diode. This also brings the benefit of faster recovery time and lower losses but means an extra device. An improved solution is an integration of a Schottky diode in the MOSFET [2.36].
The quality of the epitaxial layer has been matured over the years and therefore the reliability of planar SiC power MOSFETs has significantly improved. The degradation of the body diode has become negligible for voltage ratings below 1.2 kV, and some vendors have even eliminated the impact of body diode degradation at the voltage rating of 3.3 kV.
Process improvements have been done, as a potassium hydroxide etching process before the conventional epitaxial growth to create BPD etch pits for enhancing the conversion of BPDs to threading edge dislocations (**TED**s), and using ultraviolet photoluminescence (**UVPL**) on wafers to screen out dies with BPDs.
Also the introduction of a recombination-enhanced buffer layer between the substrate and the drift region. This layer enhances the recombination probability of electron-hole pairs in the epi-layer and therefore decreases the recombination enhanced dislocation glide for BPD. This layer insertion means also a higher cost of the wafer production. But without this measure it is difficult to decrease the number of electron–hole pairs only by controlling the carrier lifetime. Another method to suppress 1SSF expansion is proton implantation on a 4H-SiC epitaxial wafer. Due to the fact that hydrogen ions (protons) are the lightest elements they can be implanted in a depth of more than 10µm with an ion-implantation energy of some MeV. Utilizing this the PDs can be pinned and the expansion of BPDs in the substrate is suppressed. To prevent that the proton implantation causes deterioration of the device performance high-temperature annealing has to be done subsequently [2.37].
In order to reduce the on-state resistance of SiC MOS devices trench gate structures have been introduced, providing higher channel electron mobility, elimination of the JFET resistance, and smaller cell pitch. Analog to Si technology the trench gates have to deal with high electric-field crowding at the bottom corners of the trench gate oxide. To protect the structures additional p^+ implantations have been introduced in the critical areas, which can on the other hand harm the reliability of the parasitic body diode. To reduce the problems correlated to this p^+ implantation, the implantation should be done with low-dose and low-energy. It is beneficial to do the implantation after the dry etching process for the trench gates, since mainly the trench gate corners is necessary. Another approach is to do the implantation at significantly elevated temperatures (e.g., 500°C). Also the annealing conditions after implantation can influence the reliability of the body diode.

The effect of body diode degradation in SiC MOSFETs is, as described before, the expansion of BPD-induced stack faults by absorbing the activation energy from the recombination of injected holes and electrons in the drift region [2.38].

2.5.5.4 MOS Gate – oxides and degradation of channel mobility

A very important feature for the performance of MOSFETs is the interface semiconductor to gate dielectric. For SiC the history of gate structure was to start with a V-groove, which had the problem of early breakdown due to electric field crowding, followed by JFET (problem - controllability) and U-MOS (U-shaped trench with poor sidewall quality). A solution with a sufficient gate oxide interface quality was the surface gate, but nowadays the most common approach is to use trench gates, which are similar to the U-MOSFET, but with improved trench sidewall quality. Both structures are shown in Figure 2.5.16 [2.39].

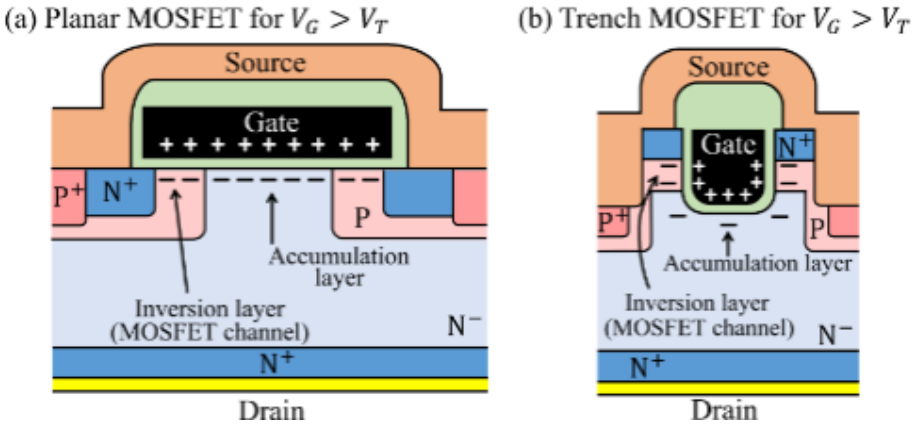


Figure 2.5.16 a) Planar vs. b) Trench device – schematic [2.39]

The reasons for poor interface quality and the ways to improve it are described in the following sequence.

For the channel region there is an extra surface roughness scattering mechanism, i.e., Coulombic scattering caused by extra charges at the MOS interface, which is more process dependent. Gate oxides are often with defects acting as carriers' leakage paths and cause early breakdown. By trapping and discharging carriers during the MOS device operation, these defects (also called states) are the main reason behind the severe Coulombic scattering. Extra charges found in most MOS systems are categorized into four groups, namely, mobile charges, fixed charges, oxide-trapped charges and interface charges [2.35]. A schematic graph showing location and polarity of various charges is depicted in Figure 2.5.17.

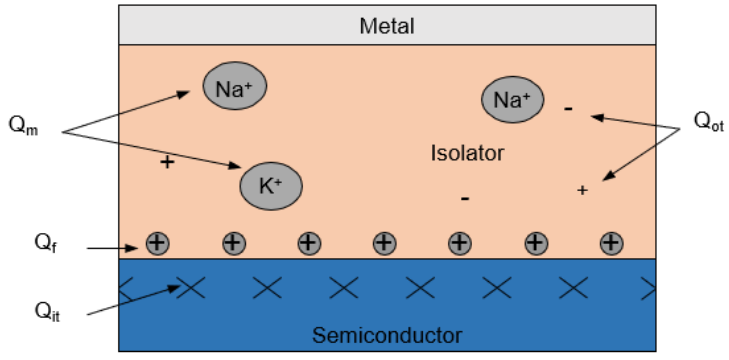


Figure 2.5.17 Schematic of oxide and interface charges

Mobile charges Q_m are metal ionic impurities (such as Na+) introduced during the device fabrication process and can move freely in the oxide with a gate bias. Since positively charged, they will attract semiconductor electrons to the surface and induce extra band bending, leading to a shift of flat band voltage. Mobile charges are highly uncontrollable and thus must be minimized through clean and careful fabrication process. In contrast to mobile charges, fixed charges Q_f refer to those who do not move with gate biases. The origin of fixed charges is believed to be the excessive ions left near the interface after the oxidation process. They are usually located in the oxide and close to the MOS interface. The total amount depends heavily on the oxidation condition.

Since fixed charges stay close to the interface, they also affect the semiconductor band bending. As a result, a shift of flat band voltage from the theoretical value is again observed.
Interface charges Q_{it} are located at the MOS interface. Energy levels of these traps are in the semiconductor band gap; consequently, they can act as carrier traps communicating (charge/discharge) with the bulk semiconductor during device operation. And since these traps are right at the MOS interface, they scatter the channel carriers much more than other charges. The origins of interface traps vary among different MOS systems. For Si/SiO_2 interface, most of the interface traps come from unterminated Si dangling bonds. H_2 annealing after the gate oxidation is typically applied to passivate the unterminated Si dangling bonds. Unlike the previous three, oxide-trapped charges Q_{ot} are induced by the device operation rather than the fabrication process.
The oxide layer, thermally grown or deposited, contains intrinsic defects such as oxygen vacancies. Although these defects are electrically neutral, during the device operation, carriers may be injected into them and make them negatively or positively charged [2.35].
The performance and low carrier density in SiC-MOSFETs suffers from a high density of oxide traps near the 4H-SiC/SiO_2 interface. Unfortunately, the 4H-SiC/SiO_2 interface is of poor quality, and the electrical performance is not even close to Si technology. The interface trap density (D_{it}) at an as-grown 4H-SiC/SiO_2 interface is typically close to $10^{13}cm^{-2}eV^{-1}$, which is two orders of magnitude higher than for the Si/SiO_2 interface. The channel mobility generally decreases with increasing D_{it}; thus, the latter is commonly used as an indicator for the MOS interface quality.
Reasons behind the poor 4H-SiC/SiO_2 interface are still not fully understood. As a hypothesis potential origin of interface traps are two sources, first is the carbon accumulated at the MOS interface during the SiC oxidation process. The reactions occurring during Si and SiC oxidation processes. The second source of SiC/SiO_2 interface traps are oxide defects, which are induced traps, i.e., the oxide-trapped charges mentioned before. To improve the SiC/SiO_2 interface three approaches are known, post-oxidation annealing, channel counter-doping and high-temperature oxidation. Whereas post-oxidation annealing is the most used method, it is a nitridation, which is usually achieved by annealing thermally grown gate oxides in nitrogenous trace gas environment (N_xO) [2.35].

2.5.5.5 SiC MOSFET Trench vs Planar, today and future outlook

One of the most influencing factors taking basic design decisions is the choice of gate design. It is today a controversial discussion to go for planar or trench gate design. This decision plays an important role for device characteristics, as chip size, forward current density, switching losses, robustness, reliability and in the end - cost. One of the most important figures is $R_{on} \cdot A$. The development of this figure through different technology nodes and SiC MOSFET providers in the last years is summarized in Figure 2.5.18 [2.40].

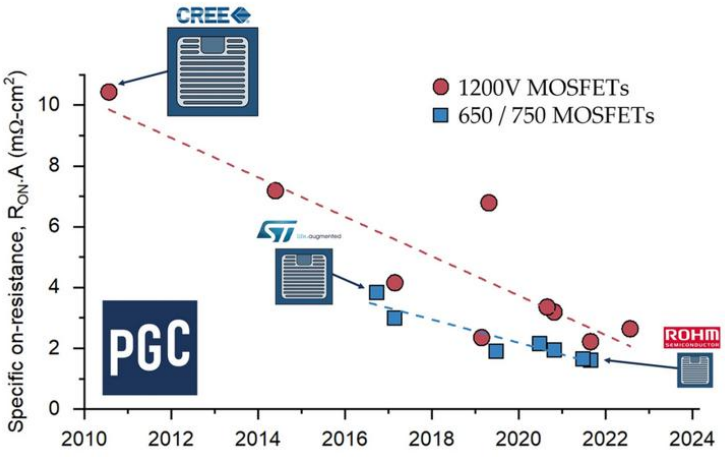


Figure 2.5.18 Overview of devices from different technology nodes and voltage classes (650V, 750V and 1200V) from Cree, ST and Rohm with their specific $R_{on} \cdot A$, as a key figure, since 2010. [2.40]

The basic structures of planar and trench gate design are depicted in Figure 2.5.16, it is the case that the trench structure allows a more compact and therefore lower resistance design than the lateral structure. The possibility to reduce the cell pitch for planar designs has stronger limitations, due to two channel and a JFET regions are all implemented laterally at the surface. Utilizing the trench structure, the channel and JFET regions are rotated by 90° and allow therefore a higher packing density of cell structures.

Beside this the channel mobility is higher at the trench sidewall, which goes linear in the MOS-equation. But higher packing density does not only bring benefits, because this means also higher temperatures, which do have an impact on reliability. One example is the long-term survivability of the gate oxide, and the electrical resistance increases with temperature and decreases the forward current. Other examples are cosmic ray hardness and short circuit ruggedness, which are impacted by higher current densities and temperatures, which can be seen in Figure 2.5.19 [2.40].

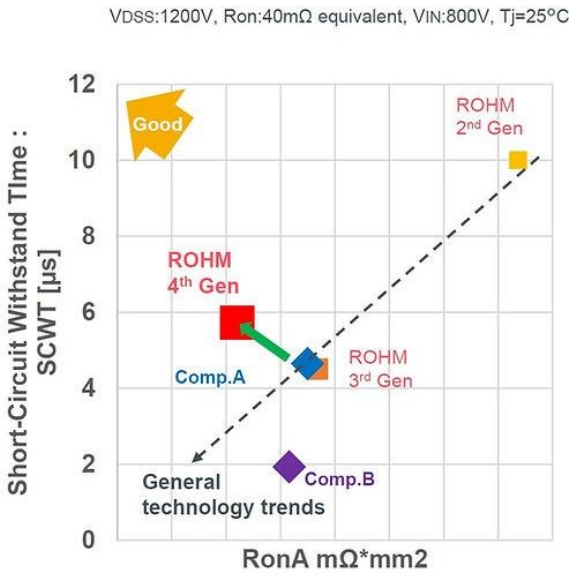


Figure 2.5.19 Technology trend, reduced specific R_{on} · A reduces short circuit withstand time, which can be countered via design [2.40]

One key feature of utilizing trench technology without derating or loss in reliability is to protect the gate oxide, this is even more important for the higher electric field strength which apply in SiC MOSFET devices. An example how this can be achieved is shown in Figure 2.5.20 [2.41].

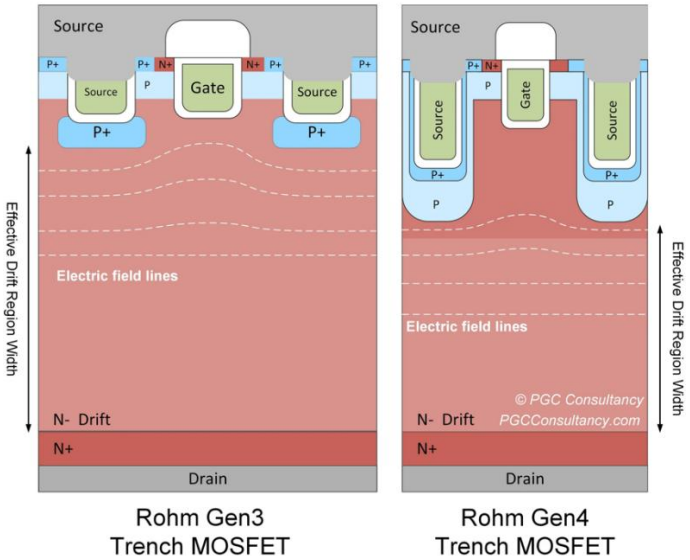


Figure 2.5.20 Improvement of gate oxide protection against electric field via design improvement [2.41]

It should be mentioned that nothing is for free, also the creation and protection trench gate structures means a significant effort in design and technology compared to planar structures. Therefore, some of the SiC MOSFET providers are still struggling to implement a trench gate and others think about doing a step back for the moment from trench to planar gate, due to cost efficiency. But in the end, to fully utilize the possible benefits of SiC MOSFET (esp. R_{on}·A), in future there will be no way beside trench gate architecture.

2.6 GaN Devices

The motivation to use GaN devices in power electronics is the same as for SiC devices. As mentioned before the maturity level of available devices and the usability in power electronic applications is up to the moment of the edition of this version of this book not suited for the use in power modules in a broad bandwidth.
Using GaN HEMT (Gallium Nitride **H**igh-**E**lectron-**M**obility-**T**ransistor) devices is the most common approach, where two basic types are available. From technology perspective the so-called D-mode (**D**epletion) GaN-HEMT is comparably easy to realize, but not that easy to drive in applications. This is because it is a normally-on device, exemplary operation parameters are for gate voltage maximum ratings -10V to +20V, the threshold voltage is about -5V and the operational gate voltage in on-state is int the range of 5V to 10V. From driving perspective, it is better suited to use normally-off devices, which is realized via using so-called E-mode (**E**nhancement) HEMT device concept. Both device concepts are depicted in Figure 2.6.1. For e-mode devices exemplary operation parameters are for the gate voltage maximum ratings -10V to +7V, the threshold voltage is about 1V to 2V and the operational gate voltage for the on-state is in the range of 5V to 6V.
The basic device structure is created by structuring an AlGaN layer on a GaN layer, which is provided typically on a carrier layer (e.g., Si or sapphire, not depicted). Due to differing band gaps, the interface between the AlGaN/GaN layers forms a zone with high charge carrier density, mobility and recombination rate, the so-called two-dimensional electron gas (2**DEG**). This structure intrinsically forms the before described D-mode device. Further layout steps, e.g., a p-GaN layer under the gate structure, are necessary to enable the normally-off E-mode function of the device by creating an artificial depletion zone under the gate contact.
Despite electrical benefits of using a D-mode device, i.e., no performance trade-off (e.g., R_{on}) by forming depletion zone at the E-mode device and higher gate robustness, an E-mode device is usually preferred due to increased safety during operation. This is, because the device is automatically off, when no gate voltage is applied and compatibility with the operating mode of most state-of-the-art Si-based power devices.

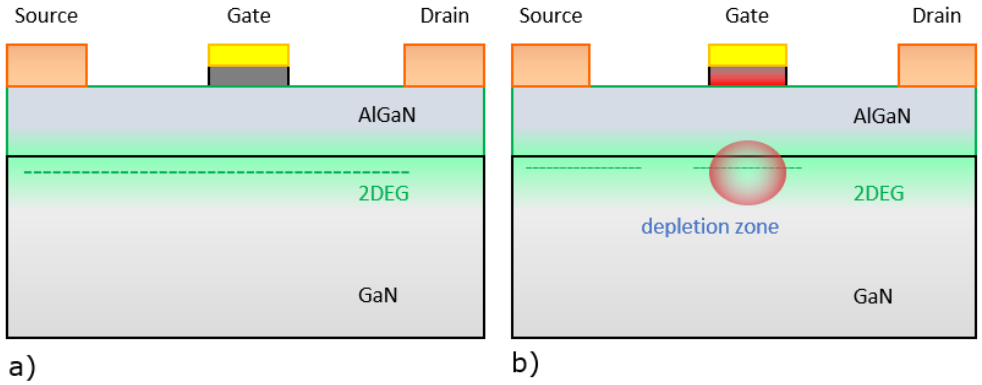


Figure 2.6.1 a) normally-on operation HEMT (D-mode), b) normally-off operation HEMT (E-mode)

To understand more in detail how a future use of GaN devices can be realized, it is worth having a look at the requirements, which must be fulfilled on the chip side. The device should be available as a bare die, which can be soldered or sintered on DBC substrates and frontside wire bonded or sintered. Also, a vertical device structure should be established to reach lower R_{Dson} and increased therefore the power density in the device. There should be a broad bandwidth of different chip sizes from different vendors for the voltage class of 1200V and the devices should be E-mode or MOS-controlled in normally-off mode configuration, to ensure the compatibility with normally-off driver topology. Therefore challenging device topologies are necessary to enable reliable the E-mode behaviour, which is due to the nature of the devices (e.g., 2DEG between GaN/AlGaN layers) and the development of production processes is still challenging.
Up to the moment of the edition of this version of this book no initiative at chip suppliers is visible to change the strategy towards the before-named requirements and therefore no "perfectly compatible" devices are expected in the near future.
But there are some promising ideas and trends that could bring in future the needed technological basis. One very interesting approach was researched in the range of the public funded project YESvGaN [2.42]. In the range of this activity, a vertical normally-off device was developed and fabricated which is based on MOS control. In Figure 2.6.2 a MOS controlled GaN device and a GaN HEMT are shown in comparison.

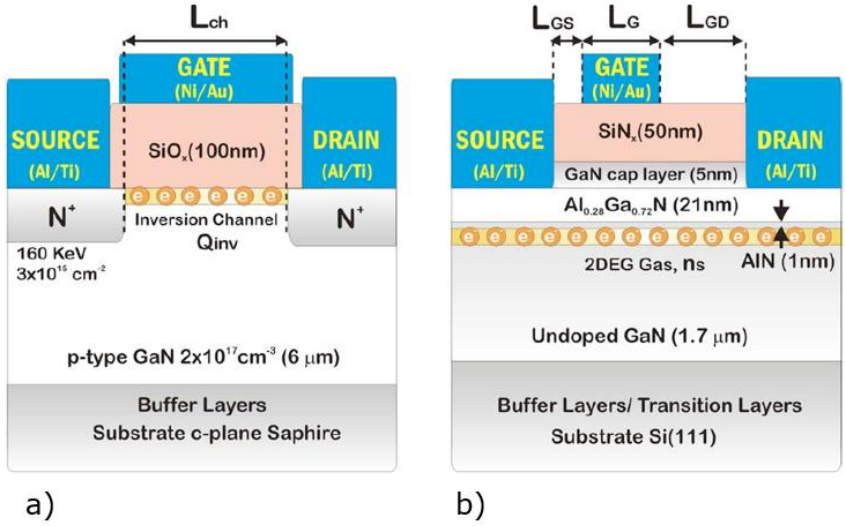


Figure 2.6.2 Schematic cross-section of a) GaN MOSFET, b) GaN HEMT [2.43]

The GaN MOSFET structure is based on p-GaN substrate with classic n^+ structure for drain and source contacts and formation of an inversion channel under gate contact. Here an intrinsic normally-off operation as well as low charge carrier mobility in inversion channel compared to a HEMT is given. But the technology basis for this topology is poorly given, e.g., GaN base material is not able to natively form high quality thermal oxide layers, which is resulting in poor interfaces inside MOS gate structure, further reducing carrier mobility due to Coulomb scattering on interface traps, as described before in the SiC section. In summary it seems to be a long way to reach the demands for an application in power modules and a sufficient maturity level.

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3 Power Semiconductor Packages

3.1 Assembly and connection technology

3.1.1 Packaging in general

Packaging of the power semiconductors has to fulfil the following main purposes:

- Provide electrical connection between one or more semiconductor chips and the electrical circuit
- Dissipate the heat generated during chip operation to a cooling unit
- Protect the semiconductor chip from harmful ambient influences
- Give space for marking, data code, manufacturer, component type and terminals

Depending on the packaging technology used, power semiconductors can be divided into the following categories:

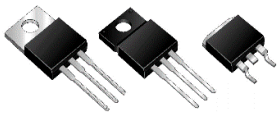
Technology	Double side soldered or sintered	Back side soldered/sintered front side bondwire connection	Pressure contact
Discrete			
Modules			

Table 3.1.1 Classification of power semiconductors according to packaging technology

Development goals of packaging are for many years cost reduction and along with this increasing power density. It can be achieved by:

- Improvement of heat dissipation
- Higher operating temperature and thermal cycling capability
- Optimization of inductances for faster switching and good current sharing
- Highly flexible packages for a series of different power ratings,
- Easy assembly in the inverter application
- Higher degree of integration (converter circuits)
- Integration of monitoring, protection and driver functions

3.1.2 Soldering

Soldering is the connection of two (metal) materials by means of liquid metal or a liquid alloy. Individual atoms in the solder then diffuse into the metal surface of the components to be soldered and a thin layer of an alloy made of solder and substrate is created. The prerequisite for void-free soldering quality are clean surfaces free from oxide for all connection components involved. For this purpose, fluxing agents are often used to clean surfaces; these agents are activated when the materials are warmed up for soldering. They also protect the surfaces from re-oxidation during soldering. Most fluxing agents must be removed again after soldering. Reducing gases, such as inert gas, can be used as fluxing agents. Applying a vacuum as soon as the solder has liquefied is a very good way of achieving void-free connections. Solder connections must conform with the RoHS Directive (Restriction of Hazardous Substances Directive) of the European Union.
A wide variety of soldering processes are available and are mainly distinguished by the manner in which heat is coupled to the part to be soldered. A process for soldering larger-areas like chips on a DBC is the use of soldering pastes consisting of little solder balls and a paste-like fluxing agent. The paste is applied onto one of connection parts using a dispenser, by screen or stencil printing, the second partner (e.g. the chip) is pressed into the paste. There it sticks by adhesion no additional equipment to fix the partner are necessary. Another method is the use of solder sheets also known as preforms. In this case a fixation of the preforms and chips to the substrate is necessary. After assembly and fixation, the components are heated in a second step until the solder melts. Common sources to apply the heat are infrared or hot steam.

Large-area solder connections between materials with different thermal expansion coefficients (Table 3.2.2) are critical. The bimetal effect causes bending and, under thermal cycling, solder fatigue which will ultimately result in solder failure. It is not reliable to solder large-area ceramics (DBC) as one single piece onto copper baseplates. This is one reason why power modules with larger power ratings are constructed from multiple DBC. This requires additional interconnection which costs space and increases the terminal resistance.
Soldering is a cost effective and well-established process. It will remain the most important assembly process for industrial modules in the next years, sintering is becoming more popular. Progress is done with different solder alloys with regards to power cycle capability.

3.1.3 Diffusion sintering (low-temperature joining technology)

Diffusion sintering is a process which replaces soldering in many cases. It may be considered as being far superior to soldering in terms of its long-term reliability. At a temperature of around 250°C, fine silver powder is sintered under high pressure to form a low-porous silver bond layer (Figure 3.1.1) between the parts to be connected.

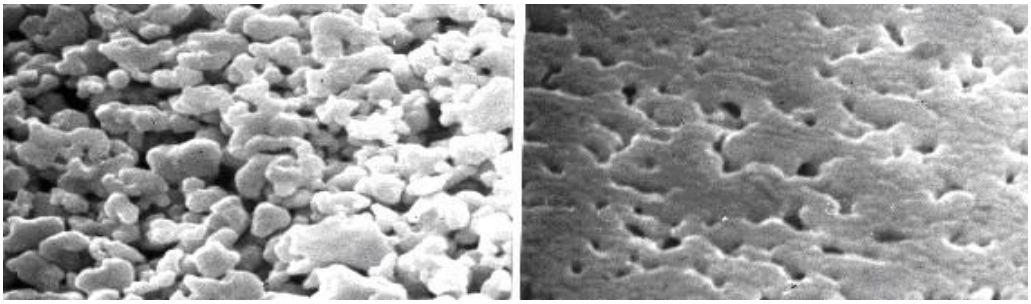


Figure 3.1.1 Silver powder before and after diffusion sintering

Sintered layers are stable up to the melting point of silver (962°C). Fluxing agent is not required. Sintered layers display better thermal, mechanical and electrical properties than solder (Table 3.1.2).

Property	Unit	Solder layer SnAg(3)	Ag sintered layer
Melting point	°C	221	962
Thermal conductivity	W/(m·K)	70	240
Electric conductivity	MS/m	8	41
Typical layer thickness	µm	70…250	20…40
Coefficient of thermal expansion	ppm/K	28	19

Table 3.1.2 Comparison of important properties of SnAg(3) solder and diffusion-sintered silver

The main advantage of the sintered layer is its resistance to temperature cycles; this is even true for high maximum temperatures. In contrast, solder tends to lose its strength when subjected to high stresses caused by temperature cycles. The great potential of sinter technology can best be demonstrated by specifying its homologous temperature. The homologous temperature (in %) of a material is defined as the ratio of operating temperature to melting point, both given in Kelvin. For homologous temperatures below 40%, materials are barely or not at all weakened by temperature. The creepage area lies between 40% and 60%. This is the area in which material properties are susceptible to mechanical stress. Above 60% their strength declines considerably; the material is regarded as unsuitable for this application (Table 3.1.3).
A sinter connection is mandatory for SiC MOSFET and a today's maximum operation temperature of up to 200°C. Sintering is also advantageous with regards to the reduced power cycle capability of SiC compared to Si devices.
The disadvantage of diffusion sintering was in the past that only materials with a precious metal surface could be connected. Nowadays, direct sintering on copper is also being introduced.

Homologous temperature for	Solder layer SnAg(3)	Ag sintered layer
Operating temperature 100°C (373 K)	76%	30%
Operating temperature 150°C (423 K)	86%	34%
Operating temperature 175°C (448 K)	91%	47%
Melting temperature (100%)	221°C (494 K)	962°C (1 235 K)

Table 3.1.3 Homologous temperature in % for tin silver solder SnAg(3) and a silver diffusion-sintered layer at different operating temperatures

In series production, sintering technology was first used to replace solders in chip-to-DBC connection. SKiM 63/93 modules were the first fully solder-free modules, followed afterwards by SKiiP 4. Sintering could also be used to eliminate the shortcomings of large-area DBC to baseplate soldering [3.1] or those of wire bonded connections. Examples of the latter option are presented in Figure 3.1.2.



Figure 3.1.2 Double side sintered chips using a flex foil for the top side contact or copper litz wires [3.2] as substitutes for conventional bond wire connections

3.1.4 Wire bonding

Wire bonding is often used to connect a power semiconductor chip surface to the DBC tracks, with other chips or to connect DBC to terminals and so on. This is a cold-welding process where ultrasonic energy is used to connect an aluminium wire (about 100µm to 500µm thick) to a surface made of aluminium, copper or gold. This process takes place at room temperature. Since a bond wire is limited in its current capability, several bond wires are used in parallel for higher amperages. Stitching, i.e. multiple bonding of a wire on a surface, is employed to distribute the current more evenly on a chip (Figure 3.1.3).

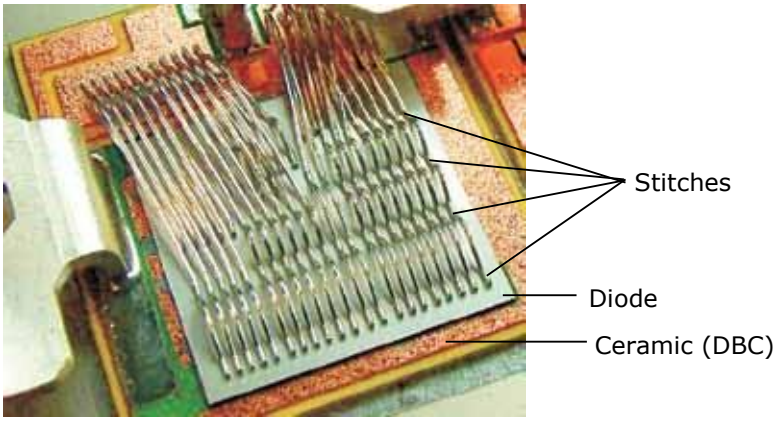


Figure 3.1.3 Many parallel, "multi-stitched" bond wires on a diode chip of 500mm² area

With the introduction of the sinter process for the backside connection of the chip, the aluminium bondwire became the limiting factor with regards to power cycle capability. To overcome the limitation copper [3.3] or aluminium cladded copper bond wires (AlCu) has been introduced. The advantage of AlCu bond wires is that the standard Al chip surface can be used [3.4], the disadvantage is that it does not reach the power cycle capability of pure copper.
Pure copper bonds require a special chip surface with copper. The reason is that copper is much stiffer and requires higher energies for melting during the ultrasonic bonding process which can destroy the filigree structures at the chip surface. Copper can be applied directly during the chip front side metallization process which makes the chip more expensive or by sintering an additional copper piece on top of the chip surface which is an additional step in the module production [3.3].

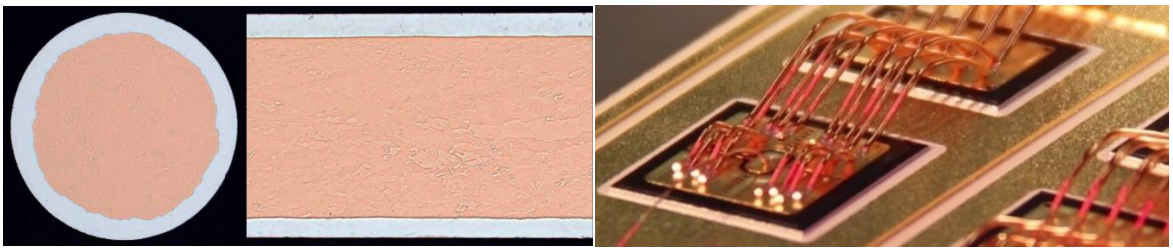


Figure 3.1.4 Cross section through AlCu bond wires [3.4] and pure copper bonds using Danfoss bond buffer (DBB) technology ™

Al-wire-bonding is a very flexible and cost-effective solution as already mentioned for soldering. This means that this technology will remain the major connection method in the near future, at least for silicon chips.

3.1.5 Pressure and spring contact

In product data sheets and technical explanations, a distinction is made between these contacts, but in terms of physical principle they are similar. Spring force is necessary for good electrical or thermal contact. It can be applied directly by a spring or by an external clamping unit with spring characteristic.
In contrast to soldering, diffusion-sintering and wire-bonding, pressure contacts are not metallurgical joints but a form-fitting connection method. This means the pressure-contacted partners can be move against each other and can glide on each other. Tensions that would arise in the case of metallurgical joints during temperature cycles owing to the different thermal expansion coefficients of the connection partners thus do not appear or to a very limited extent only. Pressure contacts do not display fatigue caused by temperature change, as is the case with soldered and wire-bonded connections. This explains the high reliability of pressure-contacted components. Care has to be taken with the contact partner to avoid fretting. A differentiation should be made between large-surface and small-surface ("dot-shaped") pressure contacts.

Large-surface pressure contact

It is used for electrical and thermal contact. The surfaces of the parts which are pressed against each other under high force, must be clean and planar. In addition, the contact surfaces must not be prone to cold welding, because this would prevent them from "floating". This can be ensured by selecting suitable surface pairs. Examples of large-surface pressure contacts are disk cells. With a suitable design, double-sided cooling can be obtained by clamping the component between two heatsinks, thus cutting the thermal resistance almost in half. Pressure contacts are used in rectifier Modules (Figure 3.1.5) for diodes and thyristors to achieve high overload and surge currents as well as an excellent power cycle capability.

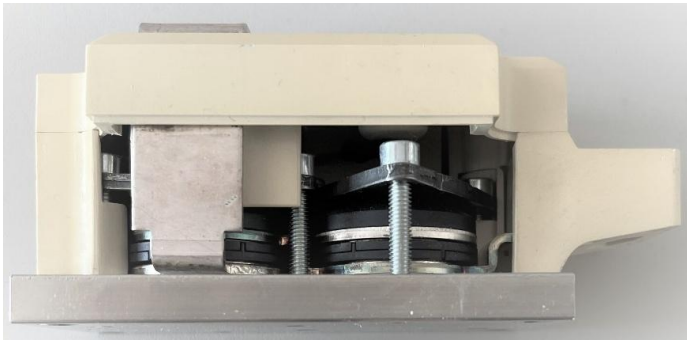


Figure 3.1.5 Inside view of a pressure contact SEMIPACK

Another kind of large-surface pressure contacts are module/heatsink connections. Here, pre-bent base plates provide the spring characteristics.

Small-surface pressure contact

Here, the contact area is line-shaped or almost dot-shaped. This contact is used only for electrical contact. Extremely small contact area requires just a small force to apply high pressure to the contact area. The pressure is so high that oxide layers or other surface pollution of the small-surface contact partner can be penetrated, thus ensuring safe and reliable contact. Such contacts

are used in the form of spiral springs for control terminals as well as in MiniSKiiP modules with S-shaped springs.

SKiiP® Technology

SKiiP is a purpose-developed pressure-contact technology which provides advantages for all module power rating classes in terms of performance, service life, reliability and costs. It is a combination of both contacts with the large-surface for the thermal contact and small-surface for the electrical contact.
The most important characteristic of SKiiP is the elimination of soldered connections to the baseplate and terminals. For this purpose, the insulating substrate (DBC) - together with the soldered or sintered chips - is pressed directly onto the heatsink by the case, pressure elements or the terminals. The main advantage of this layout is that there is no metallurgical joint or large-area soldering between the ceramic substrate (thermal expansion coefficient is about $4…7 \cdot 10^{-6}$/K) and the baseplate (thermal expansion coefficient of copper is about $17.5 \cdot 10^{-6}$/K). This helps to avoid the high mechanical tension between baseplate and ceramic parts that occurs in baseplate modules due to temperature changes. Please refer to chapter 3.3 for more detailed information on the properties of SKiiP modules.
Several power module families covering a wide performance range are based on SKiiP technology. Besides the SKiiP module family, this includes all SKiM, MiniSKiiP, SEMITOP and most SEMIPONT modules.

3.1.6 Welding

The welding of power terminals is another step in the ongoing development to eliminate solder connections from power modules. It can be distinguished between ultrasonic welding [3.5] and laser welding of copper terminals.
The advantage of ultrasonic welding is that relatively thick copper parts (1…2mm) can be welded to the only 0.3mm thick copper of a DBC (Figure 3.1.6). The equipment can be relatively flexible adapted to different terminal like wire bonding machines. The disadvantage is that relatively high energy and forces are necessary for the welding process, which stresses the ceramic underneath. Furthermore, are the welding tools relatively bulky so that some space around the terminal is required.

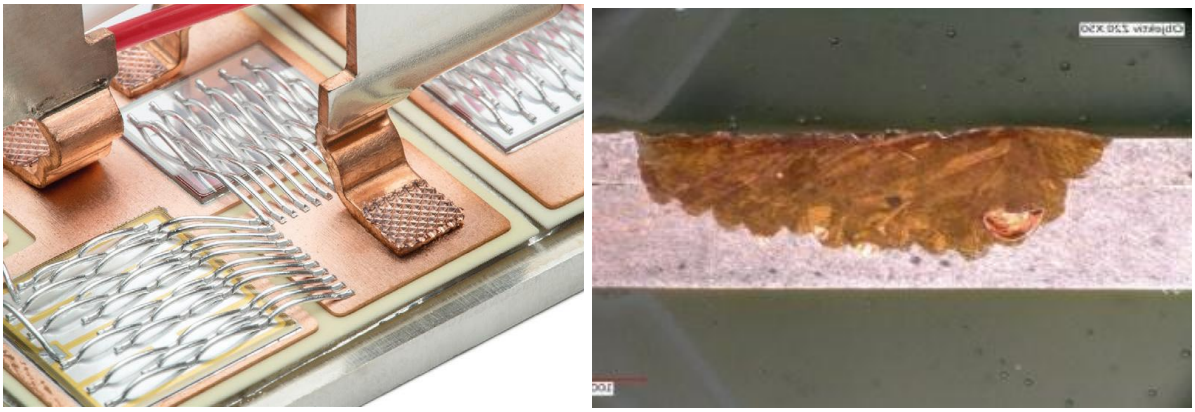


Figure 3.1.6 Left Ultrasonic welded main terminals [3.6], right cross section through a laser welded copper terminal

Laser welding on the other hand can weld only copper parts which have an equal or thinner thickness as the partner underneath. The laser beam is applied to the surface of the terminal in short pulses, melt the upper copper partner completely in a small spot and the lower partner on the surface and forms in this way a solid bond to the layer underneath. The welding itself has low space requirements, but "Eye contact" is required from the laser system to the welded parts. It is an ideal technology for high volume production lines with identical contacts. Using welding as the contact to external busbars or capacitor blocks enables ultra-low stray inductances in the commutation circuit since no screw, with the required isolation space, has to run through overlapping DC terminals.
In combination with the Danfoss Bond Buffer technology also copper ribbon bonds can be welded to chip surface and DBC. Although the technology is somewhat more expensive than wire bonding, it is many times superior in terms of power cycle capability.

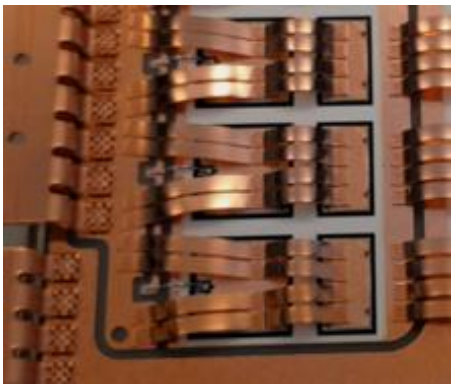


Figure 3.1.7 welded copper ribbon bonds on IGBT and diode chips with Danfoss Bond Buffer technology

3.2 Functional properties of modules

3.2.1 Insulation

3.2.1.1 Terms

The power module's insulation system must withstand the electrical stress over the entire service life in the environment of the application. Over the years, much experience has been gained with insulation, which has been documented in several standards. However, no explicit requirements for insulation coordination are specified in the product standards for power modules. Therefore, their insulation coordination is carried out according to the regulations of their most important applications and is described in chapter 10.3 and more precisely in [3.7], using the examples of two typical applications. For the purpose of insulation coordination, a distinction is made between three hierarchically graded requirements. For power modules, this division means the following:

Functional insulation separates potentials within a circuit and considers purely functional, but not safety relevant aspects. In power modules this is between the input and output terminals or between the power terminals like AC, DC or brake chopper and control terminals like gate or emitter.

Basic insulation separates grid-supplied circuits from earthed exposed parts and is thus vital for safety. A breakdown of the insulation does not result automatically in a danger of life due to the earthing of the exposed parts. In power modules this is between earthed heatsinks or module baseplates on the one hand and module power terminals on the other hand.

Protective separation realized by reinforced or double (2 times -basic) insulation separates grid supplied circuits from unearthed exposed parts and from control circuits, if they are directly connected to other control circuits which have exposed components. No further protection is provided for equipment users. A breakdown of this insulation could be fatal because the unearthed exposed parts can be shifted to the grid voltage. This is the reason why stricter requirements must be fulfilled. Protective separation is between module power terminals and it's insulated module-internal control circuit or sensors. These sensors are for current, voltage or temperature, whose outputs may be connected to the control circuit with exposed parts. Further protective separation is necessary between the power circuit and the control circuit with exposed parts on power module driver boards.

3.2.1.2 Hardware realisation

Substrates

DBC substrates (Direct Bonded Copper) are most commonly used for ceramic insulation between the inner parts at high electrical potential and the mounting surface or baseplate of insulated power modules. Here, the insulator is often made of aluminium oxide Al_2O_3; the double-sided metal layers are made of copper. The metal / ceramic connection is made at temperatures of just above 1000°C with the aid of low-viscosity copper / copper oxide eutectic. The ceramic of the future could be Si_3N_4 (silicon nitride) because of a higher mechanical strength, better thermal properties and a good overall cost performance ratio. Less often AlN (aluminium nitride) is used as ceramic layer, with even better thermal properties but it is more expensive. For this reason, AlN is largely

preferred for modules with high insulation voltages (thicker insulating ceramics), since increased dielectric strength plus better thermal conductivity can be utilised at the same time.
AMB ceramics (Active Metal Brazing) are almost equivalent to DBC substrates. These are produced by soldering copper or aluminium foils on to the Al_2O_3 or AlN ceramic with the aid of titaniferous hard solder.
The track structure for the module circuitry is etched into the upper copper surface. The lower side of the ceramic substrate is soldered to the module baseplate or directly pressed onto the heatsink surface by means of suitable case designs.
One example of plastic insulation is IMS substrates (Insulated Metal Substrates, Figure 3.2.1). Plastic materials, usually thin layers of polyimide or epoxy, have a much higher specific thermal resistance than ceramic insulators, but the layer can be much thinner. IMS substrates are often used in the low-cost / low-power range but with special adapted materials for power modules as well. The insulating material is in direct contact to the module baseplate. The upper copper layer is attached on top of the foil and structured by etching. The main advantages of IMS technology are low costs, the possibility to realise filigree track structures (possible integration of driver and protection devices) and high mechanical stability. One disadvantage of this very thin insulating layer, however, is the relatively high coupling capacitance towards the mounting surface. Furthermore, the thin upper copper layer only provides for comparably low heat spreading. This can be improved by adding metallised heat spreading layers underneath the chips.

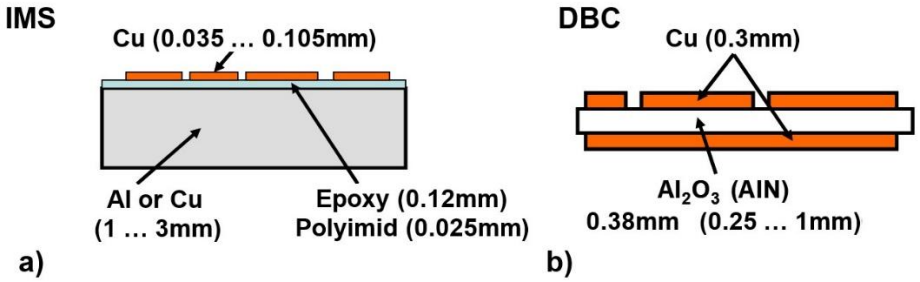


Figure 3.2.1 Comparison of IMS (a) and DBC (b) structure

The advantage of ceramic substrates is a thermal expansion coefficient very close to that of silicon. In contrast, IMS expansion is determined by the material of the baseplate (copper or aluminum), which leads to high stresses between the substrate and the soldered silicon chip when the temperature changes.
The implementation of semiconductors with higher voltage ranges places increasing demands on modules to provide high insulation voltages and a high partial discharge stability. Dielectric strength and partial discharge stability are dependent on the thickness, the material and homogeneity of the chip bottom insulation, the module case and filling materials and sometimes on the chip arrangement, too. Present-day transistor modules are subject to insulation test voltages between $2.5kV_{rms}$ and $9kV_{rms}$, verified for every module during production. Figure 3.2.2 shows the maximum attainable insulation voltages for different insulating substrates when using common standard substrate thicknesses.

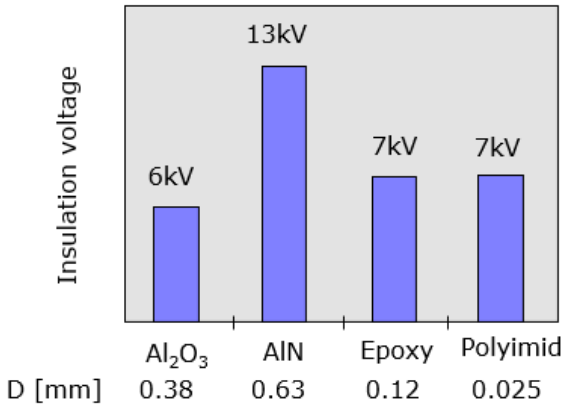


Figure 3.2.2 Insulation voltages for different insulating substrates

Housing

Plastic materials are used as an insulating material for the housing to provide electrical insulation between live parts, terminals and the baseplate (semiconductor modules), ceramic insulators are used in the higher power range e.g. for disc rectifier.
The outlines and internal structure of Semikron Danfoss power modules are designed according to the standard EN61800-5-1. If not stated otherwise in the datasheet, the dimensioning of the insulation depends on the blocking voltage class of the module. Modules of the same product line with the same housing size are designed for the highest available blocking voltage of this module type. Table 3.2.1 shows a typical specification for the coordination of insulation according to EN61800-5-1, used by Semikron Danfoss.

Blocking voltage class	DC link voltage	Grid voltage	Grid configuration	Overvoltage category	Altitude	Pollution degree
600V/650V	400V	230V	star (wye) earthed TN-C-system	3	2000m	2
1200V	900V	480V				
1700V	1200V	690V				

Table 3.2.1 Typical specification Semikron Danfoss uses for the coordination of insulation according to EN61800-5-1 [3.27]

Insulation can be implemented as clearance, creepage, solid insulation or a combination of these:

- *Clearance* designates the air space between conductive parts. It must be so large that flashover is prevented at all times if voltage is applied.
- Also, the *creepage* distances are important, as these must be at least the length of the clearances. Pollution on the surface of insulating material can create a conductive path across it. A performance value of insulating materials is the comparative tracking index CTI (test conditions defined in the IEC 60112). The more resistant a housing material is, the higher the CTI-value and the shorter the creepage track may be. Low CTI values can be compensated by larger creepage distances (see also IEC60664-1 for more information). CTI values of housings of current power modules are between 175 and > 600.
- *Solid insulation* is insulation not created solely by air or gas. To verify if the solid insulation withstands the voltage load, three tests can be performed: Impulse withstand voltage test, AC or DC voltage test and Partial discharge test.

Moulding compound

Power modules are filled with a mould to provide insulation between different electrical potentials of an internal circuit. The trenches on the DBC, which realise the internal electrical circuit, are not wide enough to ensure insulation in air.
Two kinds of potting compounds are widely used, a silicone gel based soft mould with an electrical field strength of about 20kV/mm which is 10 times higher than air and an epoxy resin based hard mould with a field strength of more than 60kV/mm. The potting compounds must be free of air bubbles to prevent partial discharge. In case of silicone, it is achieved by an almost water-like liquid consistency before curing and in case of epoxy resin this is ensured in a vacuum chamber. The advantage of silicone gel is the easy processing and it absorbs any kind of mechanical and thermomechanical stress. The disadvantage is that it protects the semiconductors only for dust and particles and not for humidity. Humidity of the surrounding air is also applied to the semiconductor with a delay of some hours and in the other way it takes also hours to get the humidity out for example after condensation has happened. Hard mould on the other side provides a certain degree of protection against moisture but it is more susceptible against thermomechanical stress. Special care has to be taken that the CTE of the compound material matches to the other materials used in the module.

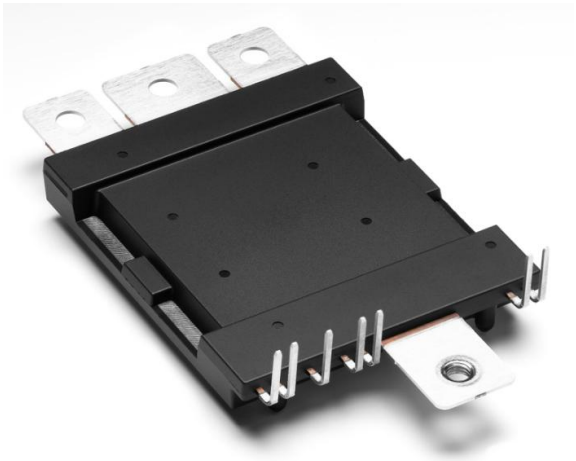


Figure 3.2.3 Module with hard moulded housing

3.2.1.3 Testing

The module insulation test voltage V_{isol}, given in the Semikron Danfoss datasheets is tested by means of routine in-production module testing - as the RMS value (AC voltage, 50Hz) between the input terminals / control terminals (all terminals connected) and the insulated module baseplate. A general explanation of differences between routine and type test are given in chapter 10.3.5.
The typical test periods of high voltage routine test are 1s or 5s. Though occasionally longer test periods like 60s are specified. For semiconductor devices UL1557 describes the possibility to shorten the test period by increasing the test voltage. The rated voltage with a test time of 60s is increased to 120% for 1s.
The test conditions for the Semikron Danfoss high voltage test are given in the datasheet (typically with the V_{isol} parameter). If the given test duration is 5s or 60s it is the type test condition. Shorter test durations like 1s and 3s are routine test conditions.
Alternatively, an insulation test can be performed as a DC test for $V_{isol(DC)} = \sqrt{2} \cdot V_{isol(AC)}$. Insulation testing for sensors contained in the module and their environment, as well as for insulation in intelligent modules is done in the same way. Power modules with large base plates can have relatively large capacitances (up to ≈10nF) between both sides of their substrate. For these modules DC tests are recommended.
All insulation voltage tests are performed at an ambient temperature of 15…35°C, a relative humidity of 45…75% and an atmospheric pressure of 860…1060hPa. The insulation test (dielectric test) is considered passed if no electrical breakdown has occurred, i.e. small leakage currents that occur are irrelevant.
The V_{isol} datasheet values often shows higher voltages than EN61800-5-1 requests. This is because the modules can be used according to other standards, such as railway applications. It is therefore not possible to conclude from the given test voltage which specification was used for insulation coordination.
To be able to use power modules across multiple applications, manufacturers specify test voltages as high as possible (within the scope of technical feasibility), for example 2.5kVac/1 min…4kVac/1min…4.5kVac/1s for 1200V IGBT modules, 4kVac/1min…5.6kV/1 s for 1700V IGBT modules, 6kV/1min for 3300V IGBT modules and 10.2kV/1min for 6500V IGBT modules. Semikron Danfoss also tests IGBT and diode modules at 9.5kV/1min in line with non-standard customer requirements.

3.2.2 Increasing current rating by paralleling

Highest chip current rating of IGBT chips today is about 300A, to produce modules with higher current rating a paralleling of chips is necessary. But even if a single chip of the required current rating is available, paralleling is advantageous. A 300A IGBT module is typical constructed by 4x75A or 3x 100A chips. The main reasons are

- thermal spreading (see Figure 3.2.11)
- using of the same internal module construction for a whole family e.g. from 225A (3x 75A) up to 900A (3x300A) only by changing different chip sizes at the same position.

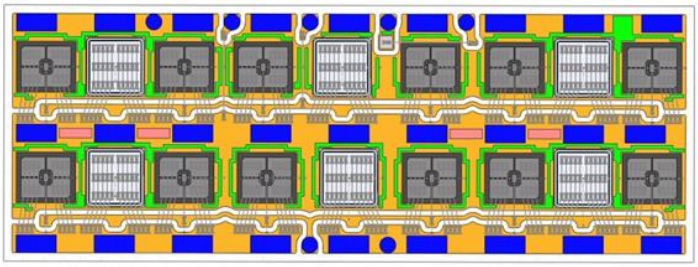


Figure 3.2.4 Parallel connection of 6 IGBT and 3 diodes per switch in a halfbridge configuration of a SKiM93

The module manufacturer takes care for a good current sharing between the parallel chips under static and switching conditions. Often compromises have to be found between electrical and thermal performance. Wider distances between the chip reduce the R_{th} but from electrical point of view the chips should be as close as possible together to minimize parasitic inductances and resistances between the chips. Differences in the individual lead resistance ($r_{cc'-ee'}$) have differences in static current sharing as a consequence, differences in the commutation loop inductances per chip position cause different switching speed and losses. Both differences can be minimized by parallel current paths in the third dimension like it is shown in Figure 3.2.21 and Figure 3.3.4. Almost all modern IGBT have PTC (positive temperature coefficient) behaviour for currents >20% of the nominal current. Which means that a hotter IGBT has a higher forward voltage as its parallel neighbours and takes a lower share of the total current. Freewheeling diodes have an NTC behaviour which makes a paralleling more difficult. A hotter diode would take even more current which produces higher losses and even higher temperatures. This issue can only be solved by a narrow parameter distribution or with selection into forward voltage groups. In [3.8] it was shown that with real distribution of forward voltages and a probability of 1ppm the highest current mismatch happens between 3 diodes in parallel and can be expected around 10%.
An integrated gate resistor R_{Gint} per chip (IGBT or MOSFET) is essential for an almost synchronous switching of the transistors. The resistor decouples the gates and allows small differences in the gate voltage during switching according the individual threshold voltages and transfer characteristics of the chips. In addition, R_{Gint} is necessary to dampen oscillations in the LC-network of the power module with the transistor as amplifier during operation in active mode (switching transients, short circuit).

3.2.3 Heat dissipation

3.2.3.1 Thermal resistance R_{th} and thermal capacitance C_{th}

To utilise the theoretical current capability as far as possible, power losses have to be optimally conducted through a stack of layers, for modules including the insulation layer, to the heatsink. The quality of the heat transfer for P_{tot}, which is generated during forward on-state, blocking state and during switching is reflected in a small temperature difference $\Delta T_{j\text{-}s} = T_j - T_s$ between chip (chip temperature T_j) and heatsink (heatsink temperature T_s). In the past, a "v" for "virtual" preceded the index of the junction temperature (T_{vj}), since "the" junction temperature does not exist, but merely an equivalent measurement or computed value. The property to dissipate heat is quantified by the stationary thermal resistance $R_{th(j\text{-}s)}$ or transient thermal impedance $Z_{th(j\text{-}s)}$.

$$R_{th(j-s)} = \frac{T_j - T_s}{P_{tot}};\ Z_{th(j-s)}(t) = \frac{T_j(t) - T_s}{P_{tot}}$$

An inner $R_{th(j\text{-}c)}$ or $Z_{th(j\text{-}c)}$ (chip to baseplate) and an outer thermal resistance or impedance $R_{th(c\text{-}s)}$ or $Z_{th(c\text{-}s)}$ (baseplate to heatsink) is specified as for modules with baseplate (case rated devices – the maximum current is specified for a given case temperature):

$$R_{th(j-s)} = R_{th(j-c)} + R_{th(c-s)}$$

$$Z_{th(j-s)} = Z_{th(j-c)} + Z_{th(c-s)}$$

For baseplate-less modules (heatsink rated devices – the maximum current is specified for a given heatsink temperature), it is not possible to measure a case temperature without seriously interfering with the thermal system. For this reason, only the total resistance between chip and heatsink is specified for these components. The value is valid for a certain TIM, layer thickness and mounting force.

Low-power components are also specified with reference to the ambient or lead temperature. Figure 2.5.13 shows a schematic of a module with baseplate. Another way to specify a R_{th} is the usage of physical and geometrical properties:

$$R_{th} = \frac{d}{\lambda \cdot A}$$

d: material thickness, λ: heat conductivity, A: heat flow area

The formula can be used to deduce which module quantities influences the $R_{th(j-s)}$ and $Z_{th(j-s)}$:

- Chip (area, thickness, geometry and layout)
- DBC substrate (material, thickness, routing)
- Material and quality of the chip/substrate connection (solder alloy, sinter material, ...)
- Presence of a baseplate (material, thickness)
- soldering of the substrate to the baseplate (material, quality)
- Module assembly (surface qualities / thermal contact to heatsink, thickness and quality of TIM)

In conjunction with the equation for thermal capacitance:

$$C_{th} = s \cdot V$$

s: heat storage characteristic, V: volume

the elements of the thermal equivalent circuit (so called Cauer network) can be calculated from the geometry layer by layer. Heat spreading must be factored into area and volume calculations. A conflicting effect that has to be considered is mutual chip heating in complex power modules by thermal coupling. The calculated theoretical thermal resistance value will often be lower than the actual measured value. The reason for this often lies in the uncertainties observed in heat spreading and thermal coupling, as well as impurities at the border layers which have not been considered in the modelling. For this reason, this type of modelling is not particularly well suited to complex power electronic systems. Normally, the computed R_{th} values are adjusted to the measured total of R_{th} with the aid of a weighting factor.
Furthermore, the thermal conductivities of especially semiconductors and ceramics are temperature dependent, which should be taken into account when comparing simulated or measured R_{th} values at different temperature levels.

Material	**Thermal conductivity λ [W/(m·K)] at 25°C**	**Heat storage coefficient s [kJ/(m³·K)]**	**coefficient of thermal expansion α [10^{-6}/K]**
Silicon	148	1650	4.1
SiC	412	2203	3.4
Copper	394	3400	17.5
Aluminum	230	2480	22.5
Silver	407	2450	19
Molybdenum	145	2575	5
Solder alloy	50…70	1670	15 – 30
Al_2O_3	24	3025	8.3 (for DBC incl. copper)
Si_3N_4	90	2190	6 (for DBC incl. copper)
AlN	180	2435	5.7 (for DBC incl. copper)
AlSiC (75% SiC)	180	2223	7

Table 3.2.2 Thermal conductivity, heat storage coefficient and coefficient of thermal expansion for frequently used materials in power electronic packaging

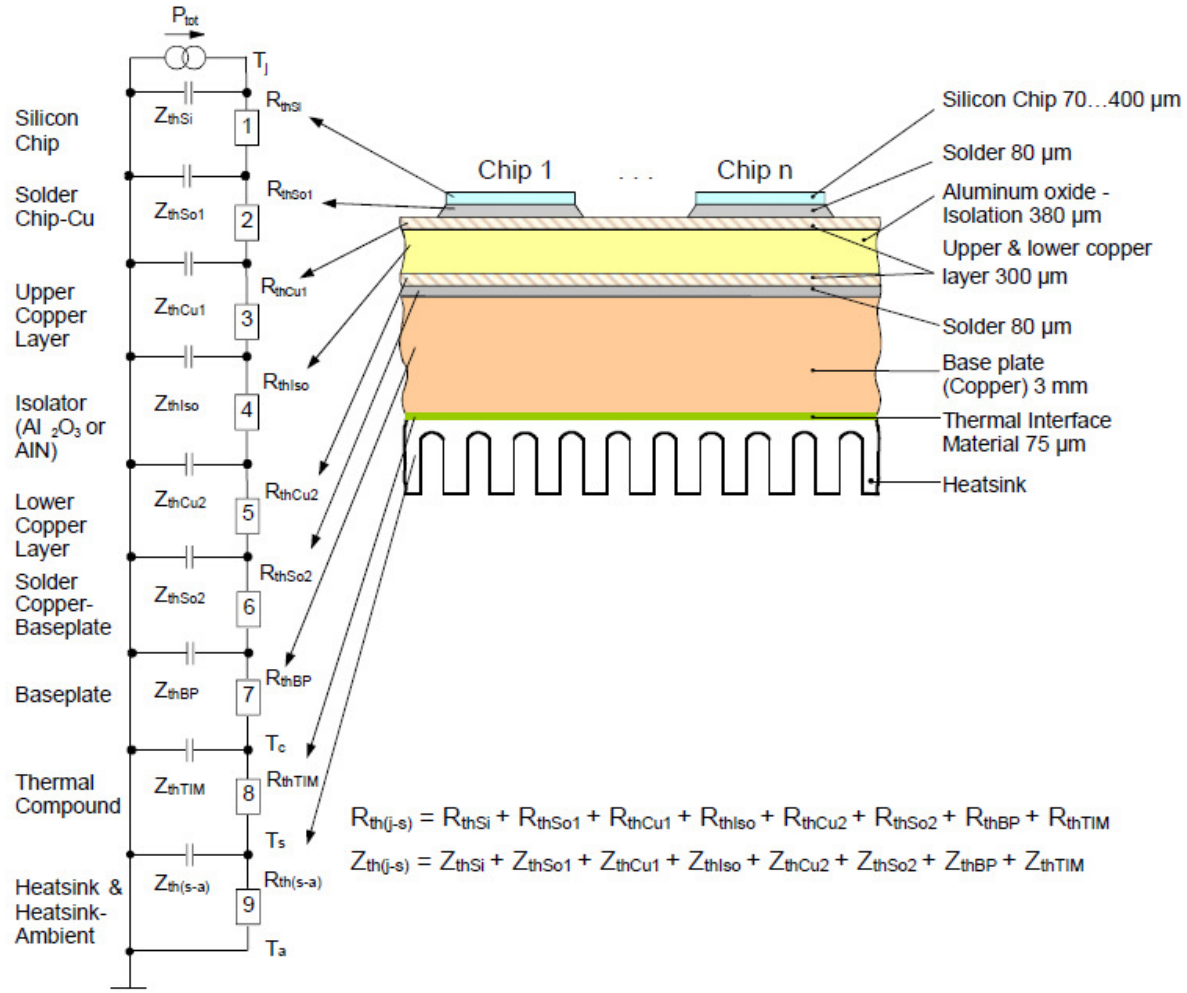


Figure 3.2.5 Basic structure of a power semiconductor module and physical modelling of the thermally relevant layers

In combination with the cooling and ambient conditions, $R_{th(j-s)}$ determines the maximum module ratings for thermal losses. The development of power semiconductor modules is therefore always associated with the reduction of the number of layers (Figure 3.2.6), the reduction of layer thickness (0.63 mm → 0.38 mm for ceramics) and the use of materials with improved thermal conductivity (AlN, graphite). This development, however, is limited by insulation voltage and mechanical strength requirements.

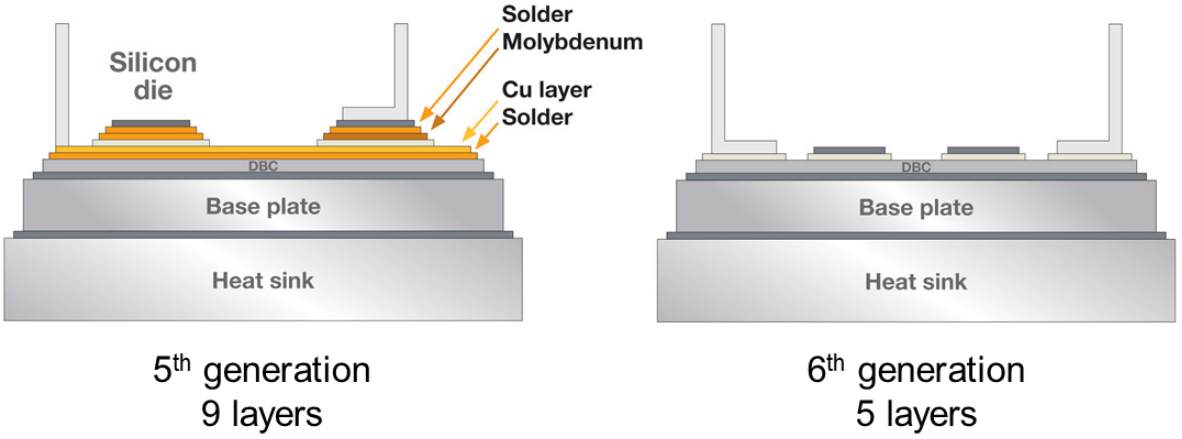


Figure 3.2.6 Development of SEMIPACK 1: thermal resistance reduced by the omission of layers

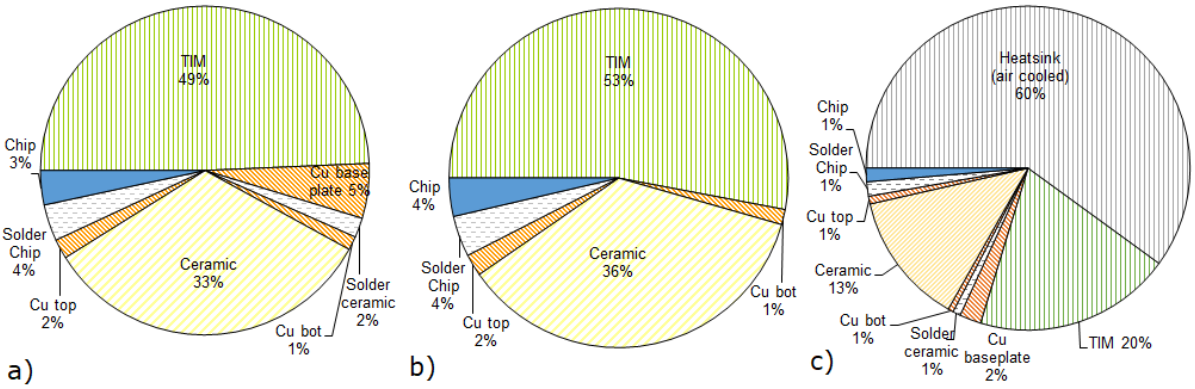


Figure 3.2.7 Influences on the thermal resistance of a 81mm² chip at a Al_2O_3 DBC substrates: a) on Cu baseplate and 100µm TIM; b) without Cu baseplate and 25µm TIM; c) inclusive an air cooled heatsink

Figure 3.2.7 illustrates the shares for the aforementioned variables affecting R_{th} for the most common module layouts using Al_2O_3-DBC substrates with or without copper baseplate.
Looking only on the module (Figure 3.2.7 a) and b)) is the biggest share of the $R_{th(j-s)}$ (approx. 50%) caused by the thermal paste (TIM – **T**hermal **I**nterface **M**aterial with λ=0.8W/(m·K)). This seems strange at first, since the baseplate promises better heat spreading and thus a lower influence from the thermal paste layer. However, baseplate modules require a thicker TIM layer, which cancels out the advantage of better heat spreading.
Module insulation "ceramic" accounts for the biggest part of the internal thermal resistance. The alternative, however - for example external insulation by means of foil - would be even worse. Compared to today's standard type Al_2O_3 with a purity of 96% (thermal conductivity λ = 24 W/(m·K)), improvements can be achieved by Si_3N_4 or AlN.
Taking the heatsink in to account (Figure 3.2.7 c)), then it becomes clear that the overall thermal performance is dominated by the heatsink. Improving the TIM-Layer or the Ceramic layer by 50% will reduce the total $R_{th(j-a)}$ only by 6…10% in this example.

3.2.3.2 R_{th} of modules with parallel chips

Parallel connection of chips is used to achieve higher current ratings. Each of these chips has an individual junction temperature and also case and heatsink temperatures underneath the chip positions are different. The measurement method used to determine the (virtual) junction temperature T_{vj} delivers an area related average value of the parallel chips (doted red line in Figure 3.2.8). The term "virtual" is normally not used because whenever we talk about junction temperature, we mean "virtual junction temperature".

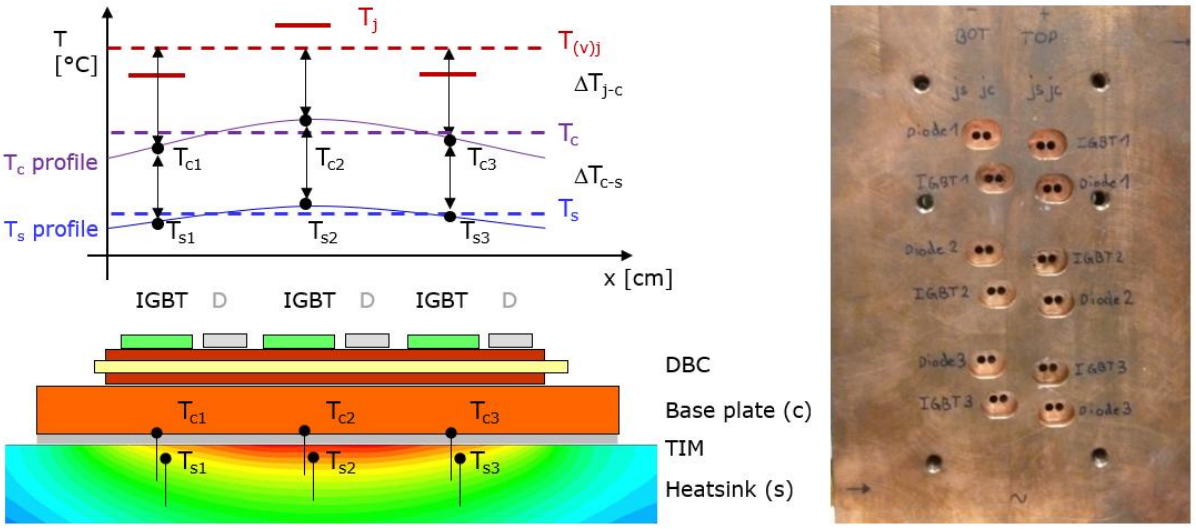


Figure 3.2.8 Measurement points for T_c and T_s in a module with parallel chips, principle drawing left and example of a special prepared heatsink right

If T_c would be measured at the hot spot in the middle position only, then the temperature difference $\Delta T_{j\text{-}c}$ would be small and therewith the $R_{th(j\text{-}c)}$. The same applies to the $R_{th(c\text{-}s)}$. For that reason the temperatures $T_{c1..n}$ and $T_{s1..n}$ are measured underneath each chip position and the average temperature is calculated. The average of the junction temperature and of case or heatsink temperature are used to calculate the R_{th}:

$$R_{th(c-s)} = \frac{T_{(v)j} - \text{average}(T_{c1} \dots T_{cn})}{P_{switch}}$$

3.2.3.3 Heat spreading

Figure 3.2.9 shows a computed value for the temperature curve in the individual layers of a baseplate-less module with undisturbed heat spreading. Here, the thermal conductivity of the individual layers and the heat flow area have been taken into account. Consequently, enlarging this area by improving heat spread would reduce the thermal resistance of the subsequent layer. Although a thinner copper layer would lead to a lower thermal resistance in a one-dimensional model, in the real three-dimensional object R_{th} would in fact increase as a result of reduced heat spreading. Thicker metal layers in the DBC substrate provide thermal advantages; however, they also increase thermal stress within the substrates.
The thermal resistance depends strong on the structure of the upper copper area, which is used as chip carrier and internal electrical connection system for the module. While the lateral heat flow in the copper layer below the ceramic is virtually unaffected, heat spreading is limited by the geometric dimensions of the copper layers under the chips. For example, in [3.9] it was determined that for a 42mm² chip on an Al_2O_3 DBC ceramic substrate, the $R_{th(j\text{-}c)}$ increases by around 15%, if the copper area equals the chip area, as compared with a case with unimpaired heat spreading.
Heat spreading depends not only on the material properties of the given layer, but also on those of the subsequent layer. A sufficiently high potential (temperature difference) must build up so that the heat flow can overcome a poorly conducting layer. This will then result in increased transverse heat conduction (heat spreading) in a layer with good thermal conductivity located above.

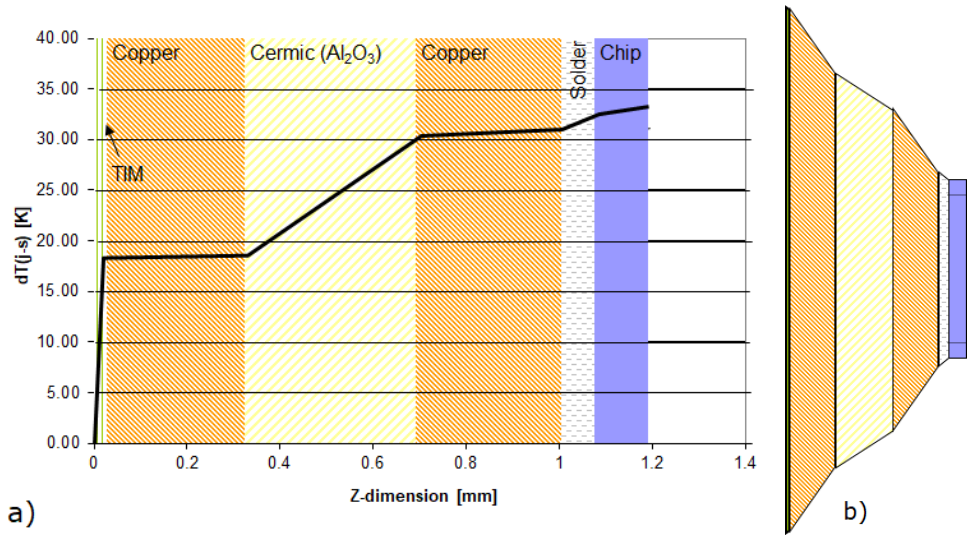


Figure 3.2.9 Layer structure with heat spreading (b) and typical temperature profile (a) for a baseplate-less module (0.38mm Al_2O_3 ceramic, 25µm thermal paste, TIM)

In accordance with the equation for thermal resistance, R_{th} should decline in inverse linear proportion to the chip area. The percentage gain in area due to heat spreading is lower for large chips than for small chips. For Example: a 50mm² chip (7.1mm·7.1mm) with 5mm spreading in any direction uses 290mm² for the heat transfer into the heatsink. A doubled sized chip of 100mm² (10mm·10mm) uses under the same conditions 400mm². The ration of the areas changes from 1:2 at the chip to 1:1.4 in the TIM layer. Figure 3.2.10 shows this effect on the $R_{th(c\text{-}s)}$. The consequences are a) that small chips are used with higher current density and b) that two 50A chips can carry higher currents than one 100A chip.

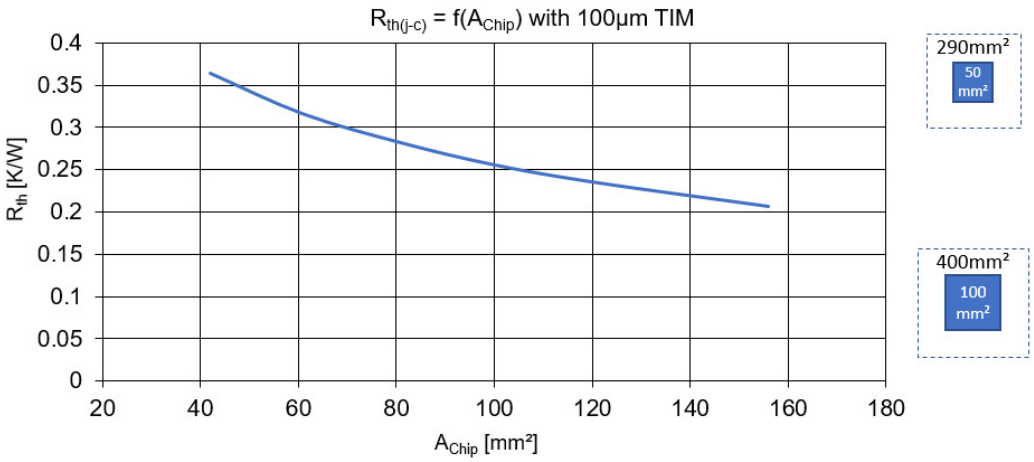


Figure 3.2.10 $R_{th(c-s)}$ of a baseplate module for a single chip as a function of the chip area for undisturbed heat spreading

That means better heat spreading can also be achieved by changing from a single heat source to multiple heat sources for example by paralleling chips in a module or also on system level by paralleling modules on a heatsink. For the sake of small module geometry, more or less intensive thermal coupling has to be accepted if transistor and diode chips are positioned close to one another. As a rule of thumb, it can be assumed that the R_{th} does not change anymore if the distance between the chips has reached 3x the thickness of the thermal stack underneath. For example, the baseplate-less module and 1mm DBC reaches that point at 3mm and the module with 3mm baseplate + 1mm DBC reaches that point at 12mm (Figure 3.2.11). With a good heatsink (e.g. liquid cooling), this point is reached earlier, with a bad heatsink later.

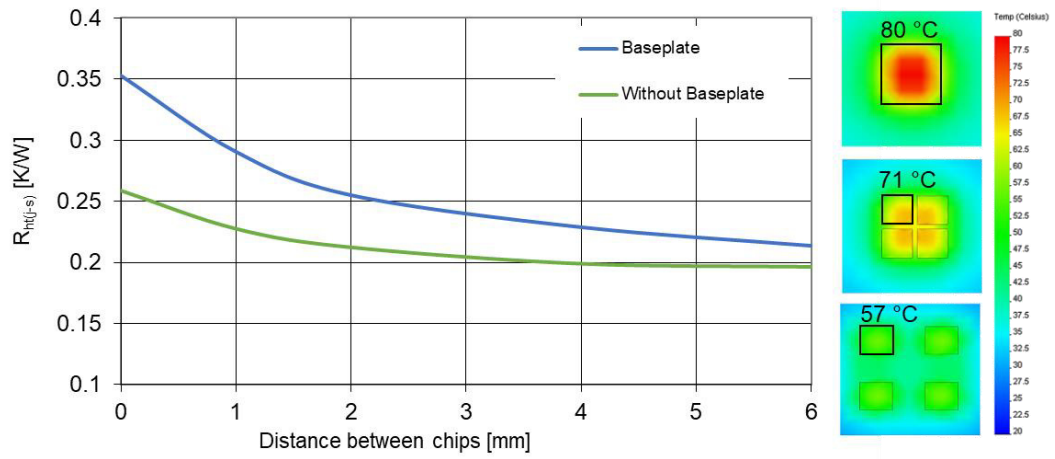


Figure 3.2.11 Thermal resistance $R_{th(j-s)}$ of 4x 36mm² chips as a function of distance in between; (TIM: with baseplate 100µm, without 25µm), right: simulation of chip temperatures with same losses but increasing distance (0mm, 1mm, 6mm)

3.2.3.4 Thermal coupling

If the heat cannot spread undisturbed in all direction because other components use the space for their heat flow, the components are thermally coupled. The coupling can take place between parallel chips of one switch (included in the R_{th}) or between different switches (not included in $R_{th(j-c)}$ but in $R_{th(c-s)}$ for the module). In general, a low thermal coupling is a design goal, but this requires space, increases cost per amp and parasitics like commutation inductances. R_{th}-measurements are carried out with DC current, that means either IGBT or diodes are loaded. In that case, each of the switches can utilize the entire space to dissipate the heat to the heatsink.

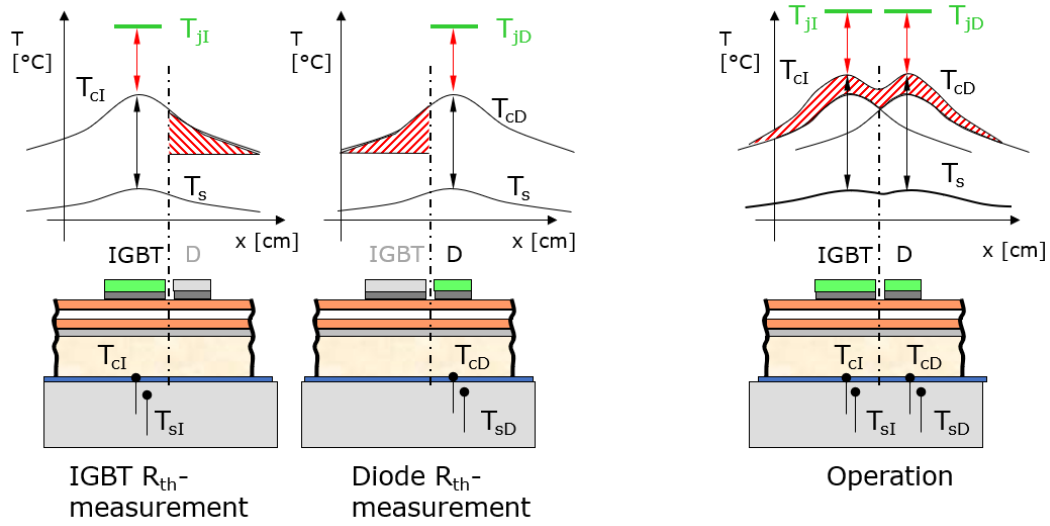


Figure 3.2.12 Influence of thermal coupling on $R_{th(c-s)}$ in example of baseplate modules

There is a thermal symmetry line between the switches. During inverter operation with losses in both switches, the hatched area in the drawing of the R_{th}-measurement (Figure 3.2.12 left side) cannot be used for heat dissipation because it is used by the other switch (Figure 3.2.12 right side). This leads to an increase of T_j and T_c but both increase roughly by the same amount, means $dT_{(j-c)}$ and $R_{th(j-c)}$ stays almost constant. The highest effect can be seen on $R_{th(c-s)}$.

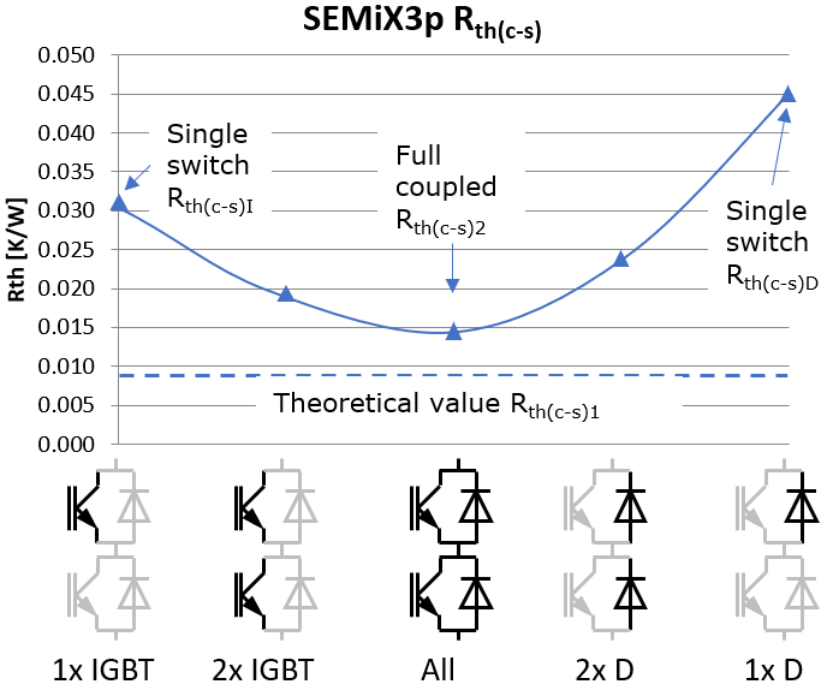


Figure 3.2.13 Influence of thermal coupling on $R_{th(c-s)}$ between the switches in an example of SEMiX 3p

The more switches are in use the more of the baseplate area is used for heat transfer. That means a single switch uses only partly the baseplate area and has therefore the highest $R_{th(c-s)}$. The case temperature rises if more switches are in use but the temperature difference is also divided by higher total losses in the module. This leads overall to a lower $R_{th(c-s)}$ for the module. In the datasheet you can find two $R_{th(c-s)}$ values. One is the so called the "theoretical" value, calculated as an parallel connection of the individual $R_{th(c-s)}$ of the switches

$$R_{th(c-s)1} = \left(\frac{2}{R_{th(c-s)I}} + \frac{2}{R_{th(c-s)D}} \right)^{-1}$$

and the second is the fully coupled $R_{th(c-s)2}$ determined using finite element simulation with equal losses/mm² in all switches.

3.2.3.5 Differences in the thermal design of modules with and without baseplate

If the two kinds of modules are compared it is not possible to use a module with baseplate to begin with and then simply removing the baseplate to perform the comparison. Of course, both design variants must be constructed under totally different aspects. Semikron Danfoss offers both technologies, because both have advantages and disadvantages.

Baseplate modules

Baseplate modules typically use few large chips in parallel with good heat spreading through the baseplate. In addition, the size of the DBC is limited due to the thermomechanical stress caused by different CTE. This means that several of the DBC are used within a module in order to realise paralleling and the circuit functionality. The baseplates are pre-bent with a convex shape to ensure the highest force and the best thermal contact in the middle of the module.

Advantages:

- Mechanically more robust during transport and assembly
- More thermal mass resulting in lower thermal impedance within the range of 1s, which can reduce temperature rise during overload if it matches the time constant (Figure 3.2.17)

Disadvantages of modules with soldered or bonded chips:

- Higher thermal resistance chip to heatsink $R_{th(j-s)}$, because of additional solder layer and thicker layer of thermal paste
- Reduced temperature cycling capability, since the large-area baseplate solder is susceptible to temperature cycles
- Higher internal terminal resistances ($r_{cc'-ee'}$), since, for thermomechanical reasons, the design is based on multiple ceramic substrates that require additional internal connectors
- Increased weight and cost

Thermal paste must be relatively thick at least 70µm to 150µm in order to prevent air between the module and heatsink surfaces. Both will never be ideally plane (Figure 3.2.16) and will not come into full contact with the heatsink across the entire surface.
An originally flat baseplate would become concave after soldering, because the two partners DBC and Copper are joined at > 200°C. During cooling down the copper would shrink more than the ceramic, because of the higher CTE. This effect is comparable to the bimetal effect. In Figure 3.2.14 are the concave areas clearly visible where the ceramics are located. The bimetal effect is overcompensated with pre-bent baseplates in a way that even after soldering the module is convex.

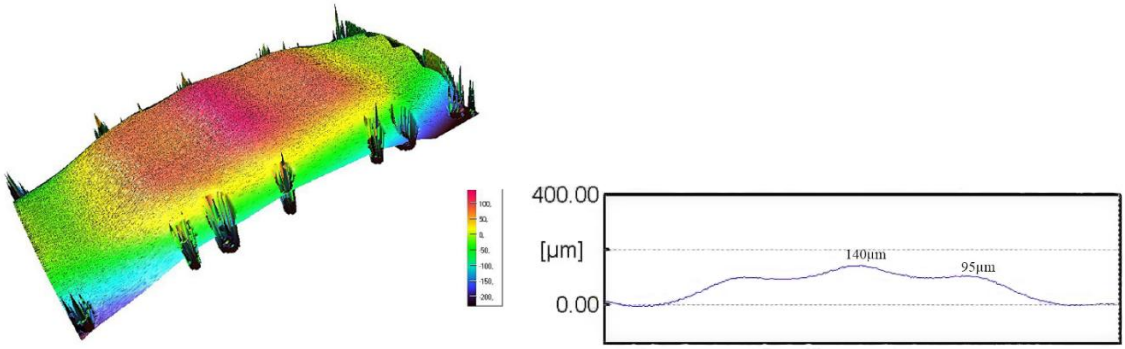


Figure 3.2.14 Surface scan of the baseplate of a "SEMITRANS 10 P2" like module and profile along the middle axis.

Furthermore, the bending varies over time due to solder creep and stress relaxation. Bending also changes as a function of the operating temperature. Even an ideally shaped baseplate would only rest flat on the heatsink at one temperature point and would lift off at a different temperature because of different expansion of heatsink and baseplate. Therefore, a thick-enough TIM layer is needed for proper thermal performance.
Modules in the upper performance range (≥ 1000A) especially for traction application use AlSiC baseplates in conjunction with AlN ceramics. This is necessary to reach high temperature cycle capability by a match of the thermal expansion coefficients of the ceramic and baseplate (a: AlN

5.7ppm, AlSiC 7ppm, Cu 17ppm → also see chapter 4.3.1). The poorer thermal conductivity of AlSiC (λ = 180W/(m·K)) compared to copper increases the thermal resistance and reduces heat spreading.

Baseplate-less modules

Baseplate-less modules use a higher number of smaller chips and achieve thermal spreading on the heatsink thanks to distributed heat sources.

Advantages:

- Lower thermal resistance, because layers are omitted and a flat contact to the heatsink allows thinner thermal paste layers
- Improved thermal cycling capability, because of removal of solder fatigue in baseplate soldering
- Smaller chips have lower temperature gradient across the chip, which means a lower hotspot temperature and less stress under power cycling conditions
- Eliminating the thermo-mechanical stress between baseplate and ceramic substrate allows usage of large ceramic substrates with low terminal resistance (Figure 3.2.15)

Disadvantages

- Lower thermal capacitance
- Processable chip size is limited, resulting in more parallel connections
- Increased requirements for thermal paste application

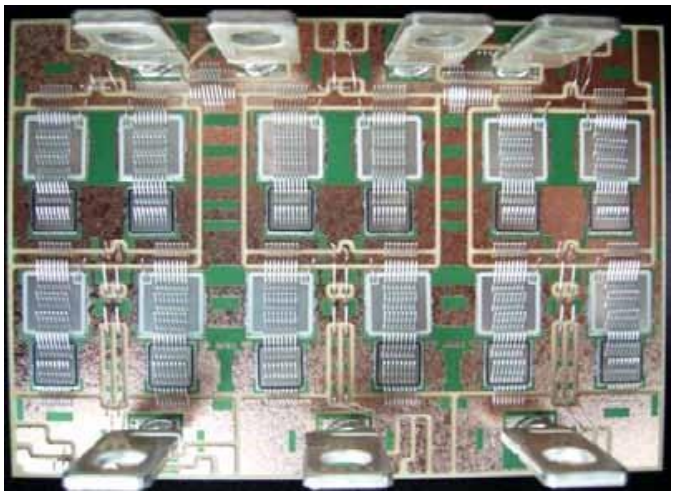


Figure 3.2.15 Large DBC substrate (115mm x 80mm), equipped with the chips of a 350A/1200V IGBT 3-phase inverter

Baseplate-less modules should be designed so that the insulating substrate is pressed against the heatsink at many different points and not just at the corners or sides to achieve an low R_{th}. The package must be designed in such a way, that the pressure is applied in the centre, along the periphery and also beside the chips. If this is guaranteed, then the thermal paste can be much thinner (about 20…30µm) compared to baseplate modules. A much thinner thermal paste layer results in a lower static thermal resistance compared to modules with baseplate.

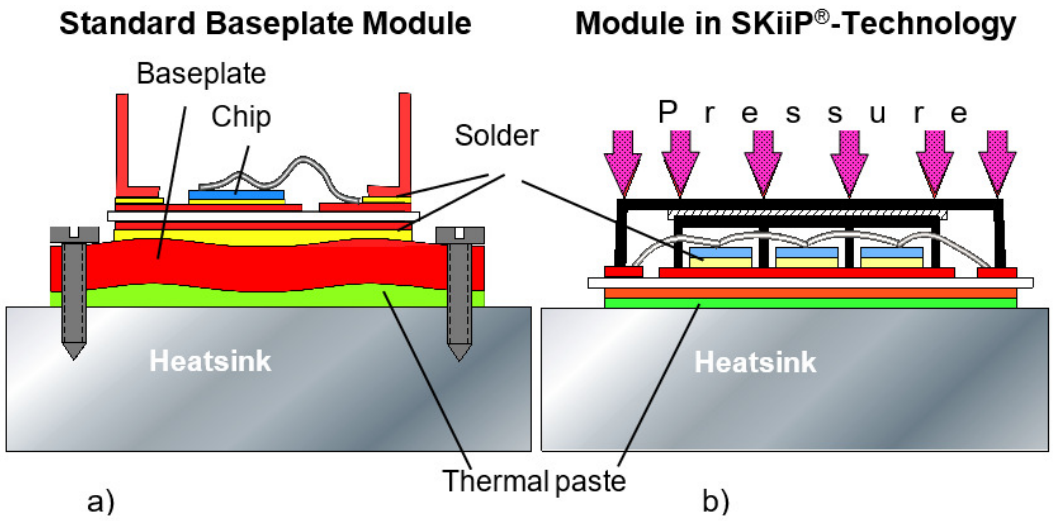


Figure 3.2.16 Baseplate bending and thermal paste requirements regarding thickness for a conventional module (a) and a module in SKiiP-technology (b)

The transient resistance however, is slightly higher in the time range between 0.1s and 1s because the thermal capacity of the baseplate is missing (see Figure 3.2.17). Thermal impedances of modules with or without a baseplate are similar in the short time scale as long as heating takes place inside the chip and the DBC substrate. For times > 100ms both curves differ over time. While the baseplate module has thermal advantages in the time range up to 1…2 s owing to the heat storage capability of the copper plate, the module without baseplate has advantages for longer periods owing to the reduced R_{th} value.

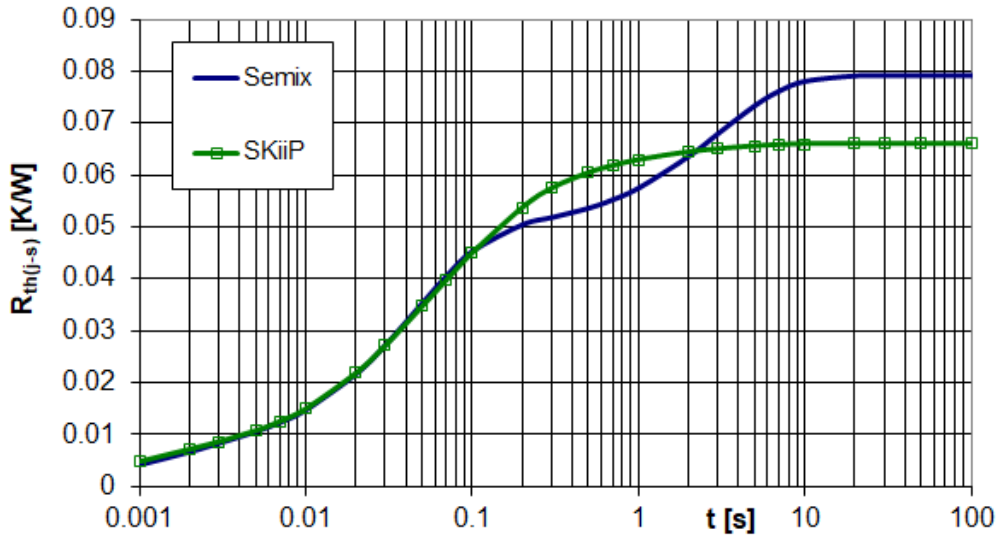


Figure 3.2.17 Comparison of thermal impedances of a 600A / 1200V module with baseplate (SEMiX4) and without baseplate (SKiiP 4); reference point: drill hole in the heatsink 2 mm below the surface

3.2.4 Main and auxiliary terminals

Most power modules available today have using screw-, spring-, Press-fit or solder-pin contacts. The usage of the modules with a PCB or a busbar is the main difference in the way, how the main terminals are connected to an external circuit.

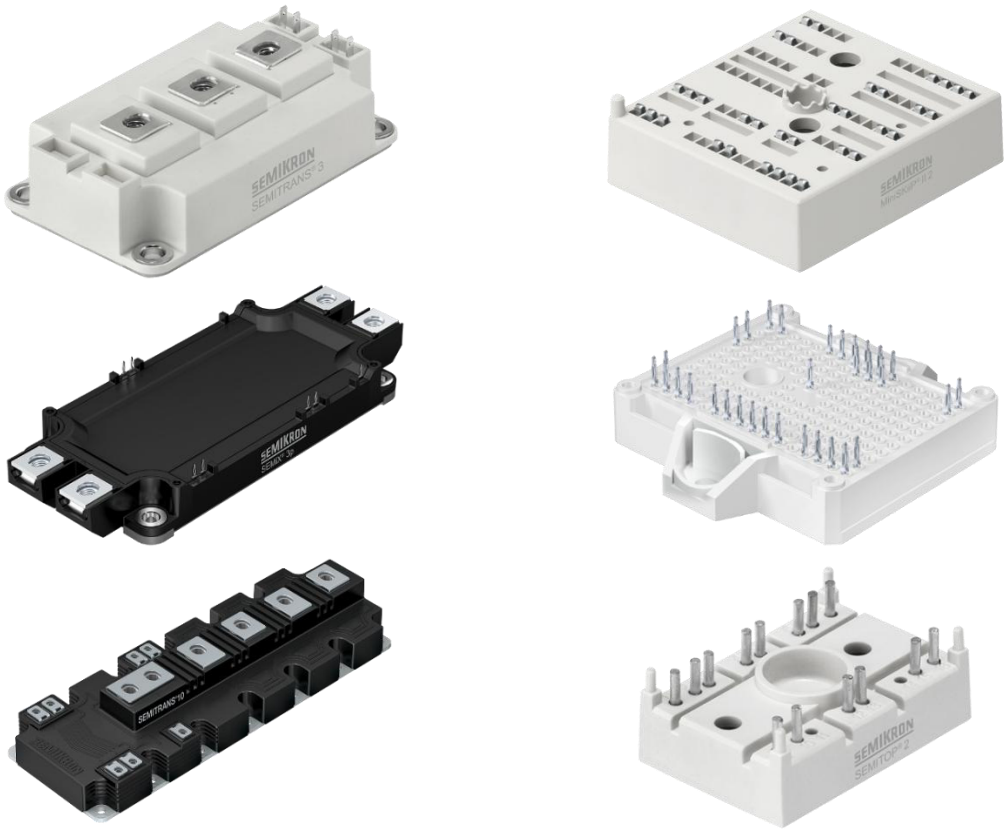
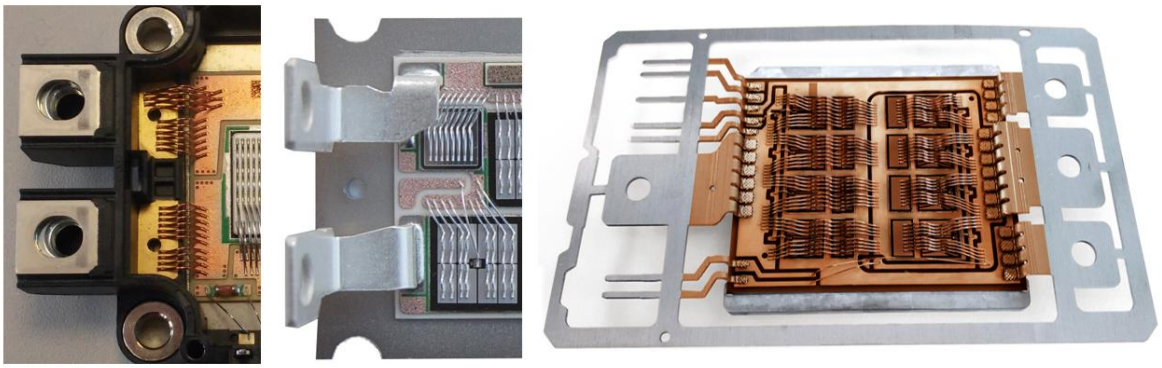


Figure 3.2.18 Examples of Modules with screw, press-fit, spring and solder-pin contact, left for higher power, right for PCB mounting and lower power

A high degree of standardisation is found in module types with screw terminals (e.g. SEMITRANS, SEMIPACK). These modules are for a current range from 200A to 1000A and more. The main terminals may be connected to busbar sandwich assemblies. The higher the current the more paralleling also from the terminals is necessary to reduce terminal resistance and stray inductance. Improved semiconductor properties (chip shrinkage) result in ever higher current ratings and power densities for the same module area. The terminals of older standard IGBT packages, in particular, are now reaching the limits of their current carrying capacity. This partially calls for current limiting due to terminal heating (specification of an $I_{t(RMS)}$ = maximum current flowing through the terminals). Losses in the terminals can be estimated with the parameter $R_{cc'-ee'}$. These occur in addition to the chip losses and are usually not negligible. A SEMITRANS 3 module with $R_{cc'-ee'}$=0.55mΩ, for instance, would produce terminal losses of approx. 90W at 400A per switch ($P_{terminal} = 400A^2 \cdot 0.55m\Omega = 88W$).



a) b) c)

Figure 3.2.19 Bonded main terminals (a), soldered terminals (b) and welded lead frame (c)

The current-carrying capacity is particularly low for terminals that are cast into the housing and are connected via bond wire, since in this case there is only a poor thermal connection to the DBC substrate (Figure 3.2.19). However, one advantage of this technology is the mechanical connection

in the housing. This makes the terminals more robust and resistant to external forces and moments (such as torque and bending moments). Nevertheless, this connection will be more and more replaced by welding.
Soldered terminal or solder pins are in direct contact to the DBC substrate, thus displaying better heat dissipation. The disadvantage of these solder connections is the more complex production process ("preform soldering" or second soldering with particular chip requirements as regards soldering capability). Users will notice a higher susceptibility to mechanical and thermomechanical stress. Often, they need a special stress relief (meanders, bending). Examples of this are the standard modules in 63mm and 34mm packaging (SEMITRANS, SEMIPACK) or the SEMiX 3s family (Figure 3.2.19 b).
Lead frames are pre-cut metal parts known mainly from ICs or discrete power semiconductors. They are often soldered or like in Figure 3.2.19 c) welded to the chip or DBC. The outer frame is cut-off after the assembly process is finished to separate the individual terminals. Advantages are the mechanical robustness, good thermal contact and some cost savings.
Pressed massive copper terminals provide excellent thermal and electrical contact thanks to numerous pressure spots. They are wear-free with regard to thermo-mechanical stress. The disadvantage of this is that the external mechanical forces have to be absorbed by the package. This means that a more complex design is needed, as is the case in SKiiP or SKiM63/93 (see Figure 3.2.21).
Additional terminals are often provided in high power modules for control and sense-units (e.g. auxiliary-emitter (Kelvin-), sense-collector) in order to minimise the influence of inductive voltage drop in the main circuit generated during switching. Auxiliary terminals can be realized with fast-on terminals, press-fit pins, springs or even as screw terminals for the real high-power modules.
Components for direct PCB assembly are used in the current range to about 200A, because they offer cost advantages in production and automatic assembly. The current limit is increasing over the years by usage of power PCB'S and multiple paralleling of small terminals. Optimised layout of connectors enables low-inductance assemblies. Solder pins (e.g. SEMITOP), press-fit contacts (e.g. SEMITOP E, SEMiX 6) or spring contacts (e.g. MiniSKiiP) are used as connectors.
In spring contacts, the high specific resistance of the spring material limits the amperage; higher amperages require parallel spring connections (e.g. MiniSKiiP with ca. 20A per spring). The contact force of 20…100N/mm² of a spring contact is equal or higher compared to a screw contact, because of the small tip of a spring. This ensures safe and reliable contact even under shock stress of up to 100G. Spring contacts have a number of advantages over solder and press-fit contacts with respect to PCB assembly:

- easier PCB routing, since "vias" are not required
- High degree of automation in the inverter assembly process possible, since no large-surface components with tolerances have to be fitted into holes
- Assembly of the (heavy and expensive) power semiconductor and heatsink after soldering and PCB pre-testing
- Improved thermal cycling capability thanks to "free-moving" contacts
- Higher resistance to shock and vibration stress (no solder fatigue)
- Quasi-hermetically sealed contact is corrosion-proof - No electromigration

The advantages of solder and press-fit contacts are

- double- or three-times higher ampacity per contact (lower terminal resistance)
- no special treatment of the contact area on the PCB (e.g. gold flash) necessary
- lower inductance especially compared to spiral springs in the control circuit (gate inductance)

3.2.5 Low-inductive internal structure

With the example of a halfbridge module, Figure 3.2.20 shows the key internal parasitic inductances in a module resulting from the necessary connections between chips and to the module terminals (bond wires to the chips, DBC tracks and terminals).

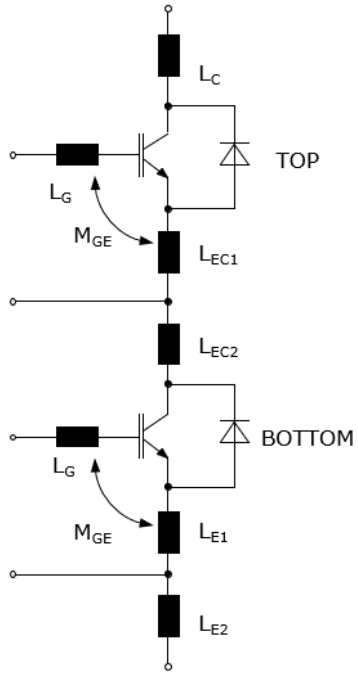


Figure 3.2.20 Parasitic inductances in a dual IGBT module

$$L_{CE} = L_C + L_{EC1} + L_{EC2} + L_{E1} + L_{E2}$$

L_G: parasitic gate inductances
L_C: parasitic TOP-collector inductance
L_{EC}: parasitic connection inductance between TOP-emitter and BOTTOM-collector
L_E: parasitic BOTTOM-emitter inductance
M_{GE}: Mutual Gate inductance between main current path and gate circuit
L_{CE}: total parasitic inductance between TOP-collector and BOTTOM-emitter

These inductances, which cause overvoltage during turn-off and a slowdown of di/dt during turn-on, as well as inductive coupling of control and power circuit, will directly affect the performance of power modules. Furthermore, parasitic inductances in modules with internally paralleled chips may result in uneven current distribution during switching and may be oscillations between the chips. Chapter 9.2 will discuss the impact on the electrical behaviour in more detail.
The goal of the development is often minimizing of the stray inductance, but depending on chip technology it can be advantageous to have some negative inductive feedback to reduce short circuit currents or with other chip characteristics to have some positive inductive feedback to accelerate di/dt and reduce switching losses if large gate resistors have the be used to limit dv/dt. In any case, detailed simulations must be carried out in order to find the optimal solution. However, one goal is always present, namely the even distribution of current under switching conditions. That means the mutual gate inductance should be equal for parallel chips.

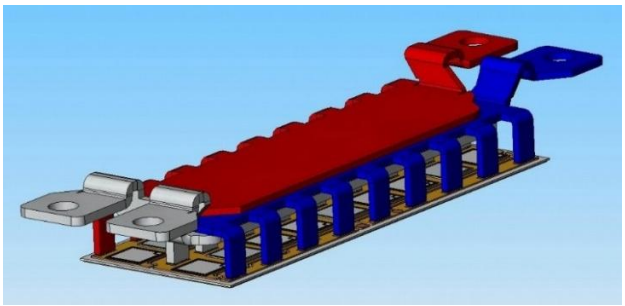


Figure 3.2.21 Internal busbar system of a SKiM 93 (red: +DC, blue: –DC, grey: AC)

Possible design measures to reduce internal inductance are parallel current paths. An example of such a design is shown in Figure 3.2.21 for SKiM 93, similar are used for SKiiP 4. The internal busbar system ensures magnetic coupling of the main current path of +DC (L_C) and -DC (L_{E2}). During current commutation between +DC and -DC, the magnetic field needn't change much,

which is equivalent to a low inductance. The many parallel current paths leading to the individual chips reduce the inductances of the connection parts, which cannot be designed in "sandwich" constructions. Figure 3.2.22 shows a switching operation with voltages at different chip positions and the DC terminals. The voltage difference between chip position and main terminals is 140V. An inductance from +DC to –DC of about 20nH can be calculated for the measured rate of current rise. It can also be seen that there are hardly any voltage differences between the individual chip positions, which indicates an extremely low inductance in the vicinity of the sandwich busbar system. The main part of the 20nH is caused by the external screw points. Here, overlapping current routes must be abandoned in order to ensure clearances in air and creepage distances at the outer terminals.

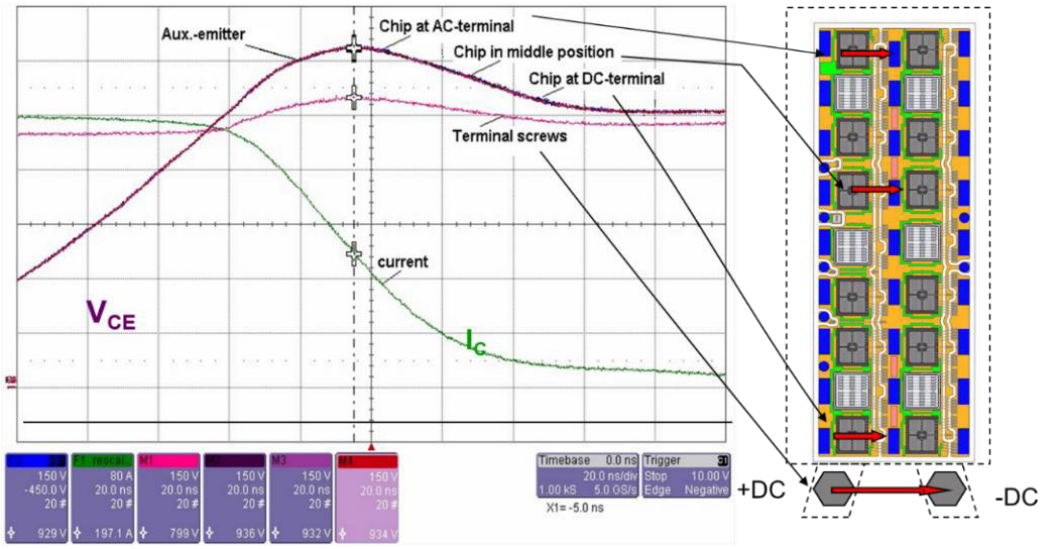


Figure 3.2.22 Overvoltage measurement in the SKiM 93 during turn-off at different chip positions and at the outer terminals at 7kA/µs

For applications, the internal turn-off overvoltage is lost with respect to the maximum voltage to be utilised or with other words: The overvoltage at short circuit or overcurrent turn-off limits the maximum DC link voltage. Users must ensure that the turn-off voltages measured at the outer terminals plus the voltage drop over the internal inductances is always lower than the blocking voltage of the semiconductors. The auxiliary emitter terminal may be used to measure voltages for the "BOTTOM" switch. This terminal is closer to the chip and therefore provides a better picture of the turn-off overvoltage than the main emitter terminal (also [3.10]).

3.2.6 Coupling capacitances

The fast rates of rise of current and voltage within the ns-range that can be achieved in MOSFET and IGBT modules generate electromagnetic interference with frequencies well into the MHz range. For this reason, the parasitic elements that are typical in the internal and external propagation paths in the module exert considerable influence on the radio interference voltages generated. Suitable insulation materials, small coupling areas or conductive shields can reduce, for example, asymmetrical interference [3.11], [3.10]. In addition to this, the internal connections in the module have to be structured such that malfunctions caused by outer stray fields or transformatory coupling into control lines are ruled out.
Another aspect is the "earth current", i.e. the current

$$I_E = C_E \cdot \frac{dV_{CE}}{dt}$$

flowing over the normally earthed heatsink over the coupling capacitance C_E of the insulating substrate as a result of the dv/dt during switching. Module capacitances can be calculated using the equation for plate capacitors:

$$C_E = \frac{A \cdot \varepsilon}{d}$$

d (thickness) Al_2O_3: 0.38mm or AlN: 0.63 mm;
$e = e_0 \cdot e_r$ =9.1·8.85e-12 F/m (Al_2O_3 and AlN);

The following shares of substrate area can be estimated for a halfbridge module:

- 40% "+DC"
- 40% "AC" and
- 15% "-DC"

The potential against earth and its amplitude when switched depend on the earthing concept for the connected load. Suitable measures (e.g. Y-capacitors) must be taken to create a current path in the converter that closes a circuit close to the semiconductor; this must be done to ensure that current i_E does not flow through the controller and monitoring units. This earth current would be identified as a fault by a residual current protective device and may trigger this device. For installations where high leakage currents occur for functional reasons, special labelling requirements and mandatory minimum cross sections for the protective conductors exist (EN 50178, EN 61800-5-1).

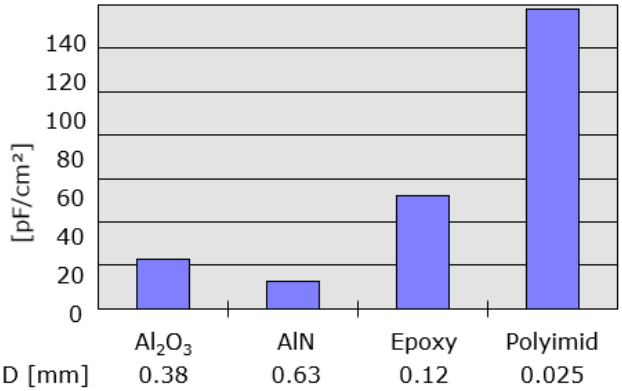


Figure 3.2.23 Capacitance per cm² for different insulating substrates

Figure 3.2.23 compares the capacitances of the most common substrate materials in their standard thicknesses. The deviating dielectric constants and the standard thicknesses depending on mechanical strength and isolation capability (thickest substrate material being AlN with 630µm, thinnest substrate required in IMS structures, with 120µm for epoxy insulation and 25µm for polyimide insulation) result in different capacitances C_E and thus different limits for the maximum switching speed dv_{CE}/dt for a maximum permissible earth current i_E.

3.2.7 Failure behaviour in the event of module defects

In the event of module malfunction (e.g. caused by humidity, cosmic ray, chip defect, wrong controller signal or end of life wear out …), the total energy stored in the circuit e.g. of the DC link capacitors in a voltage-source inverter will be discharged in the module. Chips will burn, bond wires melt, soft-gel vaporises, that means a large part of this energy will generate plasma, which may lead to module cracks or explosion. It cannot be foreseen if the result is an open circuit or a short circuit. Heavy destruction can be expected if energy is fed ongoing in existing short circuit from the mains or a battery. The ongoing burning of an electrical arc can melt the isolation and even the heatsink. Fuses or circuit brakes are necessary to prevent such consequences.
The resultant high kinetic energy of the explosion could distribute plasma and particles of the module case across the module surroundings. Module case designs try to limit the dangers involved where possible and ensure safe module rupture (e.g. by defined particle distribution) but can never exclude this. There are developments in this field that ensure, for example, that up to a defined energy level of 15kJ, no particles will leave the module; even at 20kJ the case might break, but no solid metal particles would be hurled into the surroundings [3.12][3.12]. IEC 60747-15 provides no definitions for a case rupture current or case rupture energy for power semiconductor modules.

3.2.8 Integration of sensors

3.2.8.1 Temperature measurement

More or less all power modules developed in the last 25years have integrated temperature sensors. Some use PTC (Positive Temperature Coefficient) and other NTC temperature sensors (Negative Temperature Coefficient) in SMD designs or as chip sensors.

PTC

The PTC sensor of type SKCS2Typ100 is used in MiniSKiiP, in some SEMITRANS and SEMITOP modules, as well as in SKiM 4/5 and SKiiP 3. At 25°C, the sensor has a resistance of 1000Ω and a typical temperature coefficient of 0.76%/K.

$$R(T) = 1000\Omega \cdot [1 + A \cdot (T - 25°C) + B \cdot (T - 25°C)^2]$$

$A = 7.635 \cdot 10^{-3}$ °C^{-1} and $B = 1.731 \cdot 10^{-5}$ °C^{-2}

The measurement tolerance of the sensor in the measured current range 1mA … 3mA is max. ± 3% at 25°C, max. ± 2% at 100°C.

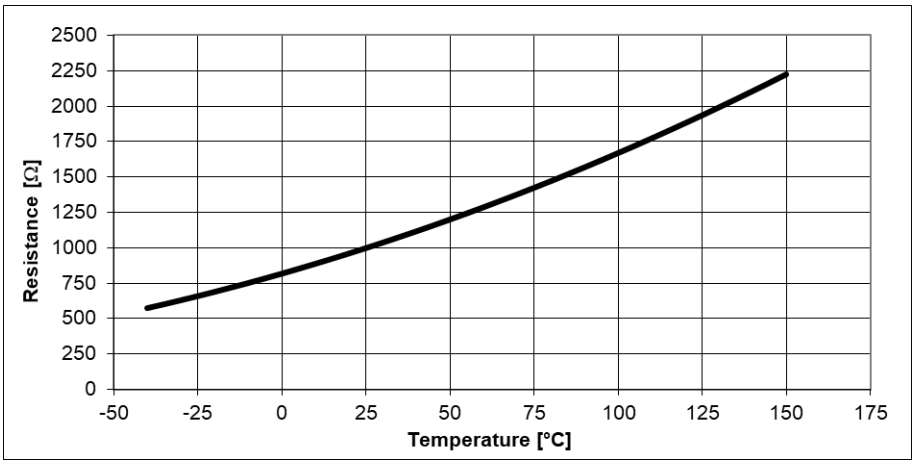


Figure 3.2.24 Characteristic curve of the PTC temperature sensor, type SKCS2Typ100

One advantage of a chip sensor is that it can be processed together with the power semiconductors in the same production line. An advantage of the PTC characteristic is that an open circuit would be detected as a failure "high temperature". For a NTC an open circuit would be read out as cold temperature.

NTC

An NTC sensor, e.g. of type KG3B-35-5, is used in SEMiX components, some SEMITOP as well as in SKiM 63/93 and SKiiP 4. The individual product groups use sensors with different characteristics. For details on the characteristic parameters, see the datasheets. For example, the sensor in SEMiX IGBT modules has a resistance of 5kΩ at 25°C and a resistance of 493Ω at 100 °C. The measurement tolerance of the sensor in the measured current range 1mA … 3mA is max. ± 5% at 100°C. Owing to its exponential characteristic, the sensor is more suitable for protection than for exact temperature measurement. To reduce the dissipation in the sensor at low temperatures a parallel resistor of for example 2kΩ is recommended. Otherwise, the sensor would heat itself up by 5W at room temperature and 1mA measuring current. The following formula is a simplification of a multidimensional polynomial. Several "B-factors" for different temperature ranges can reduce the failure of the simplification.

$$R(T) = R_1 \cdot e^{B_{(T1/T2)} \cdot \left(\frac{1}{T} - \frac{1}{T_1}\right)}$$

R_1 at T_1=25°C: 5kΩ; at T_1=100°C: 0.493kΩ (± 5%);
$B_{(25/50)}$ = 3375K
$B_{(25/85)}$ = 3420K
$B_{(100/125)}$ = 3550K (± 2%)
$T_1 = T_{ref}$ + 273.15 K [T - in Kelvin]

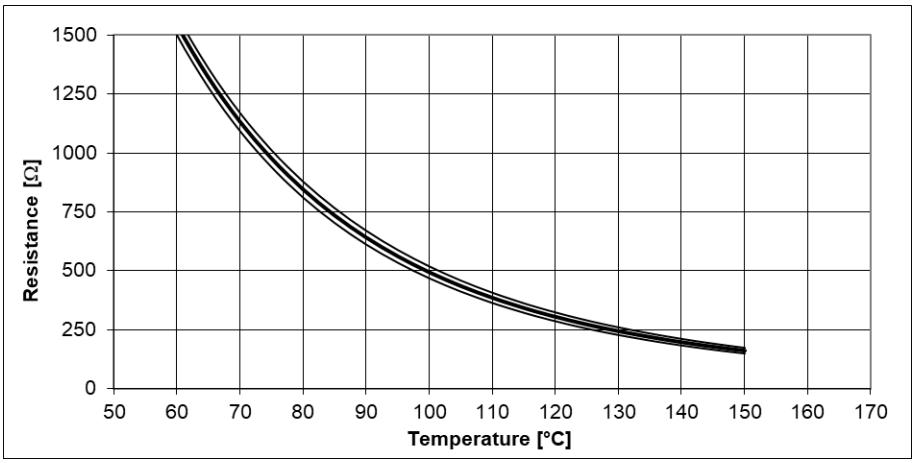


Figure 3.2.25 NTC sensor characteristic in its relevant temperature range incl. tolerance

The sensors are soldered to an electrical insulated track on the DBC substrate close to the chips but still with a few mm distance. Since the lateral heat flow is no better than the vertical one, the sensor temperature roughly corresponds to the heatsink temperature below the chip. In quasi static conditions is the temperature difference from sensor to chip a constant value. A suitable evaluation circuit provides static overtemperature protection by active driver control or by analogue signal processing. However, there are considerable dynamic time delays, represented for example in the long-time constants of thermal impedance $Z_{th(j-r)}$ in the SKiiP 3 (shares of t > 200 s for aircooled systems, > 50 s for watercooled systems). For this reason, an insulated temperature sensor cannot provide protection from short-time overload.
High-quality protection in terms of dynamics is possible with IPM solutions (see SKiiP 4 in the following chapter). The protective function can be carried out at the secondary side of the driver and thus at high potential. The sensor can therefore be placed on the same copper pad as the power semiconductors, directly beside the heat source. Measurements are much closer to the chip temperature, although not yet equal. The biggest advantage, however, is that the greatest time constant of $Z_{th(j-r)}$ is now in the range of 1s, thus enabling much better protection from short-time overload. Digital signal transmission in the SKiiP 4 nevertheless provides an analogue temperature sensor signal at the driver interface, which meets the requirements of reinforced insulation.

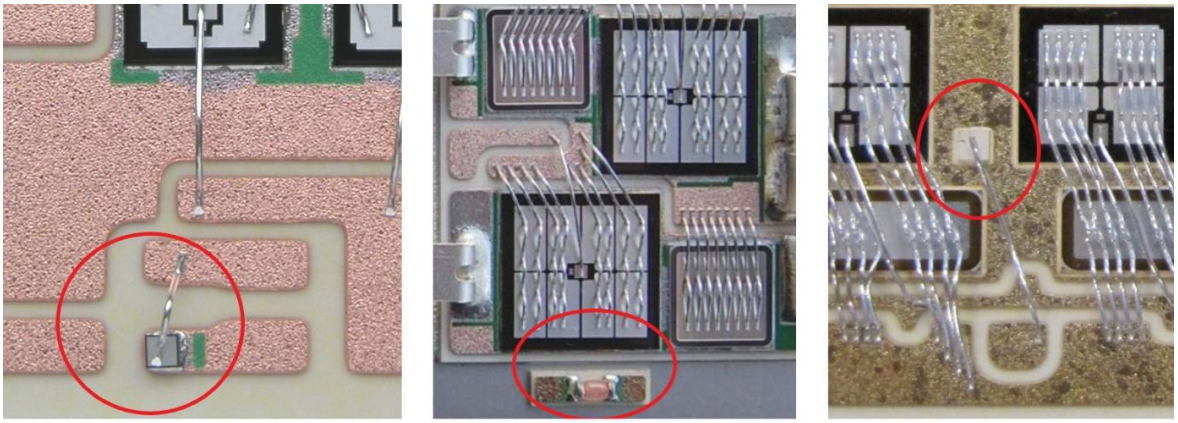


Figure 3.2.26 Temperature sensors in power semiconductor modules: a) Insulated PTC chip in a MiniSKiiP; b) Insulated NTC in SEMiX; c) non-insulated chip sensor on collector potential in SKiiP 4

With the exception of the SKiiP 4 described above, all temperature sensors have a basic insulation, but do not meet the requirements for reinforced insulation. The insulation clearances are between 0.7 mm and 1.6 mm; the required insulation voltage is achieved by filling the modules with silicone gel. Insulation clearances are so small (Figure 3.2.26 a)) that in the event of a fault, plasma - and thus high electrical potential - might be present at the sensor. For this reason, the insulation of the temperature sensor is regarded basic insulation only, as per EN 50178. Additional circuits are necessary to obtain the safety grade "Safe Electrical Insulation" described in this standard.



Figure 3.2.27 Possible voltage flashover to the insulated temperature sensor if a bond wire melts as a result of a fault

Temperature sense IGBT

To measure the temperature of an IGBT several temperature sensitive electrical parameters can be used [3.13], most common is the forward voltage at a low current also known as $V_{ce0}(T)$-method. More suitable for usage in inverter operation is an integration of one or several pn-junctions in series in an electrical insulated area of the IGBT chip [3.14]. The insulation is only functional insulation. The measurement principle is the same as for the $V_{ce0}(T)$-method – there is an almost linear dependency of voltage and temperature with NTC characteristic. The difference is that here a from main current separated current path can be used. The disadvantage is that some space of the chip gets lost and that you might have a small difference to T_{vj} or to the hotspot, because the temperature is measured somewhere on a cooler chip corner. Because of the additional terminals and routings, it is a solution for single chip switches in IPM or in discrete housings and is not available in Semikron Danfoss modules.

3.2.8.2 Current measurement

Firstly, current measurements in modules are taken to protect the power semiconductors from overcurrent, and secondly, the current signal is also required for current control loops. Rough monitoring is sufficient for the first task, which is why the semiconductor itself can be utilised as a current sensor ($V_{CE(sat)}$ monitoring). The latter must be very accurate (1%…5% tolerance), very dynamic (response times ~ 1 µs) and requires a frequency range from DC to some 10 kHz.

Current shunts

Current shunts for taking direct measurements are integrated into the emitter path (-DC) of IGBT modules or placed at the AC output. The three-square components in Figure 3.2.28 left show a solution for current measurement in the emitter path of three low-side IGBT in a 3-phase inverter module. Evaluation must be performed using a differential amplifier in the driver electronics stage. The connecting pads at the sides ensure low-inductance coupling with the main current path.

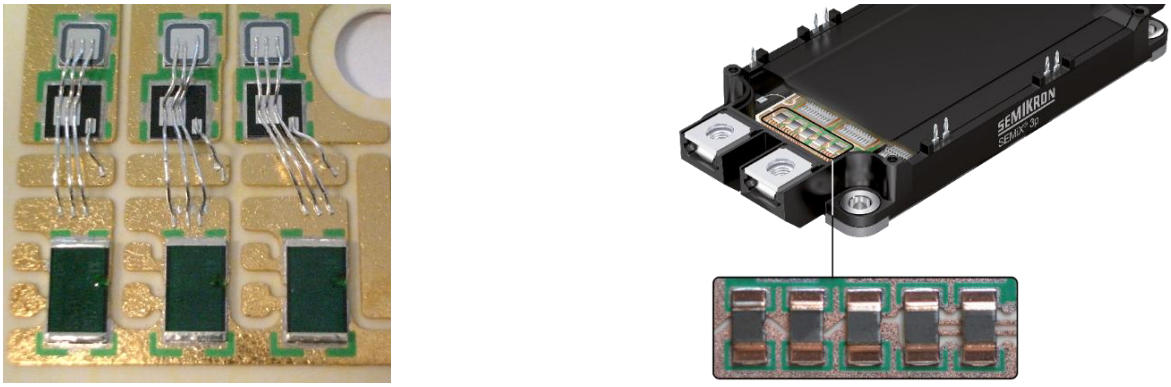


Figure 3.2.28 Current shunts in the emitter path of Low Side IGBT and at the AC terminal of a SEMiX 3p

The problem with the use of shunts is the discrepancy between the low measurable voltage range in a disturbed environment and the losses in the shunt. A 5mΩ shunt has a voltage drop of just 100mV at 20A, but 2W losses. With such a power loss, the limits for PCB assembly have been reached. Shunts that are placed on a DBC provide the advantage that the heat can be directly dissipated through to the heatsink. This extends the usable current range on the PCB from approx. 20 A to approx. 50A per shunt. The disadvantage here is that "precious" DBC space is lost.

Measuring the AC current in a SEMiX3p module like shown on the right side of Figure 3.2.28 requires several shunts in parallel to achieve a certain current carry capability. Nevertheless, is the RMS current reduced compared to a same rated IGBT module without shunts to about 200A…250A. A low tolerance of 1% allow to use the measurement signal for motor control.

Current sensors

For currents above 50A, electrically insulated transmitters operating according to various principles are often used (transformer, Hall effect, magneto-resistive effect). SKiiP uses compensating transducers (Figure 3.2.29), which are characterised by high precision, a wide frequency range and a high overload capability. Sensor evaluation is part of the IPM electronics and the protection concept. In the principle presented here, the magnetic field of the main current is measured in an air gap of the transmitter core and, with the aid of an amplifier, a current is fed in an auxiliary winding which compensates the magnetic field to zero. The compensation current is a direct mirror of the main current. It is possible to measure DC current and detect the direction of current flow.

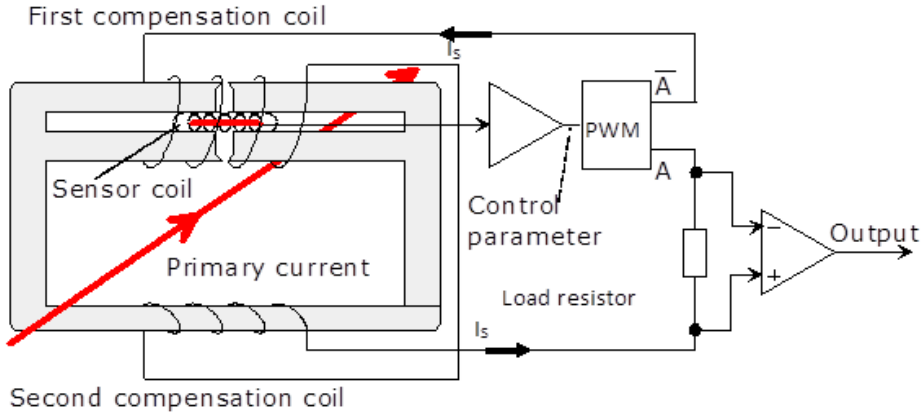


Figure 3.2.29 Operating principle of the compensation current sensor in SKiiP IGBT modules

Current sense IGBT

With these special IGBT chips with a small number of separately connected cells, a measuring current is derived that is proportional to the main current in a fixed ratio (e.g. 1:1000). On the surface is an additional bond pad required. The method is mostly used in single chip applications or discrete housings and is not available in Semikron Danfoss modules. Compared to solutions with shunts in the emitter circuit, a much higher measuring resistance may be selected here (0.5…1Ω). It can be an external shunt or integrated in an IPM. In contrast to overcurrent protection provided by V_{CE} monitoring, non or at least much shorter dead-times are required. A disadvantage here is a lower precision as well as a temperature dependency of the measurement method, meaning that it can only be used for protection purposes.

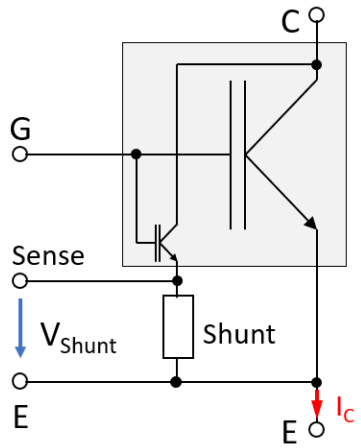


Figure 3.2.30 Sense IGBT

3.2.9 Sustainability, environmentally compatible recycling

Today's power modules refrain from using toxic materials (e.g. BeO) and the number of materials used is kept as low as possible. Cases and other materials are flame-resistant and must not release toxic gas during burn-out (UL approval). In the recycling process, the module has to be dismantled and separated into metal and non-metal components. This must be easily achievable. For this reason, newer modules are cast solely using elastomeric materials (soft moulding). All semiconductor modules produced by Semikron Danfoss are conform to RoHS respective the Directive 2022/65/EU (RoHS2) and delegated Directive 2015/863/EU.

3.3 SKiiP® high power IPM

3.3.1 Basic functionality

In addition to IGBT and freewheeling diodes, IPM modules are able to integrate more components for drivers and protective units (IPM minimal configuration) as well as complete inverter control units. Advantages are their high degree of integration and a higher degree of reliability in comparison to relevant discrete structures thanks to ASIC solutions. A disadvantage for the user consists in the fact that he will normally not be able to influence the switching features and logic functions. Therefore, IPM are often designed specifically for the individual application (ASIPM = Application Specific IPM).
The Semikron Danfoss SKiiP modules (**S**EMI**K**RON **i**ntegrated **i**ntelligent **P**ower) are equipped with a power section in pressure contact technology, as described in chapter 3.1.5. The modules contain a gate driver unit that integrates protective and monitoring functions. This driver is a SMD-PCB that is located directly above the power modules. Driving and power supply can be performed on potential of the superordinate control system.
The SKiiP driver unit integrates the necessary potential separation, a switched-mode power supply and the driver output stages. SKiiP feature current sensors in the AC outputs and temperature sensors, as well as DC link monitoring for selected types. The driver acquires the signals transmitted by the sensors for the purpose of overcurrent, short circuit, overtemperature and overvoltage protection, as well as faults resulting from supply-undervoltage. An ERROR or HALT status signal and standardised analogue voltage signals for the actual AC output current value, the actual sensor temperature and the DC link voltage are available on separate potentials at the driver connector for evaluation in the superordinate control circuit. Overcurrent protection is ensured by the current sensors as well as bridge-shorting protection by way of V_{CE} monitoring. The logic for the control signals provides short-pulse suppression and interlocking of the control signals for each switch.

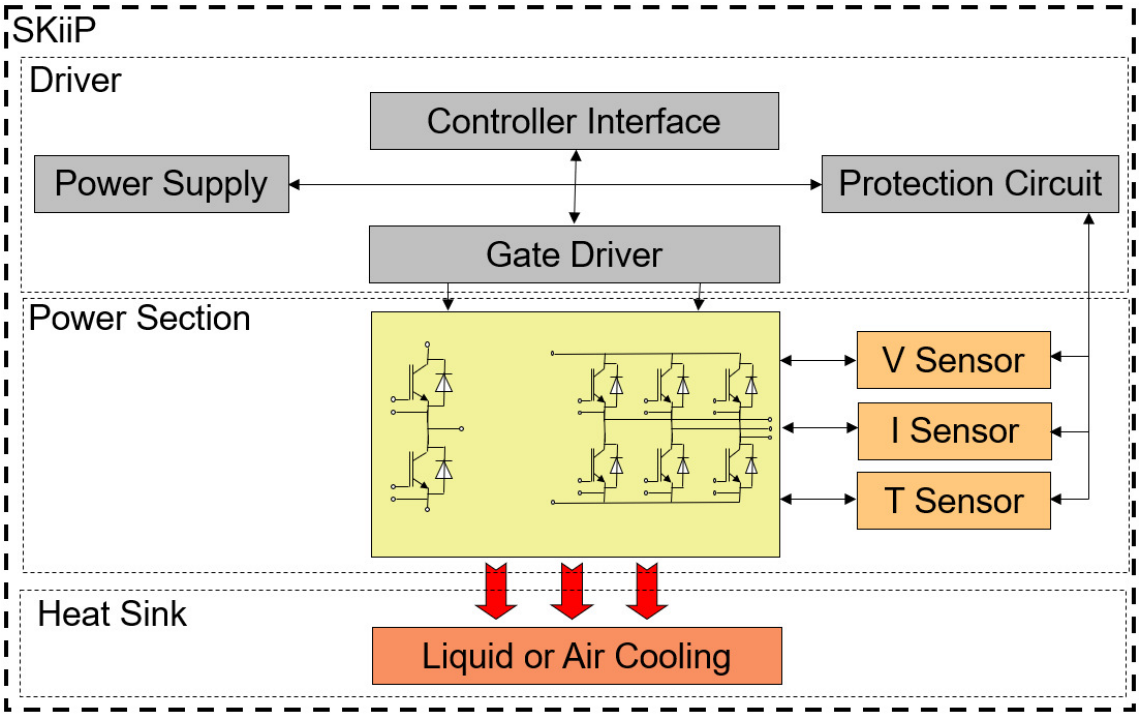


Figure 3.3.1 Principal layout of a SKiiP IPM

SKiiP IPM include a cooling system. The IGBT module and driver are joined in one unit which is mounted onto a heatsink for forced air or water cooling. This complexity enables the SKiiP to be extensively tested as a whole at the end of the production process under load and at high temperatures. Thus, with a SKiiP IPM, the customer gets a completely assembled and 100% functional, load- and burn-in tested power unit. The principal SKiiP IPM layout is shown in Figure 3.3.1.
SKiiP IPM modules contain 2 to 6 identical halfbridges mounted in a line on a heatsink with IGBT and CAL diodes for either 1200V or 1700V blocking voltage. Currently under development are 2000V SKiiP IPM equipped with SiC MOSFET. The halfbridge construction enables the SKiiP to be manufactured alternatively as halfbridge (GB) or – in the 3-fold configuration – as sixpack (GD) modules. Presently Semikron Danfoss produces three different SKiiP IPM series with properties tailored to specific power ranges: SKiiP 3, SKiiP 4 and SKiiP 7. The latest SKiiP 7 IPM generation represents an enhancement of SKiiP 3 with the latest chip and driver technology using a simplified design with less components, combined with high power cycling capability and environmental robustness.
The Table 3.3.1 below gives an overview of the characteristics, differences and similarities of the three current SKiiP series, equipped with IGBT.

	SKiiP® 3	SKiiP® 7	SKiiP® 4
			
Intended area of use	Medium power	Medium to high power	High power
Present power range	100kW to 800kW	150kW to 2400kW	600kW to 2400kW
V_{CES} Voltage classes	1200V & 1700V		
Chip Technology IGBT	Infineon Trench 3	Mitsubishi Gen. 7, Infineon IGBT 7	Infineon Trench 4
Chip Technology freewhel	CAL HD, CAL3, Pt Diode	CAL4F	
Max. chip temperat. T_{jmax}	150°C	175°C	
Max. operational chip temperature $T_{j(op)max}$	125°C	150°C (175°C in limited ovl. cases)	150°C
Individual IGBT/diode/ driver settings	not available	available	
DBC material / DCB-chip connection	Al_2O_3 or AlN / solder technology	Al_2O_3 / sinter technology	
Bond wire material	Al	1200V: AlCu, 1700V: Al	Al
Thermal Interface material	Wacker P12	High Performance Thermal Paste (HPTP)	Wacker P12 or HPTP (optional)
Standard heatsinks (forced air cooling)	SKiiP3/SKiiP7 heatsink profile		SKiiP4 heatsink prof.
Standard heatsinks (water cooling)	NWK40 profile	NWK40 profile, HPC High Performance water Cooler	NHC pofile, HPC High Performance water Cooler
Gate driver principle	lse controlled gate driv	digital gate driver with state-of-the-art driver ASIC chip set	digital gate driver
controller-side Interface	DIN41651 interface	DIN41651 interface or 25 pin D-Sub interface	25 pin D-Sub interface
Controller side supply voltage V_S	13V…30V		19.2V...28.8V
Input threshold voltage HIGH/LOW	12.3V / 4.6V		$0.7 \cdot V_S$ / $0.3 \cdot V_S$
Signal transmission	pulse transmission via transformer	Digital signal transmission via transformer	
AC current measurement	potential separated via high accuracy current sensors		
DBC Temperature sensing	Sensor isolated on DBC	Sensor isolated on DBC, digital transmission via galvanic isolation (pulse transformer)	
DC Link voltage sensing (opt. for halfbridge SKiiP)	High-impedance differential amplifier	Digital transmission via galvanic isolation (pulse transformer)	
Overcurrent/short circuit protection	Load overcurrent measurement & protection (OCP)		OCP, at 1700V SKiiP: IntelliOff protect)
	Load and internal bridge short circuit (DSCP)		
Overtemperature protection	DBC-sensor overtemperature	DBC-sensor and driver overtemperature	
Overvoltage protection	DC-Link overvoltage (option DC voltage sensing)		DC-Link overvoltage
Undervoltage protection	Primary side supply undervoltage		
	Secondary side supply undervoltage		

Table 3.3.1 Key features of the present IGBT IPM product series SKiiP 3, SKiiP 4 and SKiiP 7

Figure 3.3.2 shows the basic structure of the SKiiP IPM using the example of an SKiiP 4 on a water cooler and the "N times · fold" construction principle.

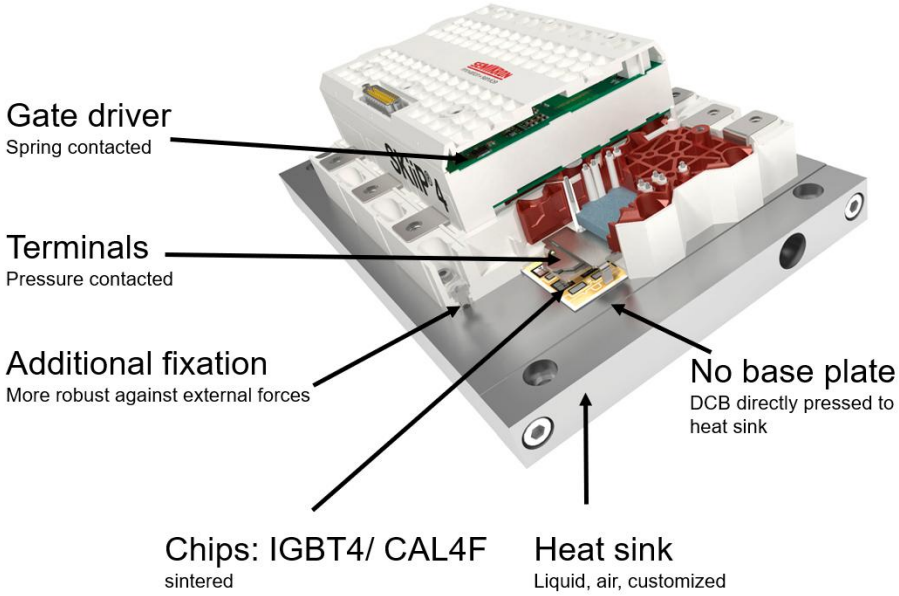


Figure 3.3.2 Basic structure of a SKiiP 4 IPM

Although the halfbridges are controlled by a common gate driver PCB, each halfbridge is equipped with separate power terminals (Main terminals AC/DC) for the customer's connections to the power circuit. The common control input is realised by a DIN 41651 or a SUB-D Driver Interface.
Table 3.3.2 and Table 3.3.3 below provide an overview of the halfbridge (n-fold) combinations for water and air cooling and the corresponding IGBT nominal current ratings (I_{Cnom}).

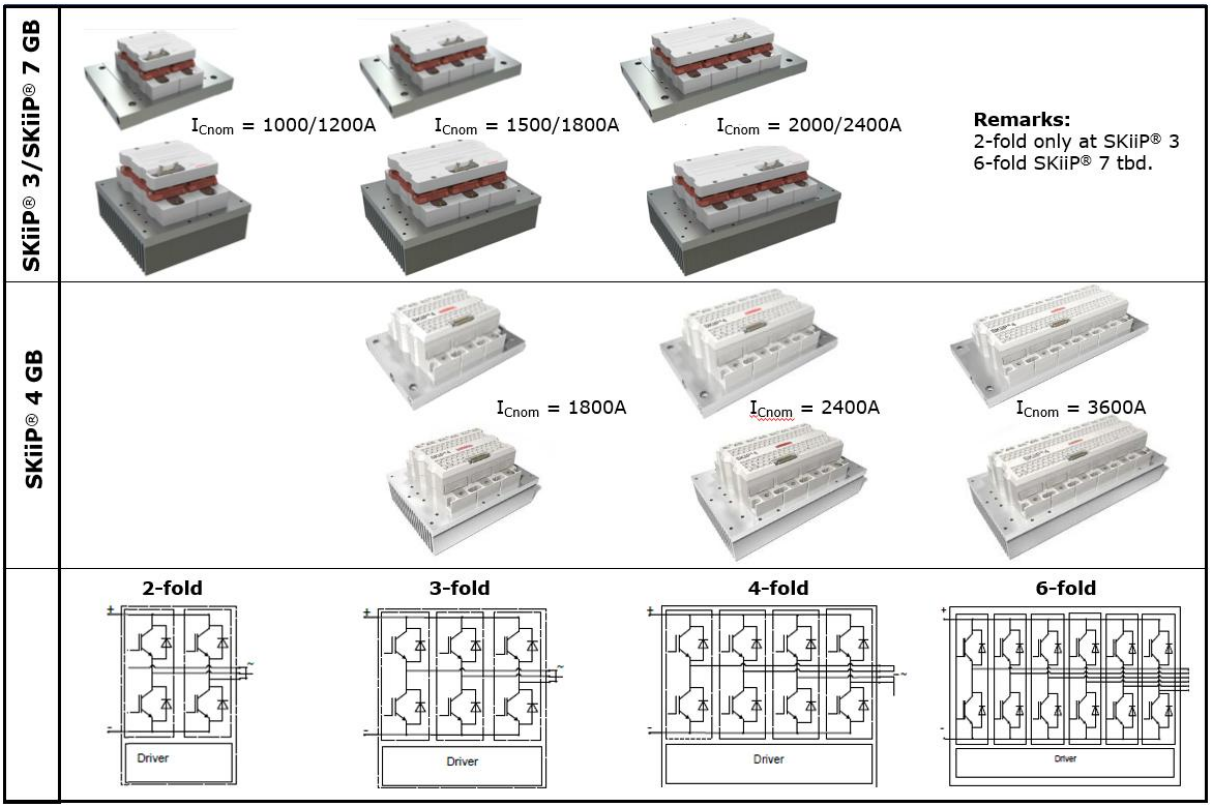


Table 3.3.2 SKiiP IPM standard product ranges for GB halfbridge modules 1200/1700V

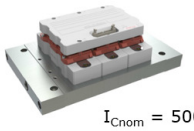
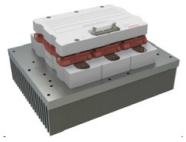
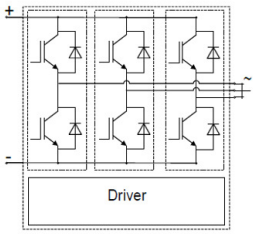
SKiiP 3/SKiiP 7 GD	 I_{Cnom} = 500...600A 	3-fold 

Table 3.3.3 SKiiP IPM standard product ranges for GD sixpack modules 1200/1700V

In the following explanations, primarily the basic characteristics of the three current SKiiP generations are to be compared and corresponding special features are to be highlighted.
For deeper explanations of the power section technologies with their specific characteristics and explanations of the individual driver functions, reference is made to the corresponding chapters in this book. Further information on common technical features and also on the evolution history of the previous SKiiP generations can be found, for example, in [3.15] to [3.18]. For detailed information on properties and application please refer to [3.19] to [3.21] and the corresponding SKiiP datasheets.

3.3.2 Specific properties of the SKiiP power sections

The SKiiP power sections are constructed utilising pressure contact technology and without a copper baseplate. Thus, the pressure to attach the substrate to the heatsink is homogenously induced by a dedicated pressure part on top, which is screwed to the heatsink.
The pressure contact technology facilitates that the Al_2O_3 or AlN substrate is pressed directly onto the heatsink without the use of a baseplate and only a well-defined minimum amount of thermal compound is required. Therefore, the SKiiP technology allows a compact power module design with very low thermal resistances, high thermal cycling capability and low parasitic stray inductances.
Contact springs are used for all auxiliary signal connections between the substrate and the Gate Driver PCB: gates, auxiliary emitters and temperature sensor. These spring contacts allow solder-free connection of the gate driver PCB.
The features resulting from this construction principle have already been described in the chapters 3.1 and 3.2. The Figure 3.3.3 shows exploded-view drawings of the single halfbridges of SKiiP 3/SKiiP 7 and SKiiP 4.

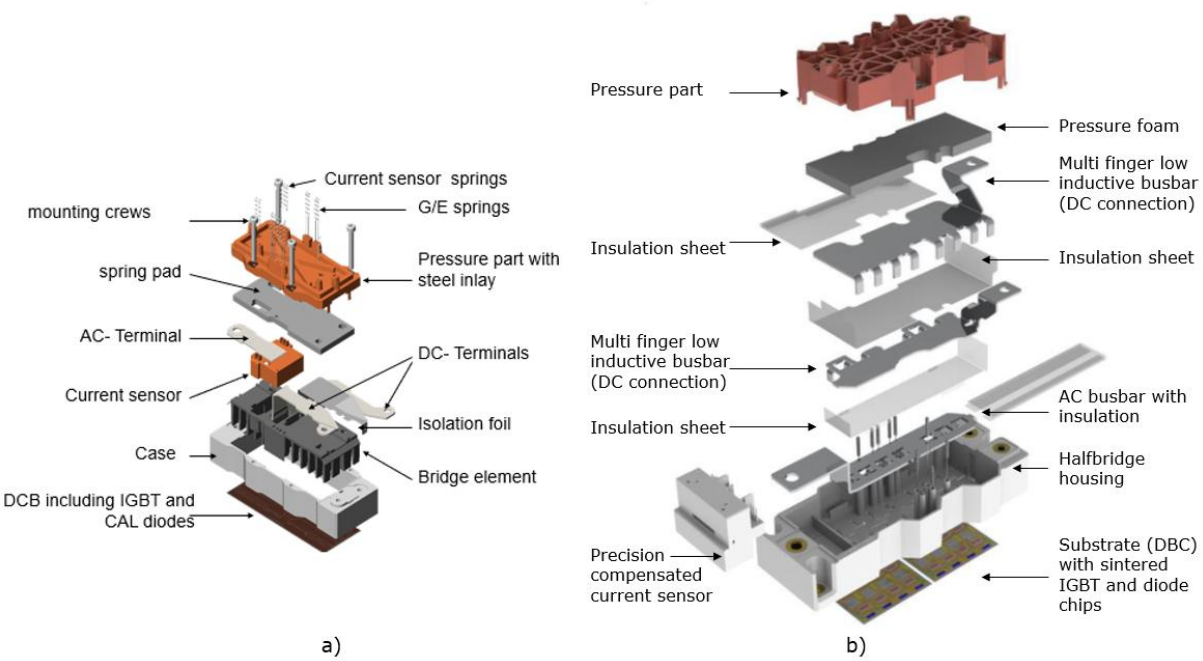


Figure 3.3.3 Explosive drawings of a SKiiP halfbridge: a) SKiiP 3/SKiiP 7; b) SKiiP 4

The SKiiP 4 IPM - intended for particularly high-power applications – uses a main terminals construction principle which differs from that of the SKiiP 3 and SKiiP 7 (Figure 3.3.4).

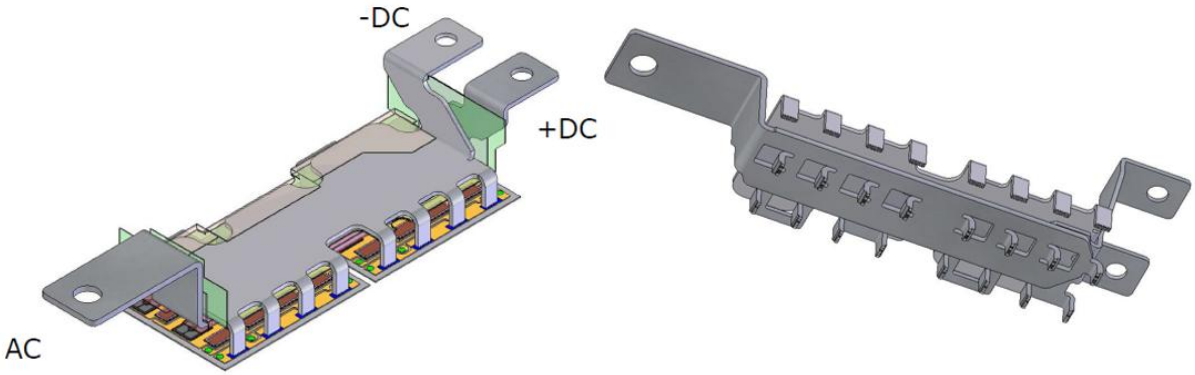


Figure 3.3.4 SKiiP 4 main terminals construction principle

Here, the pressure system ensures that the pressure is evenly applied to the numerous contacts situated next the chips, thus, resulting in a very low thermal and ohmic contact resistances Inside SKiiP 4 and SKiiP 7 the bare chips are sintered and not soldered. This sintering process connects the chip and DBC surface extremely stable up to the melting point of silver which is as high as 962°C. This ensures unsurpassed good load- and temperature cycling performances, see chapters 3.1.3 and 4.4.9.

3.3.3 Specific properties of the SKiiP gate driver units

3.3.3.1 General

The gate driver unit controls the behaviour of the SKiiP under normal and exceptional operation. It receives, checks and conditions the input signals and transforms them on the driver board's high voltage side via an isolation barrier into suitable output signals to control the power section's IGBT halfbridge(s). Also, the gate drive circuit ensures a sensing and proper handling of fault conditions as well as turning-off the IGBT safely even under exceptional conditions like short circuit, overvoltage, etc. Additionally, the SKiiP driver provides the normalized analogue voltage signals of the actual AC-current value, the actual DBC substrate temperature and the actual DC link voltage value (optional, depending on SKiiP-type). These signals are available at the SKiiP gate driver connector for further use in the superimposed control unit.
SKiiP 4 and SKiiP 7 employ various user accessible parameter to configure and customize certain parameter like threshold values through the integrated CANbus interface. Among those functions is an error storage, too providing extended information as required for a detailed failure analysis.
Figure 3.3.5 and Figure 3.3.6 show the block diagrams of the SKiiP-series specific gate driver units. While the drivers for SKiiP 3 and SKiiP 7 use analogue signal transmission, this is done digitally for the drivers of the SKiiP 4.

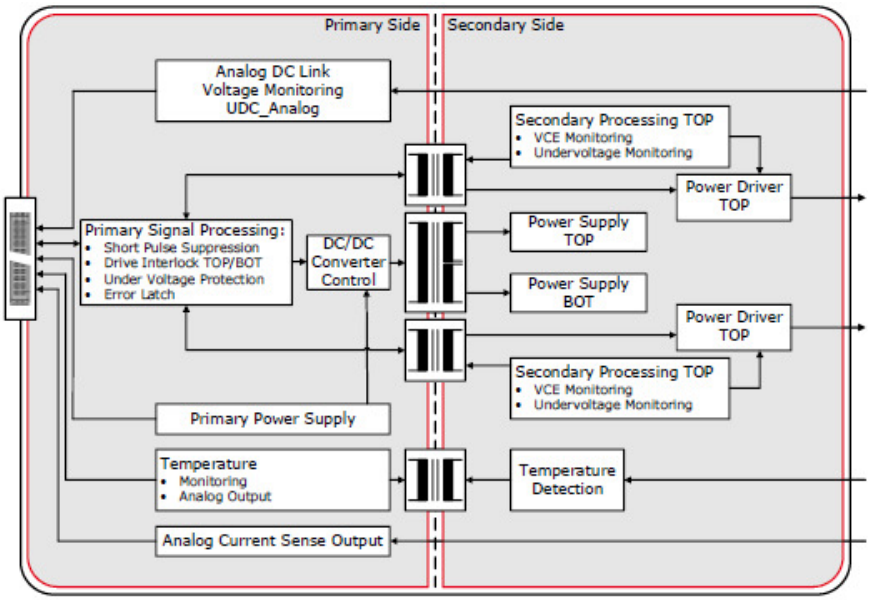


Figure 3.3.5 Block diagram of SKiiP 3/SKiiP 7 gate drivers

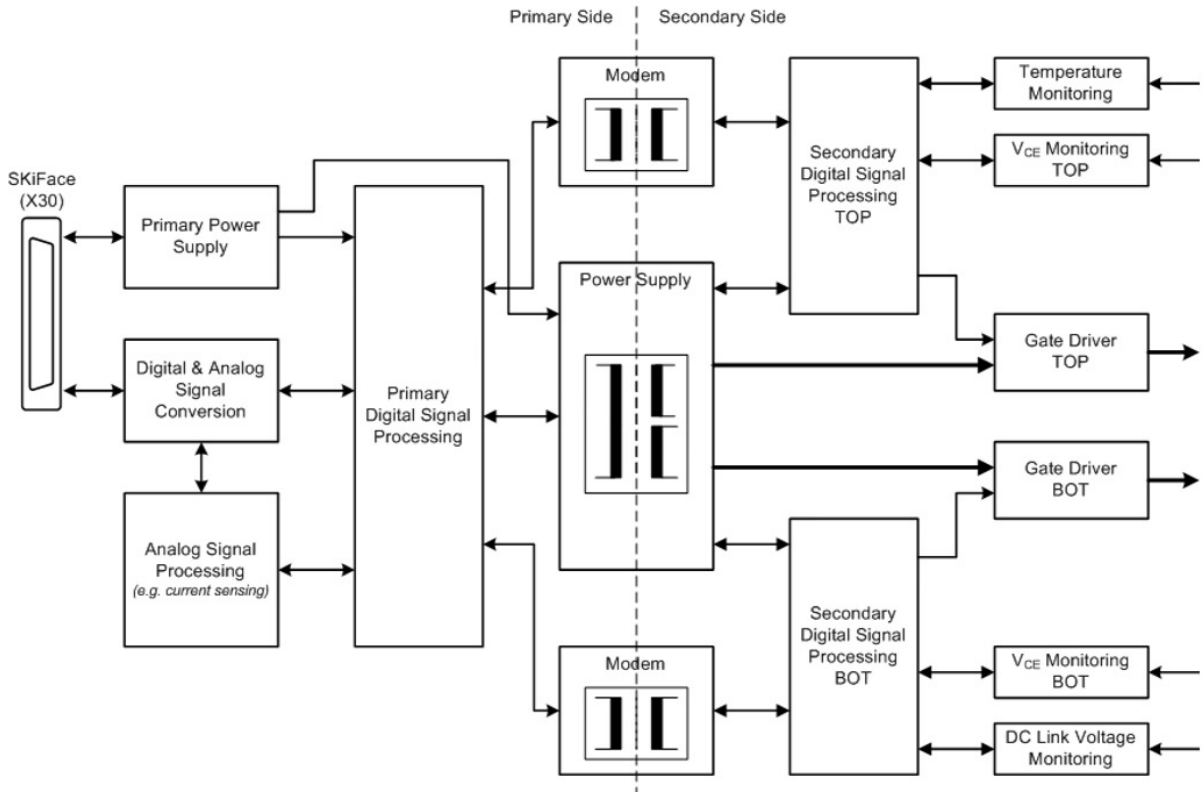


Figure 3.3.6 Block diagram of SKiiP 4 gate driver

The SKiiP 4 gate driver board provides two independent signal channels communicating from low voltage to high voltage side to transfer switching and sensor signals. The signals are transferred by dedicated pulse transformers which are designed according to the standard of reinforced isolation. This approach ensures:

- Essential reduction of temperature and aging effects
- "True" galvanic Isolation between low (primary) and high voltage (secondary) side inclusive temperature and DC link voltage feedback
- High noise immunity

For more detailed information on digital signal transmission or digital driver principles see chapter 9.5.4.3.
Based on the information in Table 3.3.4 and Table 3.3.5 only a few special features of the driver units for the different SKiiP series will be explained in more detail below. For a detailed explanation of the individual driver function blocks and for explanations about differences between the analogue and digital driver principle, please refer to chapter 9.5.4.

3.3.3.2 Controller side interfaces

There are 3 different versions of the gate driver input connectors for the controller side interfaces gate driver:

- Connector DIN41651, 14 pins, male plug (SKiiP 3/SKiiP 7 GB halfbridges)
- Connector DIN41651, 26 pins, male plug (SKiiP 3/SKiiP 7 GD sixpack)
- Connector D-Sub, 25 pins, male plug (SKiiP 4 GB halfbridges)

The connectors include pins for input of external primary side power supply, switching signal inputs, analogue signals outputs, ERROR output, HALT-signal logic (SKiiP 4 and SKiiP 7), a 15V output for external components (SKiiP 3 and optional SKiiP 7) and CANbus interface (SKiiP 4 and SKiiP 7).

3.3.3.3 Primary side power supply

The SKiiP 3 gate driver features a wide-range power supply for primary voltages between 13V and 30V. In case the gate driver is supplied with supply voltage >15V it is possible to use 15V provided at the controller connector of the gate driver as an external power supply, e.g. for a level shifter at the controller's output signals. The input voltage rating for the SKiiP 4 gate driver supply voltage is 24V±20%.

3.3.3.4 Characteristics of the switching inputs and input interface adapters

There are significant differences between SKiiP 3 and SKiiP 4 input characteristics:

- *SKiiP 3*: The switching signal inputs TOP IN for the TOP IGBT and BOT IN for the BOT IGBT with 10kΩ impedance use a positive 15V CMOS logic (threshold voltage specification HIGH: VIT+ = 12.6V and LOW: VIT- = 4.6V).
- *SKiiP 4*: The switching signal inputs for the TOP IGBT and HB_BOT for the BOT IGBT with about 13kΩ impedance use a digital positive / active high logic (input HIGH = IGBT on; input LOW = IGBT off) characteristic (threshold voltage specification HIGH: VIT+ = 0.7 · VS and LOW: VIT- = 0.3 · VS). For driving the inputs HB_TOP and HB_BOT it is mandatory to use line drivers with a push-pull characteristic. Pull up and open collector output stages must not be used for driving these inputs.

SKiiP 4 Gate driver interface "SKiFace adapter"

Since SKiiP 3 and SKiiP 4 interfaces have different configurations, it is not possible to run a SKiiP 4 system with a SKiiP 3 infrastructure. The SKiFace Adapter Board allows to adapt the SKiiP 3 system controller signals to SKiFace interface of SKiiP 4 system. The adaption of SKiiP 4 to a SKiiP 3 controller interface should only be done to test the compatibility SKiiP 4 in a SKiiP 3 design but should be equipped with a SKiiP 4 interface in the final solution.

SKiiP 3 and SKiiP 4 Fibre optic interface adapters

The SKiiP F-Option Boards allows the controlling of SKiiP 3 or SKiiP 4 by means of fibre optics for optimal noise immunity.
A SKiiP F-Option Board is able to control:

- one SKiiP GB type
- up to 4 SKiiP GB type in parallel via SKiiP Parallel Board (see [3.22] or [3.23] for details)
- most of Semikron Danfoss IGBT gate drivers

The two switching signals (TOP/BOT) and the error signal are transferred via optical connection. In addition, the analogue signals are available on the controller connector X1 (DIN41651 for SKiiP 3).

For SKiiP 4, there are three versions of F-Option Board available:

- Version 1: SKiiP 4 F-Option Board with D-Sub connector, no plastic case
- Version 2: SKiiP 4 F-Option Board with D-Sub connector
- Version 3: SKiiP 4 F-Option Board without D-Sub connector

The SKiiP 3 F-Option Boards can be used both for:

- mounting directly on the SKiiP 3 top cover (can only be done by Semikron Danfoss)
- mounting on the SKiiP 3 Paralleling Board or Driver Board (can be done by customer).

The electrical connection between SKiiP 3 F-Option Board and SKiiP 3 driver board is realized by 14-wired ribbon cable, which is part of the Board. For SKiiP 4, this connection must be realized by 25-wired ribbon cable. The built-in connector of the SKiiP 4 F-Option Board can be directly plugged-in on the SKiiP 4 top cover (Variants 2 and 3) or on SKiiP 4 Paralleling Board (Variant 1). In other cases, the usage of cable extension up to 1.5m is allowed.
The two switching signals (TOP/BOT) and the GPIO error signal are transferred via optical connection. In addition, the analogue signals as well as the CAN-Bus signals are available on the D-Sub connector X2, if present.

The main functions of the SKiiP F-Option boards are shown in the Figure 3.3.7 for SKiiP 4:

- F-Block 1: Converting the optical TOP/BOT switching signals from the board's controller connectors to the SKiiP input connectors
- F-Block 2: Converting the SKiiP 3 ERROR signal or the SKiiP 4 GPIO signal from SKiiP connector to optical error signal ERROR_OUT,
- F-Block 3: External power supply,
- F-Block 4: Forwarding of analogue signals (AC output current, DBC temperature or DC voltage) from SKiiP 3 to the controller connector,
- F-Block 5: Forwarding of SKiiP 4 CANbus to the controller connector,
- The SKiiP 4 HALT and GPIO Signals are available on the controller connector as well.

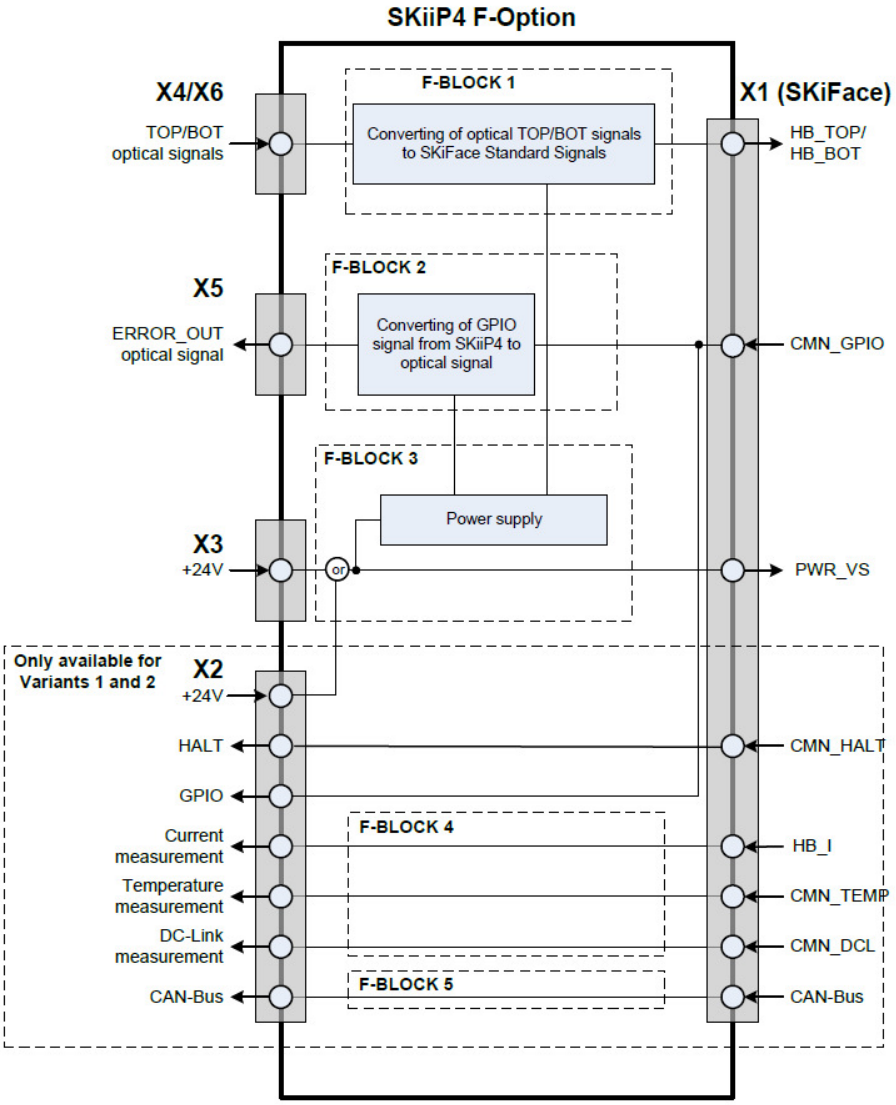


Figure 3.3.7 Block diagram of SKiiP 4 F-Option board main functions

The F-Blocks 4 and 5 as well as +24V routing from controller connector X2 to SKiiP 4 connector X1 (please see chapter 9 for details) are available only for F-Option versions 1 and 2, see above.

3.3.3.5 Error processing

In case of an error caused by:

- Overcurrent
- Exceeding the maximum DBC-sensor temperature
- DC link overvoltage (only SKiiP 4 and selected SKiiP 3 and SKiiP 7)
- Exceeding the maximum permissible switching frequency (only SKiiP 4)
- Overlapping the TOP/BOT switching signals (only SKiiP 4)
- Undervoltage of the primary side
- Undervoltage of the secondary side (only SKiiP 3 and SKiiP 7)
- Exceeding the maximum driver PCB temperature (only SKiiP 4)
- Load- or SKiiP-internal short circuit
- Internal driver error (only SKiiP 4)

the SKiiP 3 gate driver will turn off the open collector transistor to set the ERROR out signal on the corresponding pins to HIGH state (not ready to operate) for the time error is present or at least error memory reset time t_{pRESET}. Please refer to [3.19] for more detailed information.
If the maximum DBC-sensor temperature is exceeded, the open-collector overtemperature output is also set to HIGH state.

At the SKiiP 4, the gate driver will set the HALT signal to LOW state (indicating that the SKiiP 4 is not ready to operate) as long as the error is present, or at least for the "error memory reset time", t_{pRESET}. Please refer to [3.20] for more detailed information.
The IGBT will be turned-off and switching pulses from the controller won´t be transferred to the output stage. During this time the driver will check if the TOP and BOT switching input signals are set to LOW. If this is the case and no error is present anymore the driver will release the ERROR signal (SKiiP 3) or HALT signal (SKiiP 4). If the input signals have not been switched to LOW state the driver will pull the ERROR signal (SKiiP 3) to HIGH or HALT signal (SKiiP 4) to LOW (dominate) as long as the switching input signals are not LOW. So, in case of error the switching input signals should be set to LOW within the error memory reset time t_{pRESET} and not be activated before the ERROR signal is in LOW state (SKiiP 3) respective the HALT signal is in HIGH state (SKiiP 4) again.
At the SKiiP 4, the processing in case of failure includes a reaction of the HALT and GPIO1/CPIO2 Error logic. All these three signals are digital input/output bidirectional status signals, referred to the driver supply voltage V_S. The low active HALT signal logic enables and disables the gate driver (LOW: IGBT driver disabled, HIGH: enabled). The inputs are dominant/recessive (settable and readable by driver and user controller board)
The driver will set the HALT signal to LOW state during the power on reset and when an error status is active. The driver releases the HALT signal (recessive HIGH state) after the power-on reset time has elapsed and no error is present and both TOP/BOT signals are LOW and after the error reset time has elapsed and no error is present and both signal inputs TOP/BOT are LOW.
The HALT signal outputs of several SKiiP can be connected together and also to other components with open drain/collector output (wired ore). The HALT signal is set to LOW state when one of the connected SKiiP or additional components is not ready to operate.
The GPIO1 signal is the inverted HALT signal that can be used as error output signal of the SKiiP 4 (except with activated FRT function, see below). The GPIO2 signal can be used for synchronisation at parallel operation of SKiiP. It is only available after activation via CANbus interface.

3.3.4 Gate driver integrated sensing and protection functions

3.3.4.1 General

All SKiiP IPM are equipped with short circuit protection by dynamic Short Circuit Protection (DSCP) The DSCP circuit is facilitating the short circuit sensing in case of load short circuit and also internal short circuit ("shoot through protection"). A protection circuit monitors the collector-emitter voltage V_{CEsat} of the IGBT during the on-state of the device and derives a suitable threshold from this value to turn-off the IGBT in case of a short circuit. Once the threshold level is exceeded a blanking time delay starts and ignores the high current for this period to increase the noise immunity of this circuit. The activated DSCP will result in ERROR state and an ERROR or HALT signal will be issued correspondingly. More detailed explanations on the function of DSCP can be found in chapter 9.5.4.6. All SKiiP IPM are equipped with sensors for measurement of AC load current and overcurrent protection, explained in chapter 3.3.4.2 and sensors for measurement of DBC temperature and overtemperature protection, explained in chapter 3.3.4.3. Additional, in gate drivers of all SKiiP 4 and of selected SKiiP 3/SKiiP 7 an analogue measurement of DC link voltage - combined with an overvoltage protection is installed, see explanations in chapter 3.3.4.4. Furthermore, all SKiiP 4 IPM have a sensor for driver-PCB overtemperature protection and protections against extension of a maximum permissible switching frequency, explained in chapter 3.3.4.5. The output signals of the analogue sensors enable both SKiiP-internal protective functions and customer-side use for system control and protection.

The protection functions also include switching signal processing functions, such as

- Top / bottom switch interlock time (dead time for preventing the TOP and BOT switches turn-on simultaneously,
- Short pulse suppression time (suppresses short turn-on and off-pulses at the input pins),
- Power-On-Reset of the signal inputs for a defined time after turning on the supply voltage.

More detailed information on the realisation of these time intervals can be found in chapter 9.5.4.

3.3.4.2 Analogue AC current sensing and overcurrent protection OCP

Current sensing

$$9.5.4.6\Delta I = I_C \cdot 0.13\% + I_{actual} \cdot (1.37\% + / \Delta T / \cdot 0.002\%/K$$

ΔI: absolute deviation of the current value per halfbridge

I_C: nominal current per halfbridge
I_{actual}: actual measured current level per halfbridge
ΔT: difference between T_{amb} and 25°C

By calculation of the accuracy for low currents the offset value cannot be neglected and has to be considered as additional tolerance. Moreover, the AC -current sensors are used to protect the SKiiP against overcurrent (see "overcurrent protection" below).

Overcurrent protection

The overcurrent protection (OCP) is based on this integrated current sensor measurement and, hence, it protects based on a load imposed current. The application shall be selected to ensure that the peak load current stays safely below the DSCP level. OCP reacts independently from the temperature level and provides a reliable protection of the SKiiP.
If the AC output current is higher than the datasheet-specified trip level I_{TRIPSC}, the IGBT are immediately switched off and switching pulses from controller are ignored. The error signal ERROR will be set to HIGH state (SKiiP 3) respective the signal HALT will be set to LOW state (SKiiP 4).
In all SKiiP 3/SKiiP 7 with Al_2O_3 ceramic substrate, 100% of the nominal collector current I_{Cnom} corresponds to 8V output voltage. The overcurrent trip level I_{TRIPSC} is set to 125% I_{Cnom}, equivalent to 10V output voltage. SKiiP 3 with AlN ceramic substrate – each assembled with the identical chips - are specified with a higher nominal current; however, the normalisation of the AC current signal and the I_{TRIPSC} values are identical to the values of the corresponding SKiiP with Al_2O_3 ceramic (Table 3.3.4).

Topology/Size SKiiP® 3 SKiiP® 7	Voltage class, insulation and cooling	Nominal collector current I_{Cnom} [A]	Ratio of current analog value [mv/A]	Analogue current trip level I_{TRIPSC} [V] @ 10V	Ratio of trip level to nom. collector current
3-fold GD	1200V Al_2O_3	600	13.33	750	1.25
	1200V AlN aircooled		16	625	1.04
	1200V AlN watercooled		13.33	750	1.25
	1700V Al_2O_3	500	16	625	
	1700V AlN	570			1.1
2-fold GB*)	1200V Al_2O_3	1200	6.67	1500	1.25
	1700V Al_2O_3	1000	8	1250	
	1700V AlN	1200			1.04
3-fold GB	1200V Al_2O_3	1800	4.44	2250	1.25
	1700V Al_2O_3	1500	5.33	1875	
	1700V AlN	1800			1.04
4-fold GB	1200V Al_2O_3	2400	3.33	3000	1.25
	1700V Al_2O_3	2000	4	2500	
	1700V AlN	2400			

*) exclusively with SKiiP® 3

Table 3.3.4 SKiiP 3/SKiiP 7 signal characteristics and trip levels of AC current measurement

In SKiiP 4, the corresponding value of output voltage to current also depends on the number of SKiiP-folds. As with SKiiP 3, 100% of the nominal collector current I_{Cnom} corresponds to 8V output voltage and the overcurrent trip level I_{TRIPSC} is set to 150% I_{Cnom}, equivalent to 10V output voltage, see Table 3.3.5.

SKiiP® 4 size	Nominal collector current I_{Cnom} [A]	Analogue current trip level I_{TRIPSC} [V] @ 10V	Ratio of voltage to output current value [mV/A]	Ratio of trip level I_{TRIPSC} to I_{Cnom}
3-fold GB	1800	2700	3.7	1.5
4-fold GB	2400	3600	2.78	1.5
6-fold GB	3600	5400	1.85	1.5

Table 3.3.5 SKiiP 4 signal characteristics and trip levels of AC current measurement

At SKiiP 3 and SKiiP 4, the short OCP circuit is also protecting against short circuit and overcurrent situations – at the most types of SKiiP 4 1700V additional by initiating a soft turn-off function, described in chapter 9.5.3.2.

The special SKiiP 4 soft turn-off functions, called "IntelliOff" generates two different gate turn-off speeds determined by the internally connected and optimized gate resistors. The suitable gate turn-off speed will be chosen as a function of the actual measured AC current value. As shown in Figure 3.3.8, the two different turn-off speed scenarios are

- Hard switch-off: optimised for low switching losses
- IntelliOff: optimised for reduced overvoltage at overload (see also "soft turn off" feature in chapter 9.5.3.2)

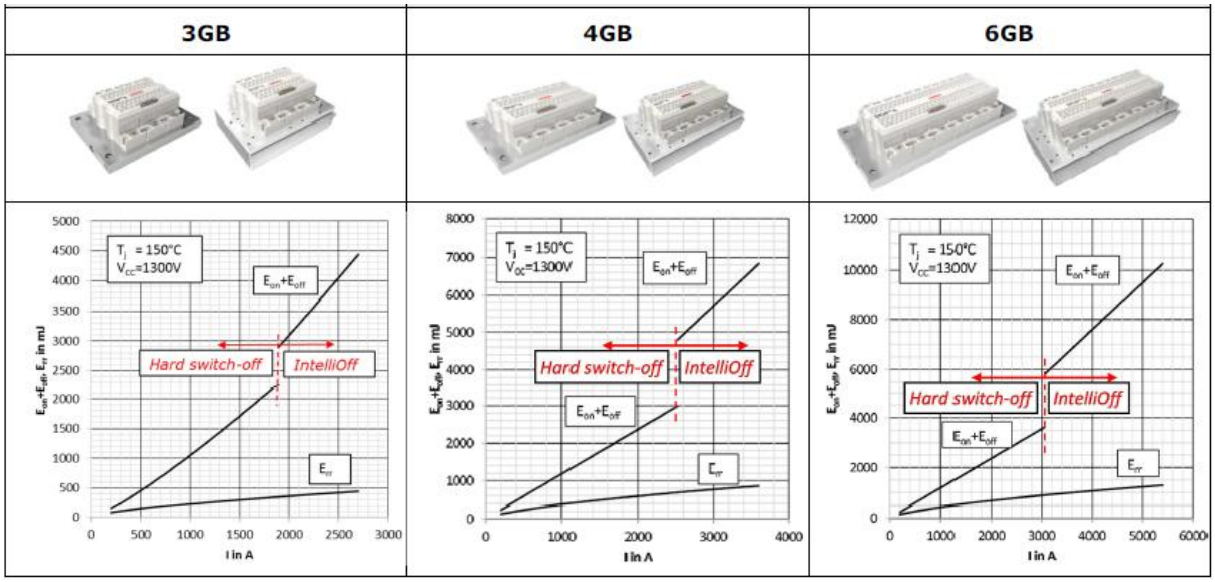


Figure 3.3.8 IntelliOff functionality and impact on switching energy dissipation of 1700V SKiiP 4 IPM modules

3.3.4.3 DBC temperature sensing and overtemperature protection

Temperature sensing

The SKiiP employs an integrated DBC-temperature sensor, consisting of a chip resistor with PTC temperature dependent characteristics. There are differences in the placement of the temperature sensor between SKiiP 3/SKiiP 7 and SKiiP 4, see Figure 3.3.9.

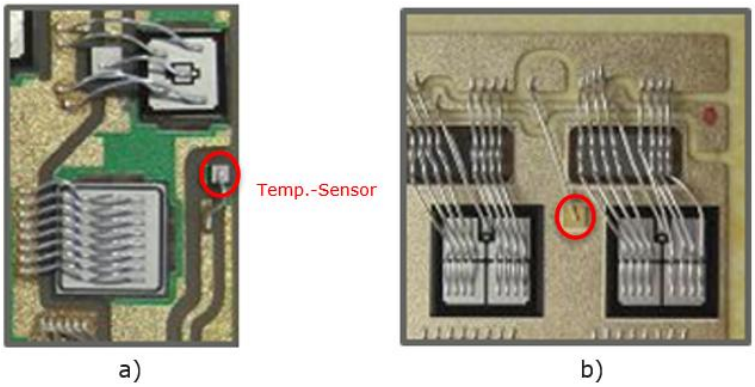


Figure 3.3.9 Placement of DBC temperature sensor: a) at SKiiP 3 on a separate (isolated) copper layer on the DBC substrate close to edge; b) at SKiiP 4 on the same copper layer like IGBT- and diode chips

The different placement of the temperature sensors also results in small differences in the thermal models of SKiiP 3/SKiiP 7 and SKiiP 4, which may need to be taken into account in thermal simulations and in the design of protective measures.
At SKiiP 3/SKiiP 7, the temperature sensor is located close to the DBC-edge on the separate DBC copper layer, at SKiiP 4 on the same copper layer like IGBT-collector and diode cathode.
This makes the temperature difference between junction and sensor higher and between sensor and ambient lower in comparison to SKiiP 4.
Only one of the temperature sensors is monitored by the gate driver. The monitored sensor is in the middle of the SKiiP (Figure 3.3.10). The protection level is matched to the maximum operation

temperature of the power semiconductors. During operation there will be a temperature profile along the heatsink from cool at the inlet of the coolant to warm at the outlet.

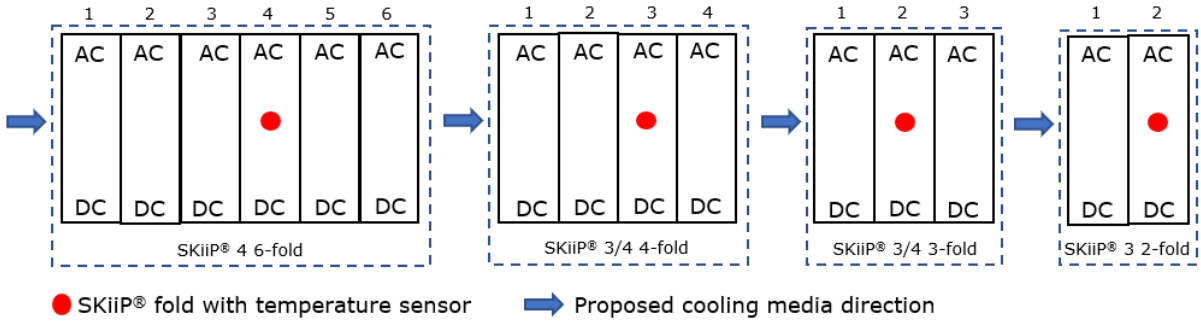


Figure 3.3.10 Temperature sensor positions inside various SKiiP sizes and resulting proposed cooling fluid direction (exemplary at SKiiP 3 and SKiiP 4)

An evaluation circuit realised on the gate driver provides a normalized, analogue voltage signal of the actual ceramic substrate temperature value, available at the SKiiP's controller interface with the characteristics given in Table 3.3.6.

Characteristic	SKiiP® 3 SKiiP® 7	SKiiP® 4
Minimum measurable temperature T_{MIN} [°C]	30	30
Analogue temperature signal $TEMP_{ana}$ [V] @ 30°C [V]	1	-
Analogue temperature signal CMN_TEMP [V] @ 30°C	-	0
Analogue temperature signal $TEMP_{ana}$ [V] @ 115°C	10	-
Analogue temperature signal CMN_TEMP [V] @ 150°C	-	10
Tolerance of analogue signal [%] @ T_{trip}	±3	±5
Bandwidth f_{0Tana} [Hz]	5	5 (-3db)
Trip level T_{trip} [°C] for overtemperature ERROR/HALT state	115	135
Threshold level for reset after failure event [°C]	-	90

Table 3.3.6 Characteristics of the DBC-temperature evaluation circuit

As can be seen from the SKiiP 3 block circuit diagram in Figure 3.3.5, the evaluation of the temperature sensor signal in the SKiiP 3 is carried out on the primary side of the driver - electrically separated from the secondary side by the DBC substrate located underneath the sensor. At SKiiP 4, the temperature measurement circuit is realised on the secondary side of the driver board, see block diagram in Figure 3.3.6. It generates an equivalent voltage which is digitized, transmitted to the primary side via a transformer for galvanic isolation and converted into an analogue signal on primary side. The analogue temperature signal is available on the customer interface with characteristics given in Table 3.3.6 above.

Overtemperature protection

SKiiP 3 /SKiiP 7: If the signal $Temp_{anaout}$ from temperature sensor reaches the trip level (T_{TRIP}, see Table 3.3.6 above), the IGBT will be turned-off and switching pulses from the controller won´t be transferred to the output stage. The error signals ERROR out and $Overtemp_{out}$ will be set in HIGH state. After cooling down, or at least for the "error memory reset time", $t_{pRESET.}$ the driver will check if the switching input signals TOP IN and BOT IN are set to LOW. If this is the case and no other error is present anymore the driver will release the ERROR signal.

SKiiP 4: A temperature rise up to the trip level T_{TRIP} will set the HALT signal to LOW state as long as the DBC temperature exceeds the threshold level of 90°C, or at least for the "error memory reset time", $t_{pRESET.}$ The IGBT will be turned-off and switching pulses from the controller won´t be transferred to the output stage. During this time the driver will check if the switching input signals HB_TOP and HB_BOT are set to LOW. If this is the case and no other error is present anymore the driver will release the HALT signal.

The built-in overtemperature trip levels of 115°C (SKiiP 3) resp. 135°C (SKiiP 4) are sufficient for most aircooled applications to protect the system. For some liquid cooled applications or short time

overloads the thresholds might be too high. In this case another protection trip level is needed and the customer can use the analogue temperature output to protect the system.
In general, for both air- or watercooled systems the protection of the built-in temperature cannot perfectly protect the SKiiP against overtemperature, especially when sufficiently fast transient load conditions occur. A detailed system verification is required to verify the efficient protection under customer specific conditions.

3.3.4.4 DC Link voltage monitoring and overvoltage protection

Voltage monitoring

The DC link voltage (V_{DC}) monitoring is standard for all GD-type SKiiP 3 and SKiiP 7 with DIN connector and all SKiiP 4. For GB-type SKiiP 3 the DC link-voltage sensing is available instead of temperature measurement, for all SKiiP 7 with SUB-D connector the DC link voltage sensing is available.
At SKiiP 3 and SKiiP 7, V_{DC} is sensed on the secondary side between DC plus and DC minus terminal by means of internal serial resistor divider and a high impedance differential amplifier. The circuit is designed, manufactured and tested for safety isolation according to the standard EN50178. The analogue DC link voltage signal - filtered with a time constant of 500µs – is available on the SKiiP customer interface with characteristics given in below.
At SKiiP 4, V_{DC} the DC link is also sensed on the secondary side of the driver board between the DC plus and DC minus terminal. After secondary-size digitising and transmitting the measured value to the primary side via a galvanic isolation, the digital value is converted back to an analogue signal on the primary side, see block diagram in Figure 3.3.6. The analogue DC link voltage signal is available on the SKiiP customer interface with characteristics given in Table 3.3.7.

Characteristic	SKiiP® 3		SKiiP® 7		SKiiP® 4	
	1200V	1700V	1200V	1700V	1200V	1700V
Analogue DC link voltage signal U_{DCana} [V] @ 900V	9	6.5	n.a.	6.5	9	6.75
Analogue DC link voltage signal U_{DCana} [V] @ 1170V	n.a.	9	n.a.	9	n.a.	8.78
Analogue DC link voltage signal U_{DCana} [V] @ 1200V	n.a.	n.a.	n.a.	n.a.	n.a.	9
Voltage ratio [mV/V]	10	7.69	10	7.69	10	7.5
Tolerance of analogue signal [%] @ V_{DCTRIP} over full temperature range	±2.5	±2.5	±2.5	±2.5	±3	±3
Bandwidth (phase shift) f_{0Uana} [Hz]	320	320	320	320	1800	1800
Nominal trip level V_{DCtrip} [V] for DC-link overvoltage ERROR or HALT state	900	1200	830	1300	980	1340

Table 3.3.7 Characteristics of the DC link monitoring circuit

DC link overvoltage protection

The DC link overvoltage protection is implemented for all SKiiP with integrated DC link voltage sensing. In case the DC link overvoltage protection is implemented and the operating DC link voltage is higher than V_{DCtrip} (see Table above), the IGBT will be turned off and switching pulses from controller won´t be transferred to the output stage. At SKiiP 3, the error signal ERROR will be set in HIGH state. At SKiiP 4, the signal HALT will be set to LOW state.
At VDC lower than V_{DCtrip}, or at least for the "error memory reset time", $t_{pRESET.}$ the driver will check if the switching input signals TOP IN and BOT IN (SKiiP 3) resp. HB_TOP and HB_BOT (SKiiP 4) are set to LOW. If this is the case and no other error is present anymore the driver will release the ERROR resp. HALT signal.

3.3.4.5 Protection against exceeding the maximum permissible switching frequency

All the SKiiP have a maximum permissible switching frequency, caused by the power losses of gate driver, power semiconductors and AC current sensors. The limit values are given on the first page of the data sheet.
At SKiiP 3 and SKiiP 7, no error signal will be set if the maximal allowed switching frequency for the particular SKiiP will be exceeded. It is the user's responsibility to limit the frequency according to the data sheet given maximum ratings.

The ambient temperature has got an influence on the max. possible switching frequency of SKiiP 3, too. In case of higher ambient temperature, the derating of the switching frequency must be considered (for all SKiiP 3 types except of 4-fold GB-type). The derating diagrams for 2-fold and 3-fold SKiiP 3 GB-types as well as GD-type are shown in the Figure 3.3.11.

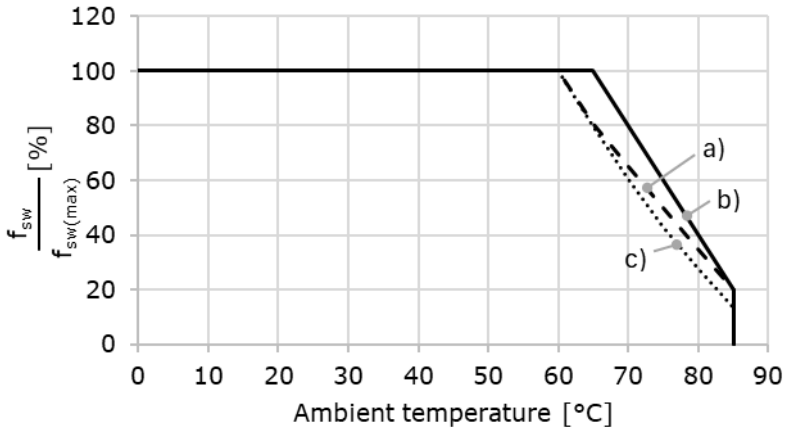


Figure 3.3.11 Switching frequency derating diagrams for SKiiP 3: a) 2-fold GB-Types; b) 3-fold GB-Types; c) GD-Types

All SKiiP 4 gate drivers are equipped with a protection function against exceeding the maximum permissible switching frequency f_{sw}. In order to prevent the module against overheating, the switching signal inputs HB_TOP and HB_BOT are monitored with respect to oscillations. An error latch will be set if the switching frequency is higher than twice the corresponding f_{sw} for a sequence of following pulses.

3.3.4.6 SKiiP 4 FRT (Fault Ride Through) – function

SKiiP 4 IPM in particular are widely used in wind turbine inverters that have to meet grid requirements such as Fault Ride Through (FRT) or Low Voltage Ride Through (LVRT). If the wind turbine is equipped with a doubly-fed induction generator, only the rotor current is controlled by the inverter. In the case of an FRT or LVRT, the rotor current may briefly increase to values above the overcurrent trip level I_{TRIPSC} of the SKiiP.
Regardless of the response of the customer's controller, the SKiiP would block both IGBT as well as set the CMN_HALT signal to LOW and the CMN_GPIO1 signal to HIGH until the driver-internal error memory reset time t_{pRESET} has expired and both driver input signals HB_TOP and HB_BOT are set to LOW by the customer's controller. In most cases, however, t_{pRESET} is too large to meet the requirements for the wind turbine's behaviour in the event of grid faults. For these applications, SKiiP 4 IPM have a so-called FRT function that can be activated via the CANbus interface.
An activated FRT function changes the error handling in the SKiiP 4 driver In this case CMN_GPIO1 is no longer the inverted CMN_HALT signal. An overcurrent error sets the CMN_GPIO1 signal to HIGH and disables the control signals for the IGBT as long as I_{TRIPSC} is exceeded. However, the signal CMN_HALT is not set to LOW and the overcurrent error is not stored in the error memory of the SKiiP.
After a time period t_{pReset} of 200µs - starting when the rotor current is dropped below I_{TRIPSC} and the control signals are blocked by the customer - the SKiiP 4 driver enables the switching signals again as long as I_{TRIPSC} is not exceeded again. The SKiiP-freewheeling diodes must continue to conduct the rotor current despite blocked switching signals, since the SKiiP overcurrent protection is deactivated and the thermal protection of the SKiiP cannot protect the diodes in this case. A thermal simulation of the specific fault cases by the customer is therefore essential in this context.

3.3.5 SKiiP 4 CANbus interface

The CANbus interface employs comprehensive interaction with the SKiiP 4, e.g., it provides the possibility to read out the type of error occurred and when it occurred. In addition to this, the CAN-interface is used to parameterize and configure, e.g.to activate/deactivate dedicated features of the SKiiP 4, and to allow a customization to a certain extent. That configuration through the CAN bus allows protection parameter settings like the DC link trip function for example as well as the activation of a dedicated function to ride through extraordinary wind turbine specific application conditions. The CANbus interface is available at Pins CAN_H and CAN_L as shown in Figure 3.3.12.

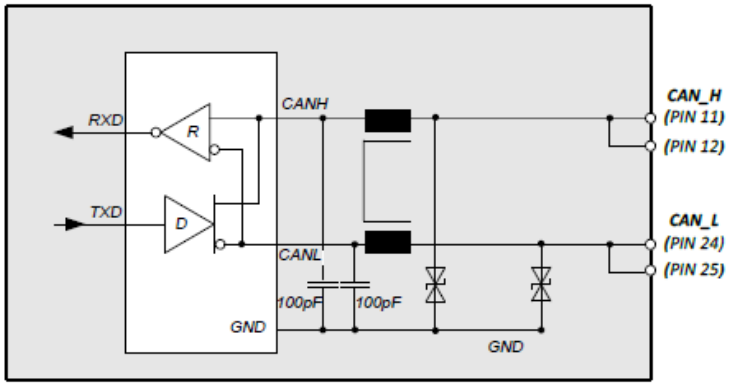
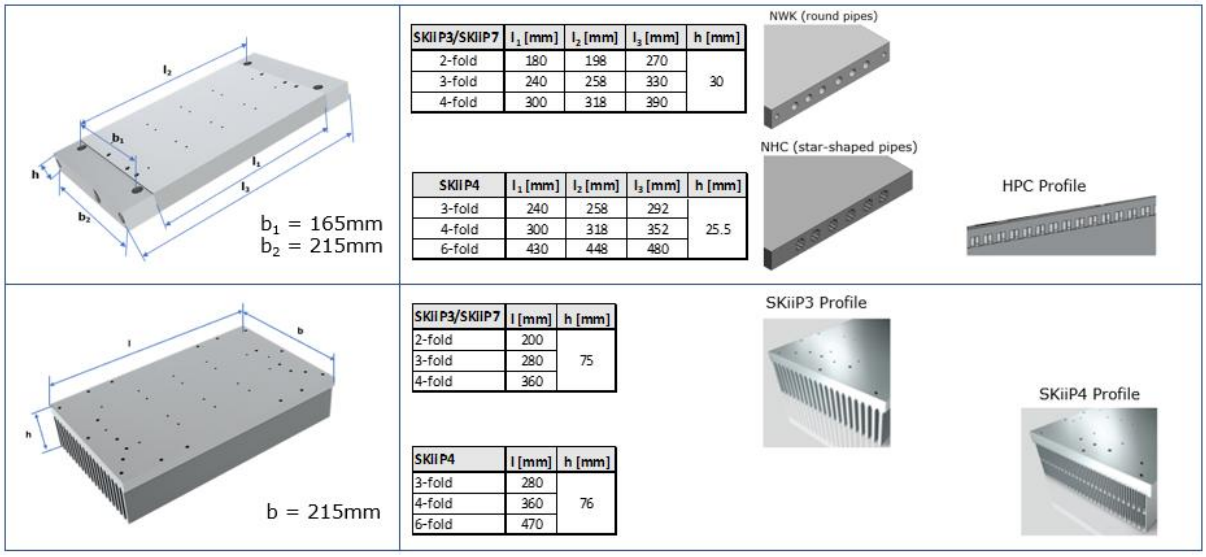


Figure 3.3.12 SKiiP 4 CANbus interface

For a detailed description of the SKiiP 4 CANbus interface please refer to the documents [3.23] and [3.24].

3.3.6 Properties of the SKiiP cooling systems

There are various standard heatsinks for SKiiP 3, SKiiP 4 and SKiiP 7 integrated (customer specific heatsinks differ). Figure 3.3.13 illustrates the mechanical dimensions of the standard heatsinks for the various air- and watercooled SKiiP versions.



SKiiP3/SKiiP7	l_1 [mm]	l_2 [mm]	l_3 [mm]	h [mm]
2-fold	180	198	270	30
3-fold	240	258	330	
4-fold	300	318	390	

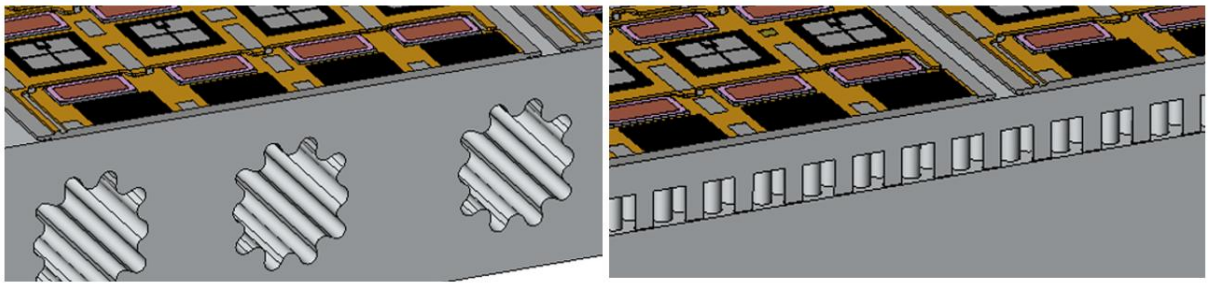
SKiiP4	l_1 [mm]	l_2 [mm]	l_3 [mm]	h [mm]
3-fold	240	258	292	25.5
4-fold	300	318	352	
6-fold	430	448	480	

SKiiP3/SKiiP7	l [mm]	h [mm]
2-fold	200	75
3-fold	280	
4-fold	360	

SKiiP4	l [mm]	h [mm]
3-fold	280	76
4-fold	360	
6-fold	470	

Figure 3.3.13 Mechanical dimensions of standard heatsinks for SKiiP 3, SKiiP 4 and SKiiP 7

In the field of water coolers, the SKiiP High-performance cooler HPC is the latest development. Various SKiiP 4 and SKiiP 7 IPM types are available with this purpose developed high-performance pin fin water cooler (HPC) as an alternative to the existing water-based cooler (NHC).
A comparison of this 2, which both have been optimised for SKiiP 4, are shown in Figure 3.3.14.



a) b)

Figure 3.3.14 a) SKiiP 4 standard star shaped cooler NHC; b) SKiiP 4/SKiiP 7 high-performance cooler HPC

The geometry of the HPC pin fin design has been optimised for the specific chip sizes and chip positions on the SKiiP halfbridges. The cross-section of the cooler shows that the path that the heat travels from the chips to the water has been significantly shortened and the heat flow is distributed much more homogeneously across the entire DBC substrate for all chips.
As a result, the thermal resistance of the mounted chips on the HPC cooler is about half that of the NHC water cooler with a similar amount of coolant flow rate. The pressure loss, however, is only slightly higher.
For a SKiiP 4 mounted on an HPC, this means a possible increase in output current of around 25% with the same junction-to-water temperature increase. As an example, Figure 3.3.15 shows the simulated junction temperature as a function of the output current for the conventional NHC cooler and the HPC cooler in comparison.

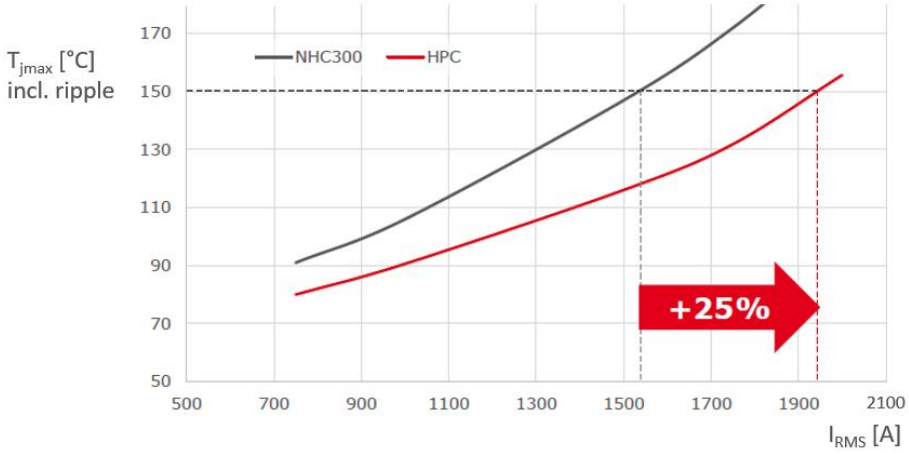


Figure 3.3.15 Output current comparison of SKiiP2414GB17E4-4DW with conventional NHC300 cooler and SKiiP2414GB17E4-4DUHP with high-performance HPC cooler at V_{DC} = 1150V, m = 0.85, cos φ = 0.85, f_{sw} = 2.5kHz, $T_{Coolant}$ = 55°C (16l/min, 50 % ethylene glycol).

3.3.7 Environment conditions, isolation coordination and reliability

3.3.7.1 Environment conditions

Overviews of environmental conditions acc. to DIN EN IEC 60721-3-3 that the SKiiP IPM fulfil, are included on page 4 of the respective SKiiP IPM datasheets. Detailed explanations of the meaning of the listed application classes can be found in chapter 10.5. This is merely to emphasise the extended climatic operating range of the SKiiP IPM compared to other power modules, achieved primarily by means of mechanical and chip design optimisation for humidity protection during operation.
Most electrical equipment is designed to operate within the DIN EN IEC 60721-3-3 climatic class 3K22 (formerly 3K3). In addition to temperature and pressure ranges, the 3K22 class gives an allowable range of relative humidity from 5% to 85%, without allowing condensation. Furthermore, the absolute humidity is limited to 25g/m³. While the 3K22 range only defines an allowable temperature range of 5° to 40°C, SKiiP can operate in a larger temperature range (-40°C to 85°C) which results in an extended operating area as shown in blue in Figure 10.5.5. Please refer to chapter 10.5 for more detailed explanations.

3.3.7.2 Insulation coordination

For all SKiiP series the isolation classification between heatsink and mains is basic isolation, because of the possibility of a dielectric breakdown through the DBC ceramic during a catastrophic electrical fault event. For SKiiP 3 and SKiiP 7 the isolation classification between low voltage circuit and mains and heatsink and mains is “basic isolation” too, because the isolation of the temperature signal is also a basic isolation only. During a catastrophic electrical fault event, plasma of an arc can apply high potential to the temperature sensor. Equipment which is designed for reinforced isolation here must have additional isolation for all parts which might be touched by a person. Because the temperature signal of the SKiiP 4 is transmitted digitally via a galvanic isolation to the low-voltage side of the gate driver, the isolation between low voltage circuit and mains here is classified as reinforced isolation.
Overviews of the insulation properties of the individual SKiiP series, according to EN 50178, IEC 61800-5-1 and UL 840 are also listed in the respective SKiiP IPM datasheets. More detailed

information on structural dimensioning, isolation limits and also the required voltage reduction for greater installation altitudes can be found in chapter 10.3.

3.3.7.3 Reliability

Overviews of tests for qualification and re-qualification according to the applicable parts the standards IEC 60068 "Environmental testing" and IEC 60747 "Semiconductor devices", are listed in the technical explanation of the respective SKiiP IPM series.
Also the test volumes regarding Electromagnetic compatibility - according to the applicable parts the standard EN 61000 "Electromagnetic compatibility/ immunity tests" are listed there.

3.3.8 Specifics of parallel connections for SKiiP IPM modules

3.3.8.1 General requirements

With regard to symmetry, cooling conditions and derating, the general statements made in chapter 9.3.1, especially the explanations on the "individual driver concept" likewise apply to the parallel connection of SKiiP IPM modules. Basically, a properly functioning parallel connection of SKiiP requires the following considerations and features:

- synchronous setting of the switching signals including external propagation times
- Common error management for all paralleled SKiiP
- separate monitoring of the analogue sensor signals for current and temperature
- common auxiliary power supply for all paralleled SKiiP

An output current imbalance caused by different output voltages of the paralleled SKiiP which could be a consequence of:

Different transmission times of gate drivers (jitter)

Dead times cause a phase shift of the modulated output voltages, proportional to dead time and output frequency

Different turn-on delay times of the SKiiP-IGBT

Different turn-on delays cause phase shift and voltage differences. The phase shift is proportional to the delay time and the output frequency. The voltage difference is proportional to switching frequency.
Tolerances of IGBT and freewheeling diodes forward voltage drops and its temperature dependencies
The IGBT used in the SKiiP have a positive temperature coefficient, limiting an inhomogeneous current distribution. The freewheeling diodes have a positive temperature coefficient, but they are produced with a small forward voltage tolerance range.

Different DC link voltage levels

Different DC link voltage levels are a result of different power circuit impedances. To avoid different output voltages caused by different DC link voltages levels, the DC link should be connected in parallel. Furthermore, oscillations between such interconnected capacitor banks must not occur. For large systems fuses between the capacitor banks are recommended. The paralleled systems should have the same DC link with the same capacitor type and capacitor values.

Different cooling conditions of paralleled halfbridges

The cooling system of the paralleled SKiiP units should be designed in way to avoid thermal stacking. To minimize the impacts of the above-mentioned effects the system designer has to make sure, that there is sufficient inductance between the AC output terminals of the paralleled SKiiP IPM.
This has the tasks of

- Prevention from the generation of an imbalance current during the switching moment as shown in Figure 3.3.16. That could lead to different switching loss and in severe cases to undesired oscillations. The value t_{jitter} is given in the SKiiP datasheets.
- Avoidance of a different RMS value of the output current. Existing current asymmetry can be reduced using an AC choke and their ohmic shares (choke and cable resistance). Low-frequency applications (< 5Hz) are particularly difficult, however, since the inductive share is ineffective in practice.

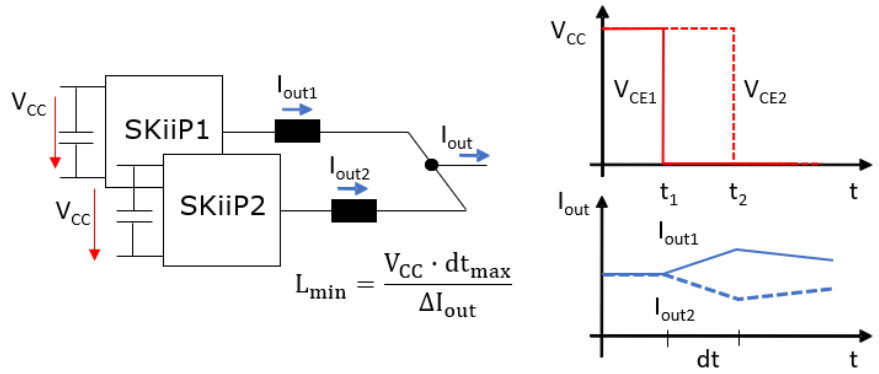


Figure 3.3.16 Dynamic decoupling of parallel SKiiP IPM modules using inductances in the load terminal paths

Differences in the RMS currents are caused mainly by the branch impedance in the converter phases. For identical output voltage (voltage-time area), the currents are distributed in inverse proportion to the branch impedance (Figure 3.3.17).

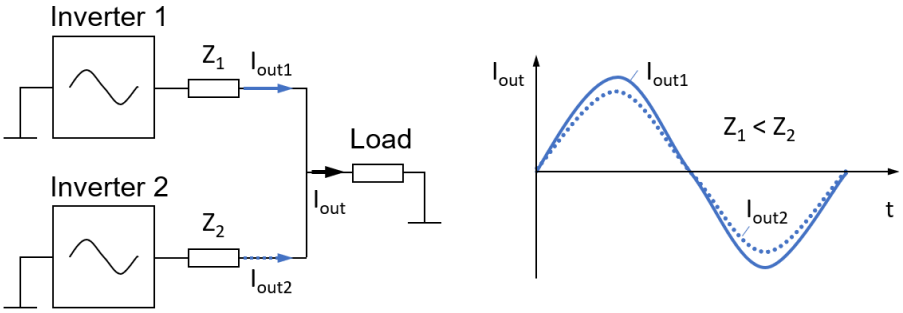


Figure 3.3.17 Abstract single-phase circuit diagram of 2 parallel converter phases as a voltage source with branch impedance Z_1/Z_2 and current asymmetry caused

For a typical SKiiP IGBT on-state resistance of 1mΩ, 100µΩ difference in branch impedance means 10% current displacement. As soon as one of the two parallel SKiiP-IGBT turns on, the DC link voltage will be applied over the parallel connection for the interval (t_1-t_2) until the other SKiiP IGBT has switched, too. The external inductance prevents commutation of the entire output current I_{out} to the "slower" SKiiP, as well as oscillations between the SKiiP. As regards driver signal jitter, one can assume that for one period of output frequency, the switching occasions are evenly distributed. This means there is no need to be concerned about any influence on the RMS output current, at least over the long term. Loop currents are caused by permanently displaced driver signals or semiconductor switching times (phase shift of fundamental frequency of output voltages). Once again, limiting is achieved by way of the inductance. To limit the current divergence, for example to 50A for a maximum SKiiP 3 jitter time of 125ns and a DC link voltage of 1200V, the following inductance would be needed:

$$2 \cdot L_{min} = \frac{1200V \cdot 125ns}{50A} = 3\mu H$$

In other words, approx. 1.5µH per SKiiP. In spite of all the mentioned actions it has to be taken into account that for remaining imbalanced current sharing a derating of the nominal current of the power stage has to be considered. In case of paralleling SKiiP 4 IPM, the use of parallel mode (common error management, e.g. using the HALT signal) is necessary.

3.3.8.2 SKiiP Parallel Boards

Synchronous switching using one common gate signal cannot be guaranteed owing to the different driver signal propagation times inside each individual SKiiP. To be able to implement parallel connections, some conditions must be met by special measures between customer's controller and SKiiP.
With reference to the explanations of the SKiiP-specific gate drivers in chapter 3.3, SKiiP Parallel Boards by Semikron Danfoss for up to four parallel connected SKiiP perform the following functions:

- synchronous setting of the controlling signals including external locking time, where required controlled delay of switching commands as active current balancing measure
- separate monitoring of the sensor signals for current and temperature as well as other error messages
- common error management for all connected SKiiP with a common error message,
- common auxiliary current supply for all connected SKiiP.

Detailed descriptions of the boards are included in [3.25] and [3.26].

3.4 Discrete power semiconductors

3.4.1 Preface

Discrete power semiconductor devices have been widely displaced by isolated power modules. However, they are still important, e.g., for power assemblies of low or very high power, and on the other hand due to advantages in manufacturing costs, cooling effort or even load cycling stability. The metal and ceramic hermetically sealed housing of screw and disc type devices ensures protection against influences from their environment.

3.4.2 Axial diodes

Especially in the lower power range, discrete power semiconductors are available in a variety of package designs and cases, e.g., MINIMELF, MELF, SMA (DO-214AA), SMB (DO-214AB) ...SMC (DO-214AC), GF1 (DO-214-BA), D²Pak and SO-DIL for surface mounting or axial diodes, SIL, DIL and various TO cases as wired components for PCB mounting.
In the following, however, only the axial diode and axial high-voltage rectifier types will be described, as only these are included in the Semikron Danfoss production programme. Axial diodes mostly have a plastic case and solderable metal wires (leads) in axial direction for mounting into a PCB. The semiconductor chip is connected to the terminals by soldering on both sides. Axial diodes are mounted by inserting the connecting wires through metallised holes in the PCB and soldering them to the traces (Figure 3.4.1).

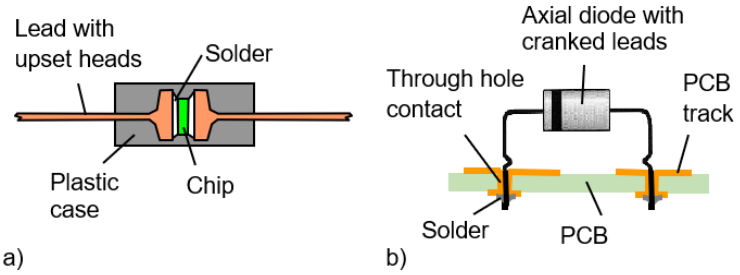


Figure 3.4.1 Axial (lead) diode: a) Cross-section; b) Mounting example on a PCB

Semikron Danfoss produces axial (lead) diodes with maximum mean forward currents of 1A, 3A and 6A with reverse voltages up to 1600V and as avalanche diodes with breakdown voltages up to 2000V. Semikron Danfoss also manufactures high-voltage rectifiers with axial screw terminal in two sizes (Figure 3.4.2).

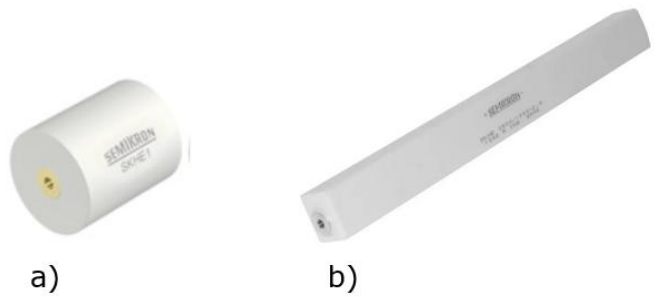


Figure 3.4.2 High voltage rectifiers: a) V_{RRM} = 4800V, I_{FAV} = 1,25A; b) V_{RRM} = 8000V, I_{FAV} = 2,1A

These rectifiers consist of a series connection of avalanche diode chips in an epoxy case and are specified for use in cooling oil.

3.4.3 Stud screw diodes and thyristors

Stud Screw packages were the first housings for rectifier diodes and thyristors on the market. Although produced by only a few manufacturers and in relatively small quantities, they are mainly used as spare parts, but also for systems in which forced air cooling or liquid cooling is not possible.
The design of stud screw diodes or thyristors is characterised by a solid copper hexagon with threaded stud that is used to screw the component onto a heatsink and discharge the heat generated at the chip. A glass or ceramic cap with a bushing for the cathode terminal ensures hermetical case sealing. Case parts are joined by welding or brazing. The chip is directly soldered onto the copper, or a disk made of molybdenum (thermal expansion coefficient $5 \cdot 10^{-6}$/K) is soldered between the silicon and copper to prevent high mechanical tension in the semiconductor as a result of significant differences in the expansion coefficients for silicon ($4.1 \cdot 10^{-6}$/K) and copper ($17.5 \cdot 10^{-6}$/K).

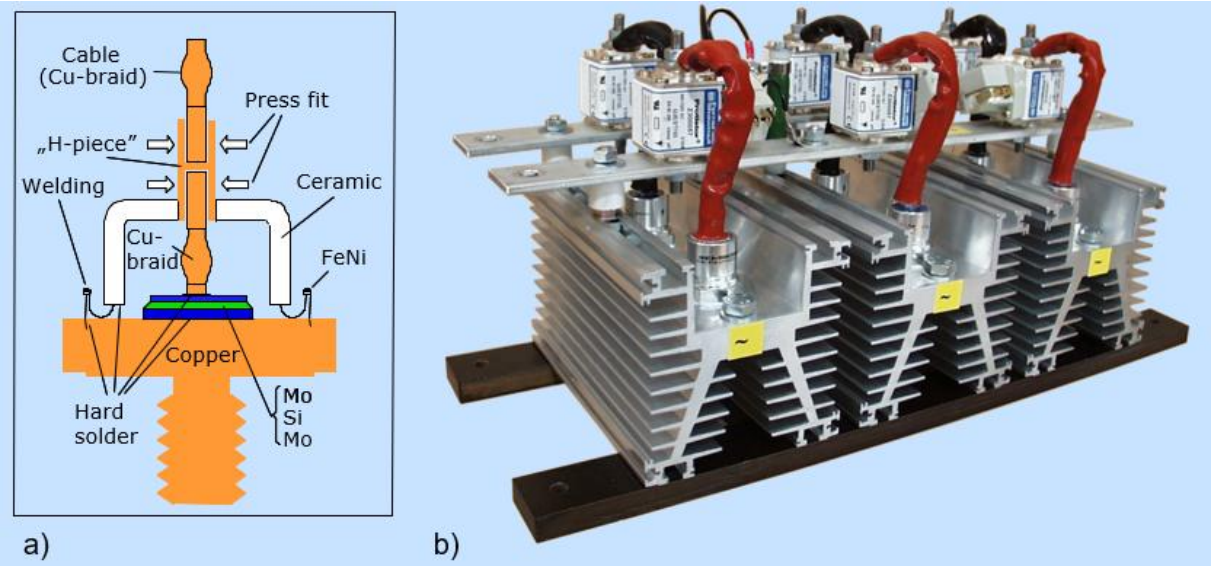


Figure 3.4.3 Stud screw diodes: a) cross-section of a stud screw diode; b) Application of stud screw diodes in a natural aircooled SEMISTACK B6U

Stud screw diodes and thyristors are very reliable and robust, last not least due to their hermetically sealed cases. Thanks to the close thermal coupling of the active component with a solid copper part, transient and thermal resistances are very low. The disadvantage is that the heatsink is not insulated but connected to the anode potential (SKN types) or cathode potential (SKR types).

3.4.4 Disk type diodes and thyristors

The power range of disk type (or capsule) diodes or thyristors extends well beyond the power range of isolated diode/thyristor modules because of the two-sided cooling capability and the outstanding thermal behaviour due to the absence of the insulating layer between chip and heatsink. Mainly for system cost reasons Disc type cells are used today mainly for high power applications (several 100A up to several kA).
When two-sided cooling is applied, the thermal resistance is about half as high as that of the same silicon chip size in a screw-mounted case. For two-sided cooling, however, two heatsinks and a clamping device are required. The voltage range extends from a few 100V (disk type diodes for welding applications) to a reverse blocking voltage of more than 10kV.
Added to this is the advantage of absolute hermetic tightness, which enables their operation in particularly critical atmospheres or in non-conductive liquids. Disk type cells are pressure-contacted components, meaning that the semiconductor is not connected to the connection parts by metallurgical joining but by means of pressure. Pressure contacts are extremely reliable and durable parts, since there are no solder layers that might show fatigue during frequent temperature cycling.
If a disk type diode or thyristor failed due to surge current, the chip surface melted and alloyed with the massive metal plates. The semiconductor chip loses its blocking capability and get short with increasing failure current. In contrast to soldered modules, disc type cells therefore remain shorted safely after such an event.

The diode or thyristor chip is often joined with a molybdenum disk by means of aluminium alloying or sintering, but layouts also exist where the semiconductor chip floats freely between two molybdenum disks. The case ring is made of ceramics or epoxy.

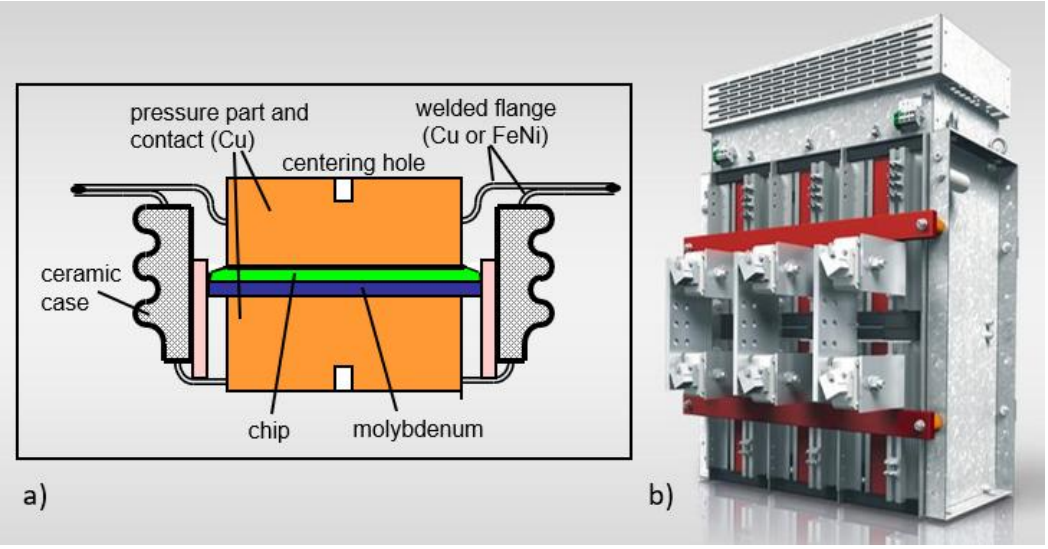


Figure 3.4.4 Disc type power semiconductors: a) Cross-section of a pressure contacted disk type diode; b) Application of disc type thyristors in a forced aircooled SEMISTACK B6C

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[3.25] A. Schiller, "Technical Explanations SKiiP 3 Parallel Board" rev. 02, Nuremberg, Semikron Danfoss 2017
[3.26] A. Schiller, "Technical Explanations SKiiP 4 Parallel Board" rev. 03, Nuremberg, Semikron Danfoss 2017
[3.27] IEC 61800-5-1, "Adjustable speed electrical power drive systems - Part 5-1: Safety requirements - Electrical, thermal and energy", ed. 2022

4 Reliability

4.1 General

Reliability, i.e. maintaining the characteristics relevant to operation over a defined period of time, is one of the most important quality features of power modules. On the one hand, power modules are highly utilised electrically and thermally; on the other hand, premature failure may cause dangers, direct and consequential damage and, last but not least, high costs. Owing to the comparably small batch sizes, often extremely long service life requirements (10...30 years) and complex test specifications, reliability is very difficult to properly evaluate. Reliability statements are possible thanks to

- exact control of all influences on production processes
- testing under conditions very close to practical application in order to discover typical failure mechanisms
- testing the components within the system while monitoring the most important parameters

In the context of reliability, the term "Design for Reliability" is often heard [4.1.]; this ultimately means that when a power electronic assembly is designed, component (here the power semiconductor) aging is already factored in. Exactly so much safety must be considered that the maximum values of the components at the end of their forecast service life meet the minimum requirements for this assembly (Figure 4.1.1). To be able to do so, however, accurate data on the different manifestations of aging is needed [4.2.].

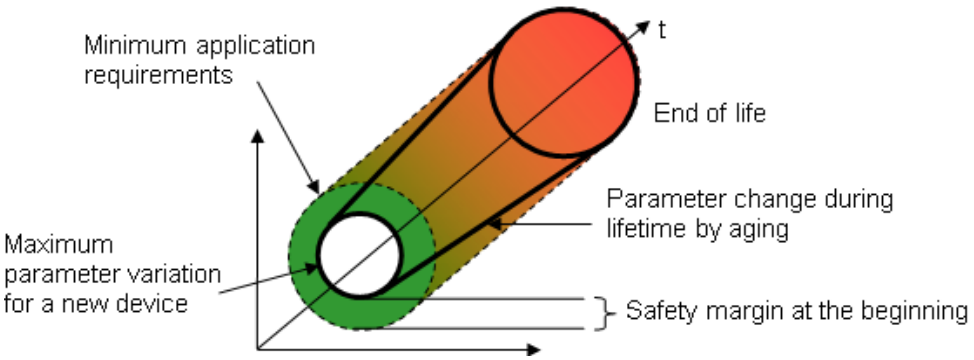


Figure 4.1.1 Design process for reliability

Characteristics in the data sheet describe the product at the moment of production respective of shipment. Because this status is measurable. It is in the responsibility of the inverter designer to add some margin to ensure a proper functionality to the end of the expected lifetime.
Some selected tests for power modules will be presented in the following chapter. Semikron Danfoss certified quality assurance system in compliance with ISO 9001 and IATF 16949 will not be discussed in detail here (details and actual status of certification see the homepage of Semikron Danfoss).

4.2 MTBF, MTTF and FIT rate

The FIT rate (Failure in time) refers to the number of times a component fails during one hour in operation. Normally, this value is standardised to 10^{-9}h. 50FIT means that of 1 million components in 1000hours of operation 50 will fail randomly.

$$\mathrm{FIT} = \frac{n_f}{N \cdot t}$$

n_f: number of failures; N: number of components in operation; t: monitoring period

Early failure and failure at the end of service life are not considered for analysis. The time interval with the initial decreasing failure rate can last from weeks to several month in power electronic. The FIT rate corresponds to the flat section of the "bathtub curve" with constant failure rate (ideal case) and a shape parameter of a Weibull distribution k = 1 (Figure 4.2.1). It is not possible to screen out all components which will suffer an early failure even not with a burn in. When the failure rate starts to rise again, then end of life is reached.

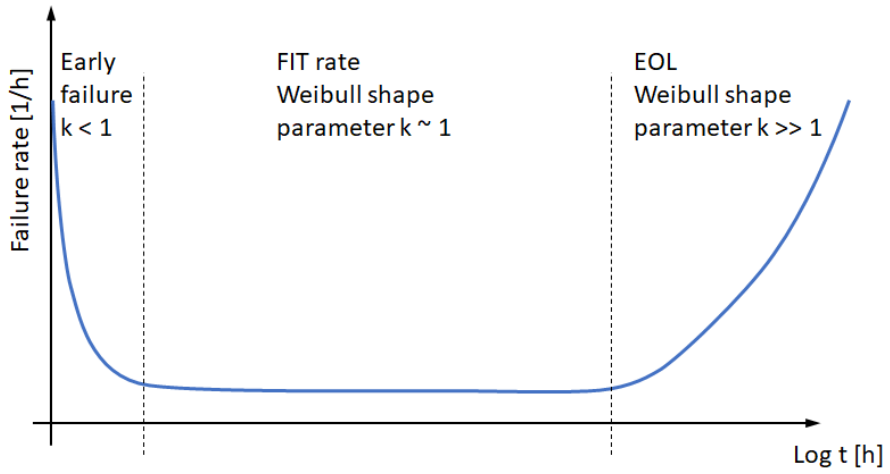


Figure 4.2.1 Bathtub curve

The MTBF value (Mean time between failure) refers to the mean expected time between two failures. The MTBF value is the reciprocal of the FIT rate.

$$\mathrm{MTBF} = \mathrm{MTTF} = \frac{1}{\mathrm{FIT}}$$

In the world of power semiconductors, it is generally better to specify the MTTF value (mean time to failure), since MTBF refers to the time between two repairs. As repair time is obsolete, both values are identical. In contrast to components for signal processing which are in duty a million times, there is only a weak data base for power semiconductors. Besides the significantly lower quantities in the field, information on operating hours and conditions is rarely available for returned products. A typical FIT rate of a standard power module is in the range of $50 \cdot 10^{-9}$ hours (SN 29500-3 specifies 70 FIT). This corresponds to an MTTF value of $2 \cdot 10^{7}$ h and applies mainly to modules with two functional switches like SEMITRANS 3 or modules with a more complex circuit but the same dimensions (similar chip area inside). Higher integrated and larger components also have a higher failure rate.
The Arrhenius effect is often mentioned in the context of FIT rates, which means that the failure rate increases exponentially over temperature. This statement is only partly true, since it only considers temperature-dependent failure mechanisms. Accelerated service life tests assume that a process which is triggered by an activation energy is exponentially dependent on the temperature according to the Arrhenius equation. An application relevant test would last years because this is the expected lifetime. This aging process needs to be accelerated by increased T_j during testing and the results are then transferred to "normal" operating conditions.

$$N = A \cdot e^{\frac{-E_A}{k_B \cdot T}}$$

E_A: activation energy, k_B: Boltzmann constant, T: absolute temperature

If a failure rate N for a temperature-related failure mechanism is known, the characteristic for an entire temperature range can be calculated by adjusting factor A and the activation energy.

4.3 Failure mechanisms

4.3.1 Thermo-mechanical stress (power and temperature cycle)

Power cycling or temperature cycle failure are End of Life (EOL) failure. Power cycling happens, when a semiconductor chip inside a package is loaded by current and is heated up by the losses caused by the current flow. During the heating phase a temperature gradient arises inside the package. After switching off the current the chip cools down and the temperature gradient disappears. The up and down in combination with different thermal expansion coefficients (CTE) of the used materials stresses the interconnection between the materials and leads to a wear out of the semiconductor package. Figure 4.3.1 explains the structural details relevant to the wear out of an IGBT module.
Power cycle occurs in seconds, the shorter the time, the higher the temperature gradient. Aging happens close to the chip. Which failure mode (chip solder or bond wire) is triggered first depends on the temperature gradient and the duration of the cycle.

The further the connection is away from the chip, the longer it takes to heat it up completely. The worse the power semiconductor is cooled, the more all layers are raised to the temperature level of the chip. This gives a smooth transition to temperature cycling at which all layer of the thermal stack have the same temperature. One difference beside of the temperature gradient is also the time of one cycle. Temperature cycle takes place in several minutes up to an hour, so that all components have reached a constant temperature.

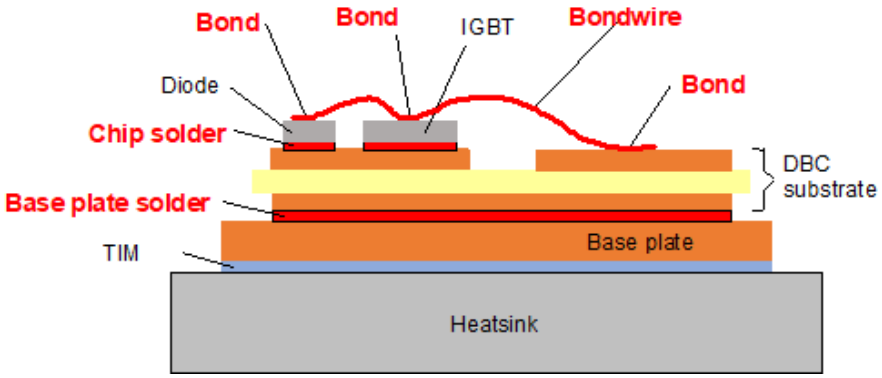


Figure 4.3.1 Structural details of an IGBT module (connections that are relevant to module lifetime are marked red)

Figure 4.3.2 shows the theoretical linear expansion for different layers with an edge length of 1 cm. The bars show the differences in true to scale (except bond wire). Huge differences in length are an indication of considerable stress. On the left, the temperature ratios of a typical application condition are assumed with T_C=80°C and T_j= 125°C. The temperature gradient in the module has the effect that the copper base plate will only extend to about three times the length of the chip despite its 5-fold CTE. The table also demonstrates that an AIN ceramic substrate is better adapted to silicon. In turn, the stress between AIN ceramics and copper base plate is increased so that this combination can be used with restrictions only, or not at all. AIN ceramics and AlSiC base plate constitute a better combination under the aspect of module service life. Al_2O_3 ceramics is in between the thermal expansion of Si and Cu and therefore makes an ideal partner layer for modules with a copper base plate. Bond wires are not connected via large-area joints. The linear expansion shown here (blue bars shorter scaled) results in wire bending. The comparably small bond foot, however, is subject to particular stress due to the great difference in the CTE of silicon chip and aluminium bond wire.

Material	CTE 10^{-6}/K	T [°C]	ΔT [K]	Δl Power Cycling	T [°C]	ΔT [K]	Δl Temperature Cycling
Chip (IGBT) Si	3.5	125	100	3.5µm	125	100	3.5µm
AIN – DBC	8.2	105	80	6.6µm	125	100	8.2µm
Al_2O_3 – DBC	10.7	105	80	8.6µm	125	100	10.7µm
AlSiC base plate	7	80	55	3.8µm	125	100	7µm
Cu base plate	17	80	55	9.4µm	125	100	17µm
Bond wire Al	23	100	75	17.2µm	125	100	23µm

Figure 4.3.2 Linear expansion of different material layers in a power semiconductor module with an edge length of 1cm by heating from T_j=25°C to T_j=125°. left: temperature gradient as for a typical power cycle; right: entire module with identical ΔT as for temperature cycling

Figure 4.3.1 and Figure 4.3.2 show that the solder connection of the substrate to the copper base plate is the most critical connection for longer cycles with a low temperature gradient in the module. First it covers by far the biggest area, second it has the highest mismatch in the CTE and finally it is the outer connection in the cooling path. It is therefore useful for an increase of the power cycling capability to make improvements to the most exterior source of failure (= closest to the heat sink). A damage here will increase the ΔT_j of all connections located above in the thermal path and cause them to age faster and finally to fail as well. For this reason, high-quality solders and sophisticated soldering procedures have to be applied in order to avoid deformation and fatigue also in case of high temperature cycling amplitudes. The development of modules without

base plate eliminated "base plate solder" as the source of failure in the Nineties. The introduction of sinter technology to replace chip solder pushes the failure limit for this type of connection further up and makes the bonded connections the weakest link in the chain. The improvements of bonded connections introduced in recent years now result in significantly higher power cycling figures than technically feasible 20 years ago.
Furthermore shows Figure 4.3.2 that the temperature gradient with active heating (power cycle) compensates partly the different CTE. Therefor much higher cycle numbers can be achieved with active heating compared to passive heating (temperature cycle).

4.3.1.1 Solder fatigue on the base plate

Large-area soldering of a module base plate is stressed in particular in slow processes and intense heating up. At first, the solder connection will start cracking at the corners. As a result, the thermal resistance of the module will increase. This may cause chip overheating and speed up other failure mechanisms so far that they will then produce a failure. The quality of base plate soldering is safeguarded by temperature cycling tests.

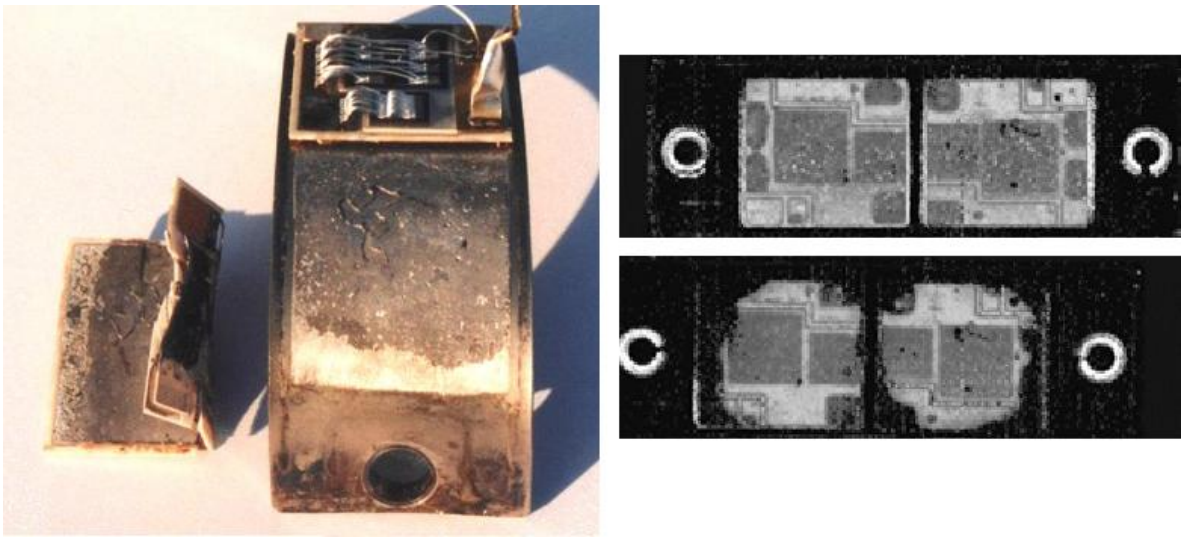


Figure 4.3.3 Baseplate of a 34mm module with torn off DBC (left: light-coloured areas show solder fatigue) and Ultrasonic image before (right upper) and after temperature cycling (right lower)

4.3.1.2 Solder fatigue in chip soldering

Solder fatigue on chips mostly appears together with damage of the bond wires. The more the whole module heats up, the more the solder connection is strained. Solder fatigue leads to an increase in R_{th} and the chip temperature, which in turn will cause higher losses and thus a higher temperature difference ΔT in the IGBT. In the end, the aging process is accelerated.

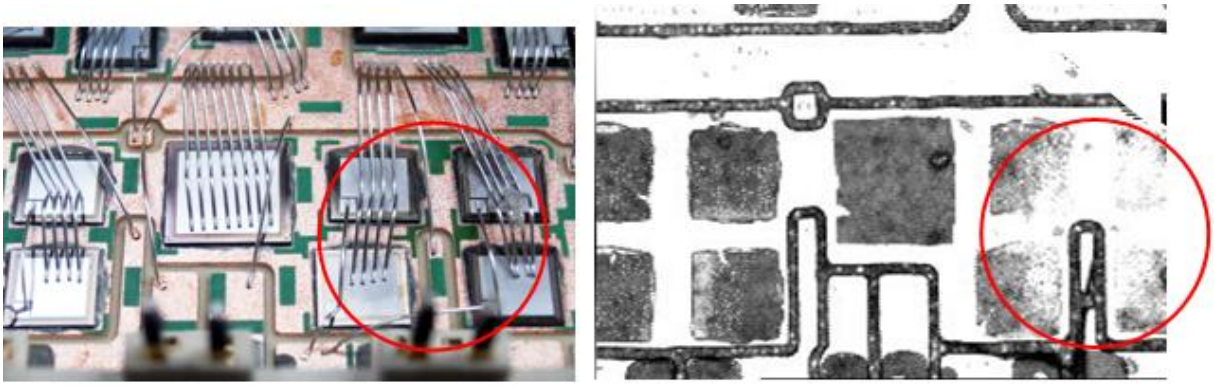


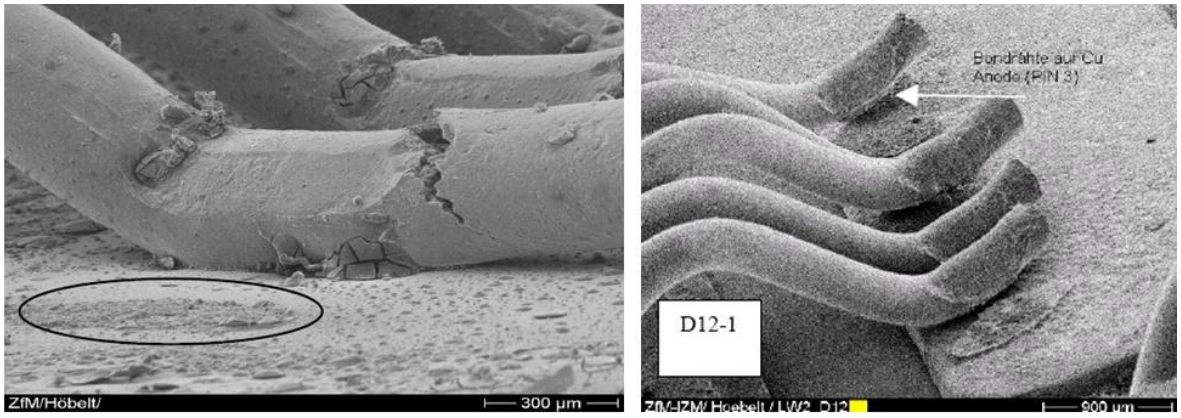
Figure 4.3.4 Chip solder fatigue caused by power cycling test: a) photograph; b) ultrasound image

The four IGBT chips (Figure 4.3.4) on the right of the DBC substrate underwent power cycling, the other IGBT chips and CAL diode chips on the left did not. In the ultrasound image (SAM = Scanning Acoustic Microscope), delamination after power cycling can be seen. The four parallel, jointly

current-carrying IGBT have their hottest spot in the centre. It can be clearly seen that delamination starts right there at the inner corners. For larger chips, the temperature gradient over the chip area might result in damage at the centre where the temperature ΔT is highest, rather than at the edges, as is usually the case [4.3.]. This effect will become more and more important in the future with an increase of the permissible chip temperature (e.g. to 175°C) and the resulting higher power density. The quality of the chip soldering is verified by a power cycle test.

4.3.1.3 Bond wire lift-off or cracks

In comparison with copper and silicon, aluminium has a relatively high thermal expansion coefficient. This damages the welded connection of the bond feet ("lift-off") and, due to changes in the length of the bond wires, even the kink at the bond foot becomes damaged ("heel crack"). Further movement is caused by temperature-related bending of the module base plates and in addition to thermal movement also by mechanical stress (e.g. owing to high current surges). The soft moulding with silicone applied in the power modules will absorb these mechanical vibrations. Since power modules with rated currents > 10A per chip have more than one bond wire positioned in parallel, a loss of bond wire contact will not immediately result in component failure. Contact losses will become noticeable by an increase of the forward voltage in the power cycling test. Those parallel, not yet fully destroyed bond wires must now carry additional current, the bond feet will be heated up even more. Thus, their aging process is further accelerated. In the last bond wire left, the current density will then be so high that the metallisation will start melting, an internal arc will occur and eventually the chip will be destroyed. A pure circuit interruption ("open terminals"), however, is very rare in practice.



a) b)

Figure 4.3.5 Bond wire damage: a) Breakage and lift-off at the marked area; b) Failure due to bond wire lift-off [4.4.]

The main weak points of bond connections are the aluminium bond wire area right above the ultrasonic bonds, whose crystalline structure is impaired by bonding. Thanks to new wire alloys, improved bonding tools and optimised control of the bond processes parameter, the bond lifetime could be doubled in recent years. For example, it was in [4.5.] proven that a correlation between the angle of inclination of the bond wire and the maximum number of possible power cycles exists. A larger angle respective a higher aspect ratio (loop height to width ratio) leads to an increased cycle number.
The failure probability can be reduced by factors with the usage of copper or at least aluminium cladded copper bond wires. "Bond wire failure" can be eliminated as cause of failure by using double-sided pressure contact, as is found in disk cells, for example. The quality of bond wire connections is tested with the power cycle test too.

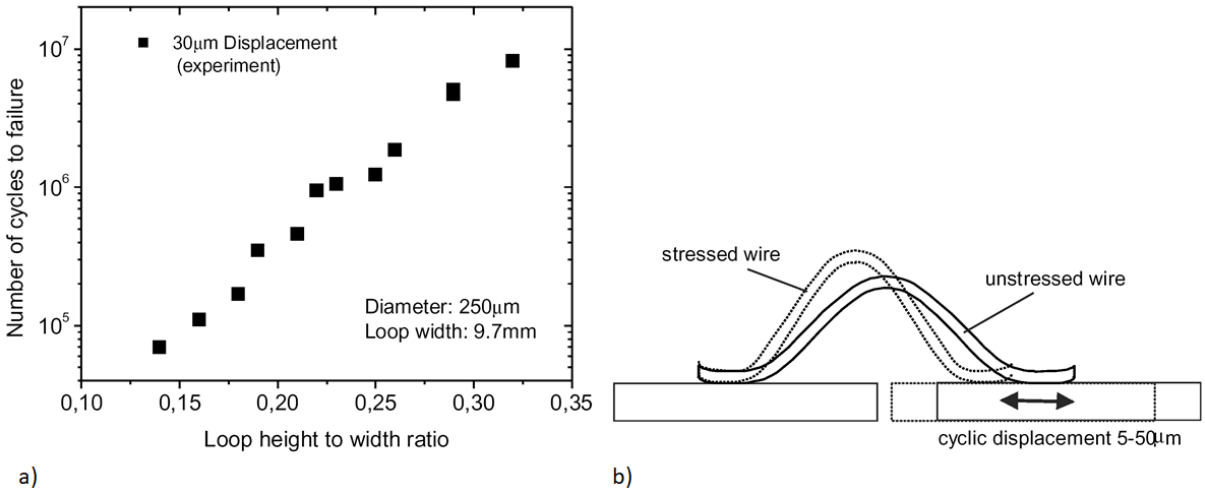


Figure 4.3.6 Function of aspect ratio in relation to power cycling capability [4.5.]

4.3.1.4 Reconstruction of chip metallisation

This is another aging process that is induced by power cycling. This process is accelerated by high current amplitudes. Changes in the chip metallisation gradually increase the chip resistance causing additional losses, higher ΔT and a worse adherence of the bond wires, this accelerates the ageing process. Limiting the repetitive current load (I_{CRM}) is therefore necessary.

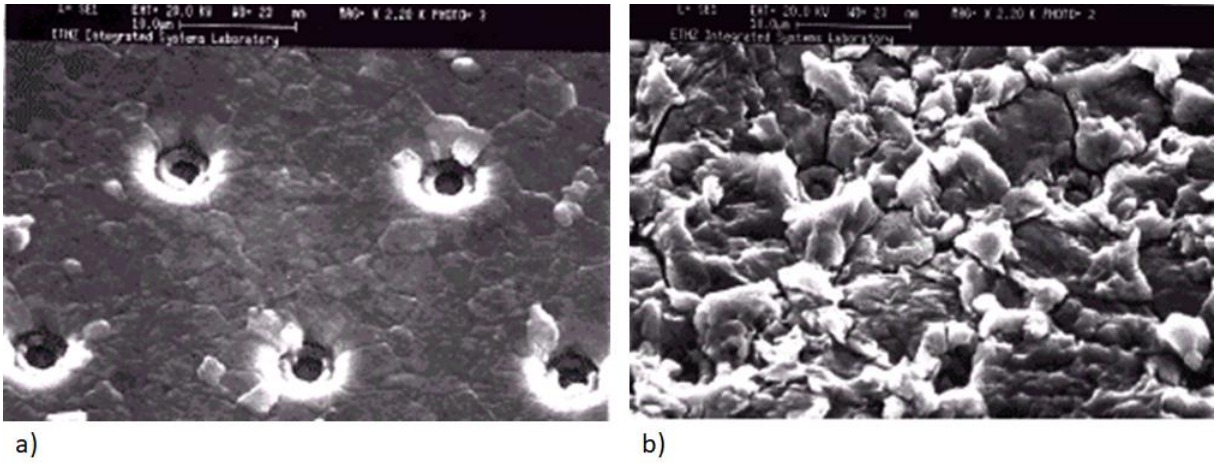


Figure 4.3.7 Reconstruction of chip metallisation, a) before and b) after power cycling [4.6.]

4.3.1.5 Modelling of the aging effects in power cycles

Models are used to predict the lifetime of a power module under thermomechanical stress in a real application. The stress caused fatigue of a single temperature cycle is calculated and count it up for a number of mission profiles. So, there might be the case that not $T_{j(max)}$ or the semiconductor current rating determines the size of the module but the required number of power cycles to achieve a certain product lifetime. The models and the coefficients for calibration are derived from accelerated power cycle tests (see 4.4.9).
The most popular model in the past from the late 90th was published by the LESIT study [4.7.] and introduced additional to the junction temperature swing a dependency of the cycle number from the medium junction temperature. The medium temperature is used as an absolute value in Kelvin. It is not the average temperature over time.

$$N_f = A \cdot \Delta T_j^{\alpha} \cdot e^{\left(\frac{E_a}{k_B \cdot T_{jm}}\right)}$$

with $\quad T_{jm} = \frac{T_{j(max)} + T_{j(min)}}{2}$

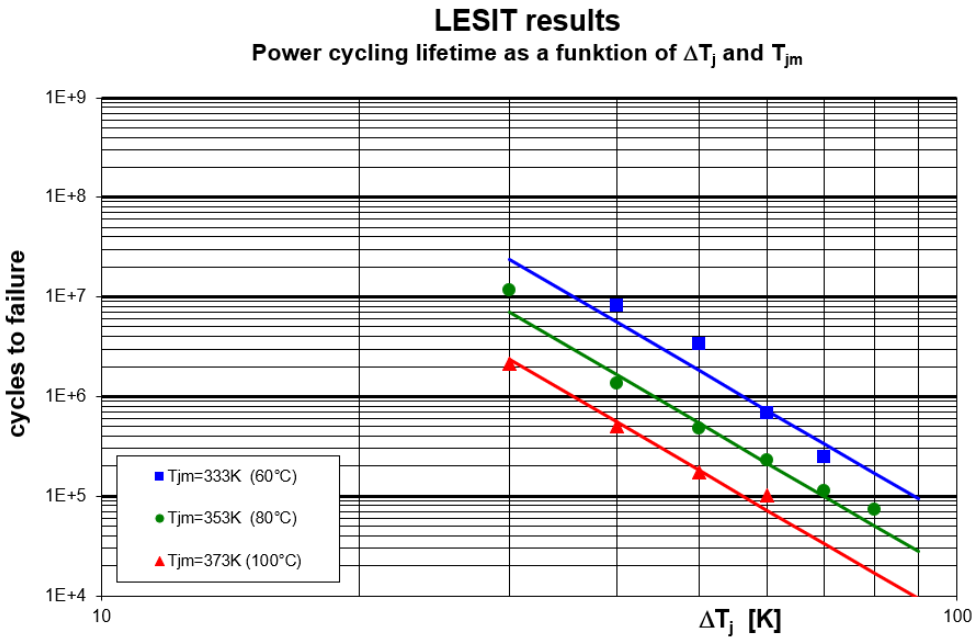


Figure 4.3.8 Power cycling curves for power modules in dependency of different mean temperatures from LESIT Study [4.7.], A=3.025·10^5, α=-5.039, E_a=9.891·10^{-20}J, k_B: Boltzmann constant

In the meanwhile, a lot of investigations and publications provide a much better understanding of influencing parameters and interaction of different operating conditions. In 2008 a model was published at the CIPS conference [4.8.], which considered additional parameters like current density, pulse duration, voltage class (→ chip thickness) and bond wire diameter.
At the PCIM conference in 2013 [4.9.] and ESREF conference 2017 [4.10.] results of a test series have been published which allowed to separate failure modes for solder fatigue and bond wire lift-off/heel crack. This is important for the improvement of power modules and is the base for the SKiM63-Model used for backside sintered chips and front side contact with bond wire. Furthermore, the model provides a function of time dependency for a much wider range of on-times used here as well.
The models presented here are valid for Semikron Danfoss product lines used mainly for transistors (IGBT, MOSFET) with bond wire connection on the top-side and solder or sinter connection on the backside of the chips. The data base for the model comprises more than 1000 test for following components and conditions:

- Voltage classes from 600V to 1700V
- IGBT, CAL-Diode, rectifier and SiC devices like MOSFET or Schottky diodes
- Chip thickness from 70µm to 310µm
- ton times from 1s to 28s in DC-test and 0.04s to 0.4s in Inverter test (AC with switching losses)
- ΔT_j from 50K to 120K (DC-Test) and 30K to 63K (Inverter test)
- Medium temperature between T_{jm} = 333K … 400K (60°C … 127°C)

The model equations use terms of long-time established power cycle models like Arrhenius Term and Coffin-Manson Law as well as the time dependency and the chip thickness [4.9.], [4.10.]. The formula is extended by two terms with an exponent β which results in an additional increase of N_f at low ΔT_j [4.11.].

$$N_f = A_0 \cdot {A_1}^{\beta} \cdot {\Delta T_j}^{-\beta} \cdot {\Delta T_j}^{\alpha} \cdot e^{\left(\frac{E_a}{k_B \cdot T_{jm}}\right)} \cdot \frac{C + {t_{on}}^{\gamma}}{C + 2^{\gamma}} \cdot k_{thickness}$$

$$\text{with} \quad \beta = e^{\left(\frac{-(\Delta T_j - T_0)}{\lambda}\right)}$$

The model equation can be used for most types of Semikron Danfoss power modules with slightly adapted set of parameters (see Table 4.3.1 and Application note [4.12.]). Exceptions are modules with pressure contact, double side sintered chips or modules using Danfoss Bond Buffer and copper bonds.

Parameter	Baseplate modules	Baseplate-less modules	Baseplate-less modules	Explanation
	Soldered		Sintered	Backside die attach
	Aluminum bond wire			Topside contact
A_0	$2.90 \cdot 10^9$		$2.05 \cdot 10^{11}$	Technology coefficient
A_1	60			Factor of low ΔT extension
T_0 [K]	40		38	Initial temperature for low ΔT extension
λ [K]	17			Drop constant of low ΔT extension
α	-4.3			Coffin-Manson exponent
E_a [J]	$4.5 \cdot 10^{-20}$		$2.54 \cdot 10^{-20}$	Activation energy
k_B [J/K]	$1.38 \cdot 10^{-23}$			Boltzmann constant
C	1	0.38	1.44	Time coefficient
γ	-0.75	-0.7	-1.21	Time exponent
$k_{thickness}$	1 | 0.65 | 0.5 | 0.33			Chip thickness factor

Table 4.3.1 Parameter of power cycle model for different module technologies

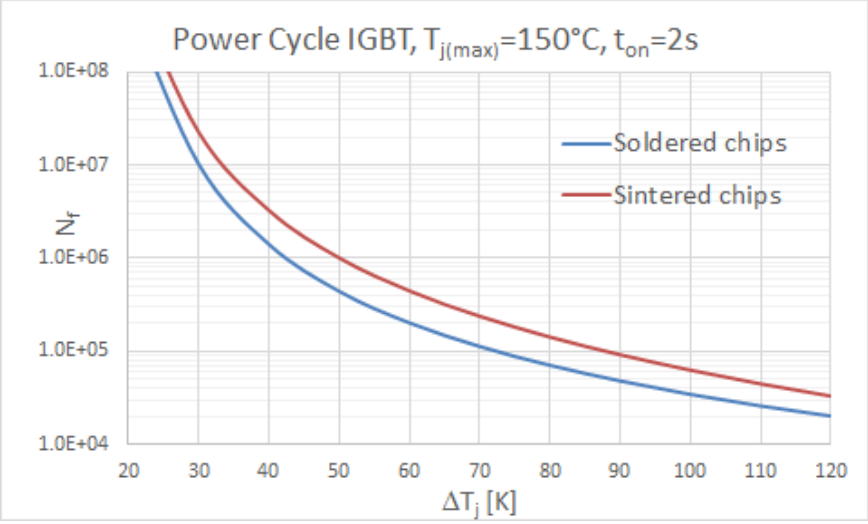


Figure 4.3.9 Power cycle numbers for IGBT modules with soldered or sintered chips

The power cycle capability of soldered and sintered IGBT chips is compared in Figure 4.3.9, at t_{on}=2s are the curves for modules with and without baseplate identical.

Time dependency t_{on}

The term in the model equation related to t_{on} in seconds was introduced in the SKiM 63 lifetime model [4.9.] for sintered and wire bonded power modules. It has been adapted to the test results here for other assembly technologies using the parameter C and γ. It is a time dependent scaling factor, normalized to a pulse duration (heating time) of t_{on}=2s. For modules with copper baseplate a different dependency was found compared to modules without baseplate, even though the front and back side chip contacts are the same. A reason might be the different temperature gradient inside the module in Y and X direction as well as a different micro-mechanical bending behavior depending on the construction of the power module (with or without baseplate). Furthermore, in modules without baseplate smaller chips are used while in baseplate modules typically larger chips are built-in.
Nevertheless, higher numbers of cycles are achievable in all cases for short cycles, while for longer durations the power cycling capability is lower. The function approaches a minimum value for times 30…60s and in [4.13.] it is mentioned that for time < 40ms no further increase of cycle numbers can be expected.
Fatigue of the baseplate solder is an additional failure mode for modules with baseplate. This ageing process is not the relevant failure mode in the tests considered here for the power cycle models, but can lead to a lower number of cycles, especially with long cycle durations.

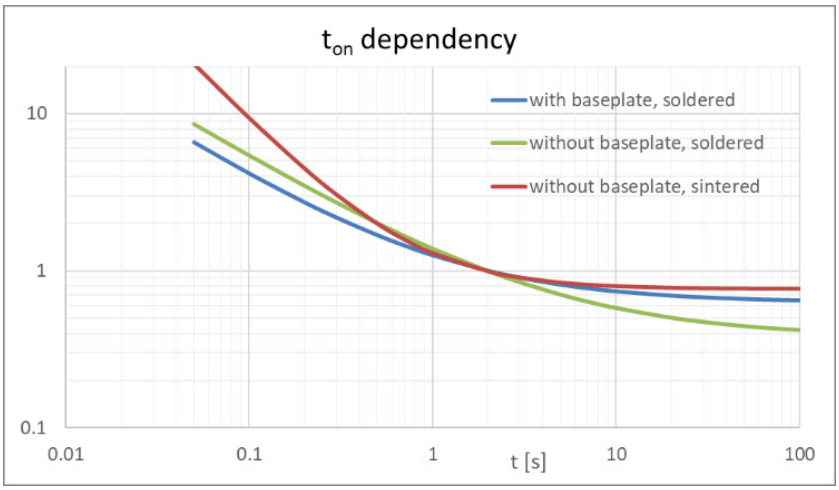


Figure 4.3.10 Time dependency of power cycle numbers for modules with and without baseplate

Dependency from medium temperature T_{jm}

The influence of the medium temperature is much lower as it was predicted in the LESIT study mentioned before. For example, if an IGBT is stressed by a temperature swing of ΔT_j = 60K in the application, it can withstand about 880k cycles (see Figure 4.3.11) at a lower turning point of $T_{j(min)}$ = 40°C (40°C↔100°C). On the other hand, the expected number of cycles is only about 260k at the same ΔT=60K but at an upper turning point of $T_{j(max)}$ = 150°C (90°C↔150°C). This is a factor of 3.4 compared to a factor of 10 by LESIT.

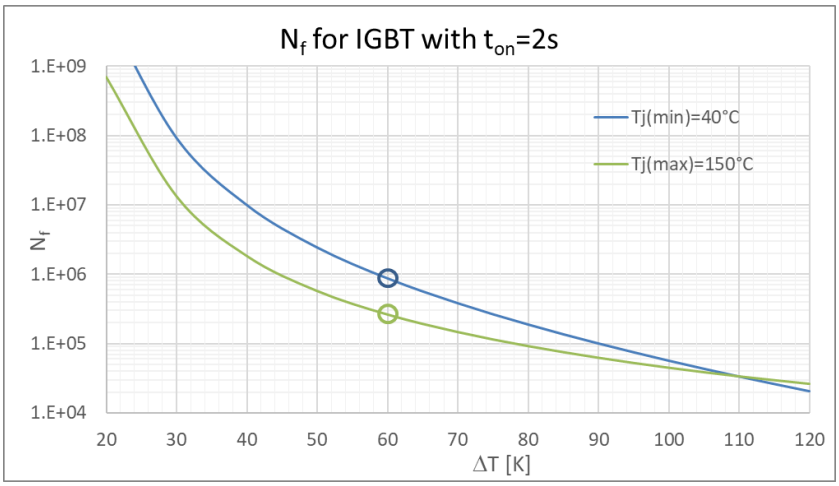


Figure 4.3.11 Power cycle number in dependency of medium temperature for soldered chips

Low ΔT_j behaviour described by exponent β

In several papers and studies the topic "What happens at low ΔT_j?" has been investigated [4.13.]. Depending on the test conditions and the triggered failure mode (solder fatigue) an increase of N_f was reported. Furthermore, there appears to be a discrepancy between the predicted numbers of formerly used PC models and the field experience of inverter operating for years at low frequencies and low ΔT_j for example at ΔT_j = 30K.
One problem is, that the models are derived from accelerated tests at ΔT_j = 70K and ΔT_j = 110K where plastic deformation dominates. They are applied to the low ΔT_j in the real applications where more and more elastic deformation takes place [4.14.].
An inverter tests have been performed with a back-to-back inverter to stress the IGBT on the inverter side and the diodes on the rectifier side to get some million cycles at low ΔT. The test results are set in relation to an expected value N_{f*} for the model without low ΔT_j effect in Figure 4.3.12. A clear increase towards low ΔT_j can be seen (factor >1). The parameters A_1, T_0 and λ used in combination with the exponent β were derived from the blue curve in Figure 4.3.12.
The root cause of failure in the inverter test was solder fatigue beginning at the chip centre. In [4.10.] was shown that the effect is related to the short cycle times. This is in contrast to high ΔT_j DC tests in which the solder fatigue starts in the corners and the edges of the chips.

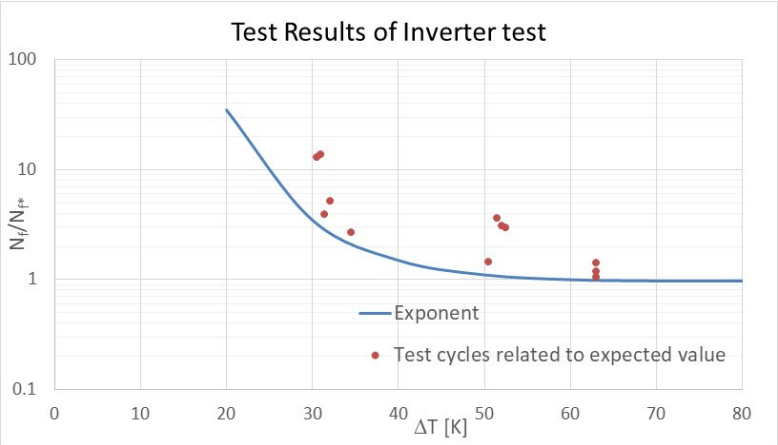


Figure 4.3.12 Inverter test results of IGBT and Diodes at low ΔT_j related to the expected value

Chip thickness

An influence of the chip thickness was observed too as it was indirectly introduced by the voltage class in [4.8.] (IGBT with higher voltage class are thicker than low voltage IGBT). Thicker chips are stiffer and generate higher stress on the interconnections and fail earlier.
The thickness of the different chip generations and supplier are not known to the user of the power modules. Furthermore, was there only a very small dependency observed between 650V and 1200V IGBT, much smaller than the standard deviation considering the total number test results under one test condition. Therefore, the thickness is clustered here to make the model more user friendly and is introduced in the model by constant factors. For SiC devices the factor represents not only the higher thickness which contributes to the higher stiffness but also different material properties like different CTE and compressive and tensile strength.

- Factor = 1 is used for IGBT with a blocking voltage <=1200V
- Factor = 0.65 is used for 1700V IGBT, CAL diodes
- Factor = 0.5 is used for rectifier (thyristor, mains diodes) inside the IGBT module housings
- Factor = 0.33 is used for SiC devices

4.3.2 Humidity

Water is part of ambient air and depending on the relative humidity, temperature changes, air pressure and the presence of cool surfaces (heatsink!) it can condense. A lot of background information and diagrams about critical conditions and measures against condensation can be found in [4.15.].
Most industrial power semiconductor modules consist of a plastic housing with openings containing chips which are covered only by silicone-based gel ("soft mould", "Sil-Gel"). The gel provides electrical insulation between conductors but is no protection against humidity. Even hard mould (resin) is not hermetically sealed (gas tight) but offers a better protection.
The soft mould also contains diffused air. Therefore, water molecules can also propagate through the soft mould in the same manner that they mix with air, albeit at a slower rate (e.g. 0.04mm/s @ 18°C, 1mm/s @ 100°C). Once inside the soft mould, the water molecules have the following effects:

- Reduced blocking voltage: When the heat sink temperature decreases, the diffused air inside the silicone holds less moisture. Water molecules will therefore accumulate on colder surfaces thermally coupled to the heat sink, such as the substrate, terminals and semiconductor surfaces. Furthermore, the water molecules are attracted to the charged semiconductor surfaces due to them dipole characteristic and align themselves in the electric field. This leads to disruption of electric field lines at the semiconductor edge termination that can lead to reduced blocking voltage.
- Semiconductor corrosion: The effect of corrosion on semiconductor chip passivation is well-known [4.16.]. With applied voltage and humidity, the chip edge passivation corrodes until breakdown occurs and the semiconductor fails (Figure 4.3.13). The semiconductor corrosion is a long-term aging effect that is investigated in power module reliability testing. The basic form of this testing is known as "High Humidity High Temperature Reverse Bias" (see 4.4.4 H³TRB) testing which is performed at 80V max. The high voltage test is known as "High Voltage High Humidity High Temperature Reverse Bias" (see 4.4.5 HV-H³TRB) testing.

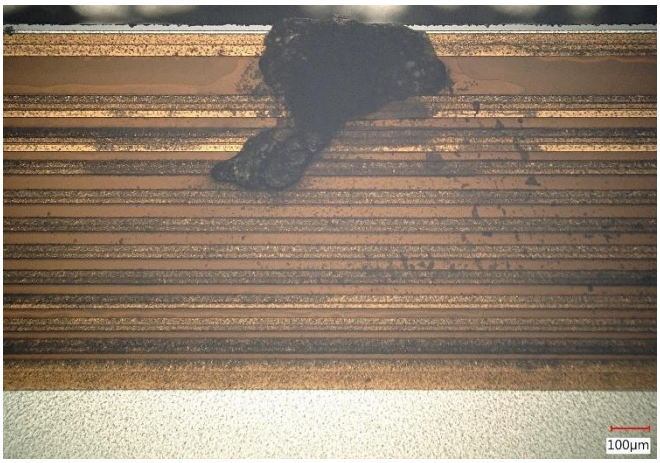


Figure 4.3.13 Flash over at the chip passivation caused by corrosion of guard rings

4.3.3 Mechanical forces or torques

Main sources for failure at the terminals with displacement and cracks are

- too high torque in the screw tightening process (electrical screwdriver instead of pneumatic)
- heavy cables which are not supported by stands or
- busbar systems where the holes are not in line with the module terminal screw holes

The terminals are supported inside of the modules against external forces by lugs for stress absorption, meander structures or by casting them into the housing material. Nevertheless, they are not designed to carry heavy load. A maximum force in any dimension is defined in the mounting instructions (example see Figure 4.3.14).

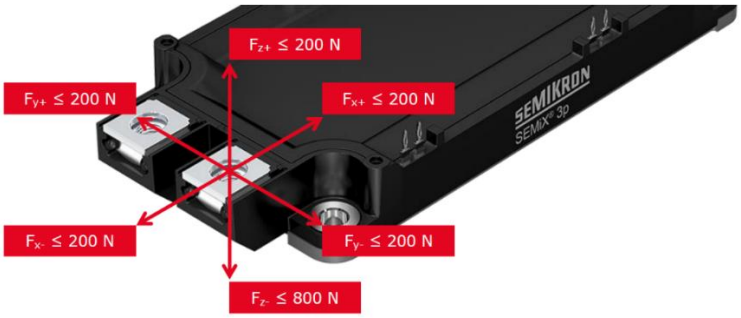


Figure 4.3.14 Example of maximum forces at the terminals of a SEMiX 3p

Another kind of failure are cracks in the ceramic caused by the forces during the mounting on a heatsink. Even a module with baseplate can crack if the module is mounted on a thick blob of a sticky thermal paste. The screws should be tightened by an electrical screwdriver with a low number of turns per minute and a soft torque limitation. Pneumatic screw drivers are not recommended due to torque overshoot at the end of the mounting process. Modules with four and more screws, the screws should be pre tightened to avoid a lift up of one module side and the final recommended torque is then applied crosswise.

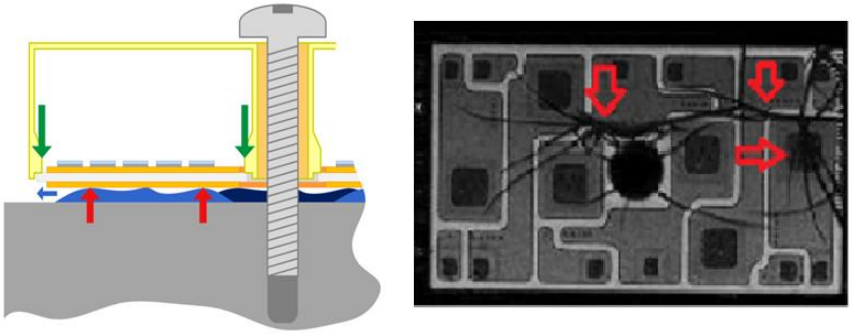


Figure 4.3.15 Too high mounting torque in combination with uneven distributed thermal paste can lead to ceramic cracks

4.3.4 Cosmic ray reliability

The useful life of a power electronic component is generally considered to be limited end-of-life failures like active power cycles or temperature cycles that a component experiences during its life. However, random failures must not be neglected when considering the reliability of a power electronic system. Single event burnouts (SEB) due to cosmic rays are a typical contribution to the random failure rate. While the single event is random, the probability of occurrence, that is, the failure rate of an inverter can be predicted from the application conditions of the inverter. This chapter focuses on the basic approach of how to estimate the cosmic ray failure rate of an application, whether under design or already existing. More details on the failure mechanism, related reliability testing and literature can be found in [4.17.].

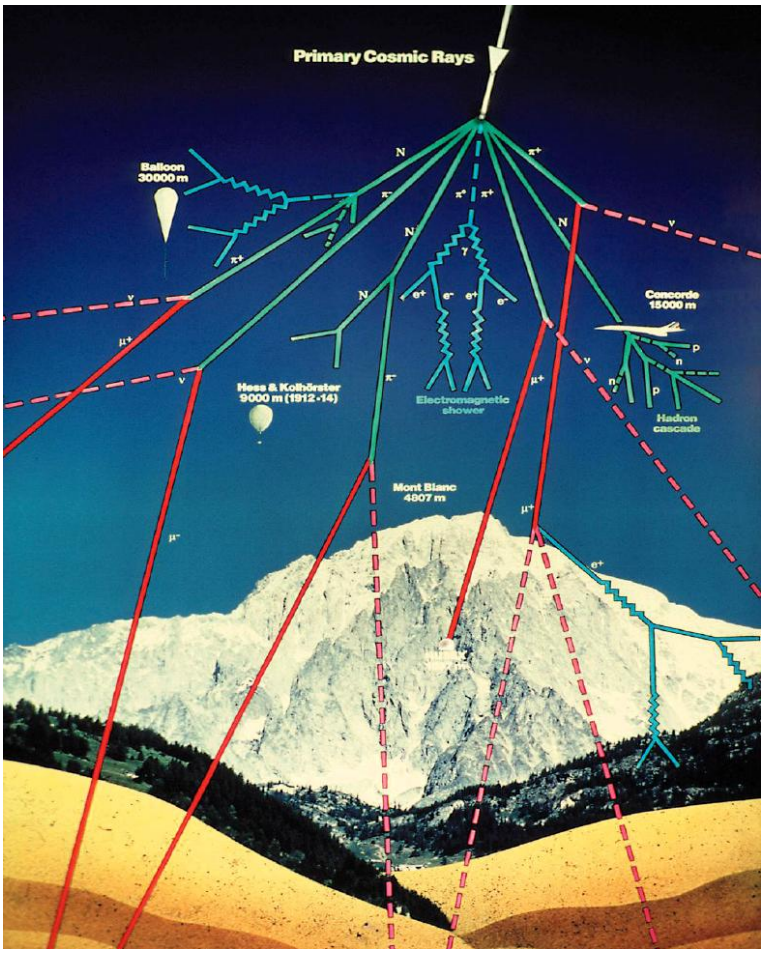


Figure 4.3.16 Diagram showing cosmic radiation [4.19.]

High-energy particles are ubiquitous in space. They constantly reach the earth from all directions. On their path towards the surface, they eventually collide with an atomic nucleus in the outer atmosphere. This collision creates a multitude of secondary particles that carry away the energy of the primary particle. Generally, these secondary particles have sufficient energy to create even more particles in subsequent collisions (Figure 4.3.16). Consequently, avalanche multiplication takes place while at the same time the particle intensity is reduced by absorption in the atmosphere. These two counteracting effects lead to a maximum of the intensity of the secondary neutrons (generally called "secondary", even if created in a multi-stage process) at roughly 10.000m to 15.000m above sea level. At lower elevations the intensity decreases. However, even at sea level, there is a relevant flux of neutrons of roughly 10n/(cm²·h) with an energy of 10MeV or more. A comprehensive account of the process can be found in [4.18.].
As secondary cosmic ray particles arrive at the earth's surface, they interact with the solid matter on the ground. For a power electronic device, this means there is a certain impact probability by in the blocking region. After the impact, the energy of the particle (typically several ten to several hundred MeV (100MeV ≈ 16pJ)) creates electron-hole pairs (that is, charge carriers) along a trace of some micrometres. An in-depth analysis of the spectrum and composition of the secondary cosmic radiation shows that neutrons are by far the most harmful component of cosmic radiation,

since they are the only ones present in sufficient numbers and at the same time capable of depositing all their energy in one single spot [4.20.].
In a device in conduction state, some extra charge carriers will do no harm; however, in the blocking state, a plasma of charge carriers in the field zone shields its interior from the electric field. The voltage drop will occur at pronounced field spikes at the edge of the plasma instead. These field spikes might exceed the critical field strength of the semiconductor and thus create more charge carriers via impact ionization, thereby extending the plasma. In this self-sustaining process, a so-called streamer develops which locally shorts the device. All this happens within less than one nanosecond. Afterwards, the charge carriers might diffuse away radially quickly enough such that the shorted region returns into its blocking state. However, if the diffusion process is too slow, sufficient energy is deposited in the device to melt the device locally and the device permanently loses its blocking capability. In an application, this leads to a permanently damaged chip and, in case of no sufficiently fast short circuit protection, to an explosion. In cosmic ray failure rate measurements, the devices are usually protected by a fuse and a molten channel through the semiconductor material can be found in a post-mortem analysis.
From this description, it is clear that the rate at which mortal hits happen is directly proportional to the area (more exactly volume, but this is in turn proportional to the area in vertical devices of given technology) over which a certain electric field extends: twice the area has twice the failure rate. Furthermore, it can be understood that cosmic ray failures only occur in the region of a chip where an intense electric field is present. This is not only the active area but can also be the edge termination [4.21.]. For simplicity, failure rates are thus usually specified per total chip area. This will introduce a certain (usually acceptable) inaccuracy, as failure rates for of the edge termination and the active area generally differ. We have not observed edge termination failures of Semikron Danfoss CAL diodes in any of our experiments. Yet, Semikron Danfoss generally adheres to the convention of specifying failure rates per total chip area.

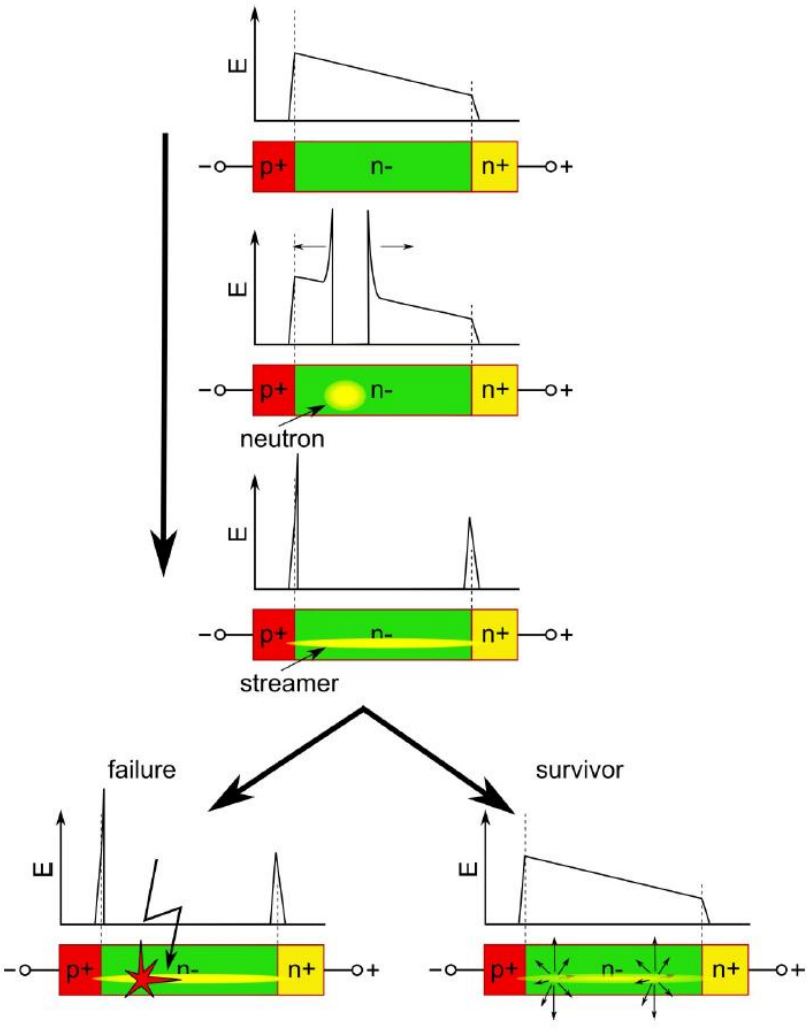


Figure 4.3.17 Microscopic mechanism of a cosmic ray impact and potential device failure

The failure process described above is influenced by the device design and by the application conditions. The likelihood for a cosmic ray failure is typically specified as a failure rate lambda(V) that depends on the blocking voltage V and is further modified by other application conditions. For one, the altitude above sea level determines the intensity of the natural flux. It roughly doubles for every kilometre elevation gain (valid up to ~4000m a.s.l.), therefore, the elevation dependence is given by the altitude factor A:

$$A = 2^{\mathrm{height}/1000\mathrm{m}}$$

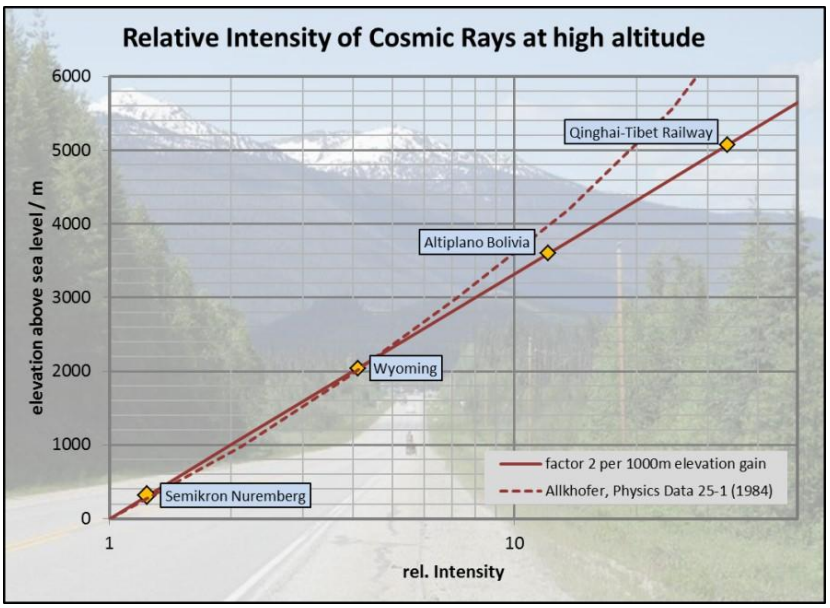


Figure 4.3.18 Elevation dependence of the cosmic ray intensity

In addition, the operation temperature of the device also has an influence on the cosmic ray ruggedness. Typically, it improves with increasing temperature, because the avalanche voltage of the device increases. As a first estimate, a formula published by ABB can be used [4.19.]:

$$F(T) = e^{-\frac{T_j - 25°C}{47.6°C}}$$

However, this is only a rough estimate and experimental measurements are required for each specific technology to obtain more accurate data.
In addition to the factors discussed above, there are several other parameters that the cosmic ray failure rate depends on to a lesser degree. One is the 11-year solar cycle: while the sun is not a source of harmful cosmic rays itself, the solar wind changes within this cycle. This influences the magnetic field of the earth, which in turn determines how well charged primary cosmic rays are deflected. The intensity varies countercyclically by about 20% from minimum to maximum within a solar cycle, that is to say, maximal solar activity corresponds to a minimum in the cosmic ray flux. For similar reasons, the intensity also depends on magnetic longitude and latitude of a location on earth. For example, the neutron flux in Tokyo (25°N geomagnetic latitude) is about 40% lower than the neutron flux in New York (52°N geomagnetic latitude); this is already close to maximal obtainable difference of about 50%. Finally, the shielding can also play an important role, in particular if the installations are typically found in basements of high-rise buildings, in mines, etc. For more details, refer to [4.18.]. Lastly, a common question asks about a diurnal cycle in the cosmic ray intensity and consequently the failure rate. As mentioned above, the sun is not the source of the primary cosmic rays which generate high energy neutrons, therefore such a cycle does not exist. However, these dependencies are often neglected, as the calculation of cosmic ray failure rates is usually only an order-of-magnitude estimate and a clear definition of these condition in the mission profile of the application is lacking.

4.4 Standard reliability tests for product qualification

4.4.1 General

The objectives of reliability tests are:

- ensuring general product quality and reliability
- establishing the limits of systems by exposing them to various test conditions
- ensuring process stability and reproducibility of production processes
- evaluating the impact of product and process changes on reliability

The following tests are minimum requirements for the product release of industrial power modules. They are being executed for release and re-qualification of new and/or re-developed modules. The scope of testing might be extended by further product-specific reliability tests. These tests are destructive type tests made on a number of production samples.

	IGBT, CAL Diode, MOSFET Products (Si based)	Rectifier Diode / Thyristor Products	SiC Schottky Diode & SiC MOSFET Products
High Temperature Reverse Bias (**HTRB**) IEC 60747-2:2016, IEC 60747-6:2016, IEC 60747-8:2010, IEC 60747-9:2007	1000h 95% (V_{CEmax}, V_{Rmax}, V_{DSmax}) 125°C<T_S<165°C (depending on technology)	1000h 66% (V_{RRM}, V_{DRM}, V_{Rmax}) $T_S=T_{jmax}$ - 20K	1000h 95% (V_{Rmax}, $V_{DS\ max}$) T_j=175°C
High Temperature Gate Bias (**HTGB**) IEC 60747-9:2007, IEC 60747-8:2010	1000h ±V_{GESmax}, ±V_{GSSmax} T_{jmax}	-	1000h ±V_{GSSmax} T_{jmax}
High Humidity High Temperature Reverse Bias (**H³TRB**) EN 60749-5:2018, EN 60068-2-67:1996	1000h 85°C, 85%rH 80% (V_{CEmax}, V_{DSmax}) max. 80V	1000h 85°C, 85%rH 66% V_{Rmax}, max. 80V	>168h 85°C, 85%rH 80% V_{DSmax}, V_{Rmax}
High Temperature Storage (**HTS**) EN 60068-2-2:2008, IEC 60749-6:2002	1000h T_{stg_max}		
Low Temperature Storage (**LTS**) EN 60068-2-1:1993 + A1:1993 + A2:1994	1000h T_{stg_min}		
Thermal Cycling (**TC**) EN 60068-2-14:2010 Test Na	100…1000 cycles (depending on technology) $T_{stg\ max}$ - $T_{stg\ min}$	25…1000 cycles (depending on technology) $T_{stg\ max}$ - $T_{stg\ min}$	200…1000 cycles (depending on technology) $T_{stg\ max}$ - $T_{stg\ min}$
Vibration IEC 60068-2-6:2008 Test Fc	20Hz … 500Hz sinusoidal sweep 5g, 2h per axis (x, y, z)		
Mechanical Shock IEC 60068-2-27:2010 Test Ea	Half sine pulse 18ms 30g 3 times each direction (±x, ±y, ±z)		
Power Cycling (**PC**) EN 60749-34:2010 (detailed test conditions depend on technology)	>20k cycles at ΔT=100K or >70k cycles at ΔT= 70K	10k cycles at ΔT=100K; 20k cycles at ΔT=100K for disc type cells	Tests are performed at ΔT=100 K and ΔT= 70 K,

Table 4.4.1 Overview of SEMIKRON reliability tests, test conditions and relevant standards

After the test is completed, static electrical parameters, thermal resistances and isolation voltage are measured as specified in the following table and evaluated according to the acceptance criteria.

Parameter	acceptance criteria
Thyristor, Diode: reverse current/off-state current I_{RD}/I_{DD}:	< +100% above the upper limit
Thyristor, Diode: on-state/forward voltage V_T/V_F	< +10% above the upper limit
Thyristor: Gate trigger voltage/current V_{GT}/I_{GT}:	< +10% above the upper limit
MOSFET, IGBT: On-resistance/saturation voltage $R_{DS(on)}/V_{CEsat}$	< +20% of initial value
MOSFET, IGBT: Max. change in threshold voltage $V_{GS(th)}$, $V_{GE(th)}$	< ±20% of the lower and upper limits
MOSFET, IGBT: Gate leakage current I_{GSS}/I_{GES}	<+100% above the upper limit
MOSFET, IGBT: Drain-source/collector-emitter cut off current I_{DSS} / I_{CES}	< +100% above the upper limit
thermal resistance $R_{th(j-c)}$ $R_{th(j-s)}$	<+ 20% of initial value
Isolation test voltage V_{isol}	> specified limit

Table 4.4.2 Acceptance criteria for reliability tests

4.4.2 High temperature reverse bias test (HTRB)

This test is used for qualifying the chips regarding their blocking capability and the stability of the chip passivation. A voltage close to the maximum blocking voltage according Table 4.4.1 is continuously applied. The voltage is well above the typical operation voltage to accelerate the test. The devices are heated up in climatic chambers to its maximum operation temperature. Leakage or respectively reverse currents are monitored during testing.

4.4.3 High temperature gate stress test (HTGB)

The gate oxide quality of IGBT and MOSFET is controlled by this test. The maximum permissible Gate voltage is applied in positive and negative direction. The devices are heated up here as well in climatic chambers to the maximum junction temperature. Especially for SiC MOSFET a higher failure rate can be observed because the oxide layer is thinner and the application process is more difficult than for silicon [4.23.]. Leakage current is monitored during testing.

4.4.4 High humidity high temperature reverse bias test (H^3TRB)

The chip passivation at the edges of the chip is additional stressed by high humidity. The reason of the voltage limitation to a maximum of 80V used to be the high leakage current of the power semiconductors in the past. It should be avoided that revers or blocking losses heat up the devices and reduce the relative humidity in the vicinity of the semiconductor. Leakage current is monitored during testing. Modern power semiconductors have not such high leakage currents anymore and the test is increasingly being supplemented or replaced by the HV-H^3TRB test.

4.4.5 High voltage, high humidity high temperature reverse bias test (HV-H^3TRB)

An additional acceleration of aging processes can be achieved by applying high voltage (80% of the rated blocking voltage) As an additional failure mode dendrite can grow caused by electrochemical migration, means ions move in a strong electric field and the presence of moisture.

4.4.6 High temperature forward bias test (HTFB)

In this test the chip backside metallization is tested to carry high currents at high temperatures. The chip conduction losses have to be factored in by setting the junction temperature and more precisely the interface temperature at the die attach. Junction temperature and forward voltage is monitored during the test. Electromigration can happen within the contact joint purely caused by the high temperature and high current density.

4.4.7 High- and Low temperature storage test (HTS, LTS)

Storage at extreme temperatures ensures above all the package (case) quality when exposed to high thermal stress. At the end of the test, the cases must not show any signs of damage (e.g. cracks).

4.4.8 Temperature cycle test (TC)

In this test, components are periodically moved up and down between a cooling chamber and a heating chamber with the aid of a lift cage Figure 4.4.1). The component is passively heated up.

Cycle times are relatively long (minutes up to an hour) to ensure that all parts of the sample will have adopted the chamber temperature and depend on size and weight of the DUT. This test shall detect critical mechanical stress in the case itself and between layers with different thermal expansion coefficients. In particular large solder areas between DBC and copper base plate are under stress (see Figure 4.3.3). The test simulates passive heating up caused by day and night change or by heat curves of the cooling medium. 100 changes between minimum and maximum storage temperature are usually required for industrial applications (-40°C/+125°C). Modern components with sintered chips and without base plate will attain 1500 changes and more.

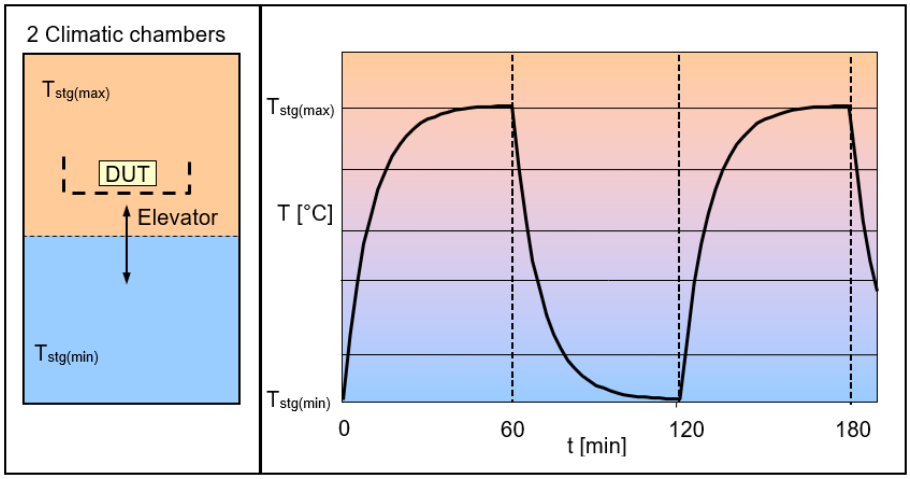


Figure 4.4.1 Temperature cycling test setup and temperature function

4.4.9 Power cycle test (PC)

During the power cycling test, components are actively heated up by losses in the semiconductor and cooled down again with the aid of cooling equipment. To heat the component up, a constant DC current between 85% and 100% of the rated current is injected into the component. The cycle time is between several 100ms and some 10 seconds. Active heating produces a temperature gradient from the chip to the case and the cooling medium. This test shall detect thermo-mechanical stress between layers with different thermal expansion coefficients. Connections between chip and DBC as well as bond wire connections are particularly subject to stress because they heat up most in the short times. The test simulates active heating up of the semiconductors as they would be exposed to during normal operation due to different kinds of stress.
In addition to this Semikron Danfoss has carried out inverter tests, where conduction and switching losses are used to heat up the semiconductors in short times.

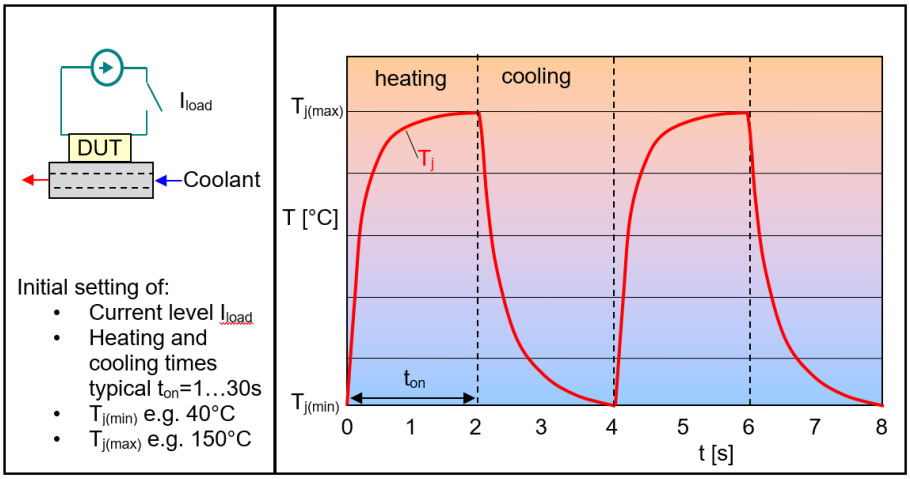


Figure 4.4.2 Power cycle test setup and temperature function

In order to accelerate the aging process, tests are performed with high ΔT_j values (e.g. for ΔT_j = 70K and ΔT_j = 110K) and extrapolated to small temperature differences to estimate the component lifetime in real applications. Test with lower ΔT_j (e.g. 50K) are not part of the product qualification, they are done rarely to validate models and for scientific purpose, because they take very long and

blocking test equipment. A test under real application conditions is not possible because a lifetime of several years is expected for power modules, which would mean that the test also would last several years.
The test results are presented in form of characteristic curves or models (see 4.3.1.5) for the maximum number of cycles as a function of temperature differences. The curves are based on the simplified assumption of uniform failure mechanisms over the entire temperature range. Other Parameter varied to achieve a lifetime model are the medium temperature of the cycle and the cycle duration. The forward voltage, the ΔT_j and the R_{th} is monitored during the test. Instead of R_{th} also $T_{j(max)}$ is monitored assuming that an increasing $T_{j(max)}$ is proportional to an increasing R_{th}.
The operator has a certain degree of freedom to set a specified ΔT_j in a specific time by varying the current level, cooling power and in case of transistors also by the gate voltage. Once set the parameter are kept constant because in the application normally nobody will reduce the load if the devices ages. This control strategy leads to lowest cycle results, because aging affects will increase losses and temperatures and accelerate the aging. In [4.24.] it was shown that the number of cycles could be doubled with constant power and even tripled if ΔT_j was kept constant.

4.4.10 Vibration test

Vibration tests are performed in a frequency range between 10Hz and at least 500Hz using an acceleration force of 5g. Increased acceleration is possible, also the upper frequency is often increased to 1000Hz or even 2000Hz. Depending on the test equipment, there may be limitations regarding the minimum frequency to be used in connection with high acceleration. The test purpose is to find weak points in the mechanical construction, for example:

- Mechanical aging of spring contacts
- Stability of solder contacts in case of vibrating masses - Cracks in cases / structural parts

A low test current monitors safe contact of all auxiliary and main terminals during testing. No additional vibrating masses (cables, DC-link capacitors) have been fitted to the samples, as it would often be the case later in real applications. Comparable tests using the setup of the final application are recommended and may result in different maximum accelerations.



Figure 4.4.3 SKiiP System on a shaker

4.5 Additional tests

4.5.1 Tests for SiC MOSFET (AQG 324)

In general, silicon carbide devices are semiconductors such as silicon power semiconductors and are qualified by the standard tests described above. Nevertheless, lead the different crystal structure, higher electric field strength, faster switching and so on to additional degradation mechanisms. Some additional test to prove the reliability for SiC MOSFET are proposed in the automotive qualification guide AQG 324 [4.25.], where also a description can be found. These tests are not part of the standard product qualification and there is no reference in the IEC standard up to now. One reason could be that the test conditions are still under discussion due to the dynamic development of new chip generations. Although this guideline was written for power modules used in electrical vehicles, the tests are more and more used to qualify power modules for industrial applications.

4.5.1.1 Dynamic reverse bias (DRB)

In this test the SiC MOSFET is stressed by high dv/dt between drain and source at room temperature. The dv/dt should be in the range of 50kV/µs and can be applied by active switching or from an external pulsed voltage source. The device does not carry load current, capacitive current is flowing to charge and discharge C_{oss}. The switching frequency should be not too high (AQG recommendation 25kHz) to avoid self-heating. Purpose of the test is to prove that trapped charges do not lead to $V_{GS(th)}$ drift or $R_{DS(on)}$ increase. Alternatively, also a dynamic HV-H^3TRB test is proposed.

4.5.1.2 Dynamic gate stress test (DGS)

In this test the gate is switched on and off with the recommended negative and maximum positive gate supply voltage at room temperature. Test frequency is in the several 100kHz range. The gate is switched without applied V_{DS} or load current. Purpose of the test is to prove that the $V_{GS(th)}$ drift is low during the expected lifetime of the product.

4.5.1.3 Reverse current pulse test

Bipolar reverse current through the body diode can lead to bipolar degradation of the MOSFET, means an increase of the forward voltage caused by growing crystal defects and positive charge carriers which acts as recombination centres for the electrons. This ageing effect is accelerated by high current densities through the pn-junction of the body diode. Normally the MOSFET-channel is switched on in reverse direction too, but during the dead time in a half bridge configuration the diode conducts for times between for about 1µs. In this test high current pulses equal or above nominal current with a duration of 1µs and a duty cycle of about 1% are applied to the body diode. The MOSFET is switched off all the time.

4.5.2 Micro-vibration (fretting corrosion) test

Contact surfaces may corrode under electrical load and the influence of micro-vibrations. Material abrasion is caused which may result in contact failure. The test objective is to check whether good electrical contact is ensured for the specific combination of contact material. In the example of Figure 4.5.1 MiniSKiiP Springs and recommended contact surface of the PCB are tested until the end of service life. The test simulates thermo-mechanical movements through a piezo actuator (frequency: 1 Hz, amplitude: 50 µm). The contacts are monitored during testing. In order to suppress "clean-burning" of the contacts (i.e. re-establishing good contact), currents are limited to 20 mA and voltages to 20 mV.

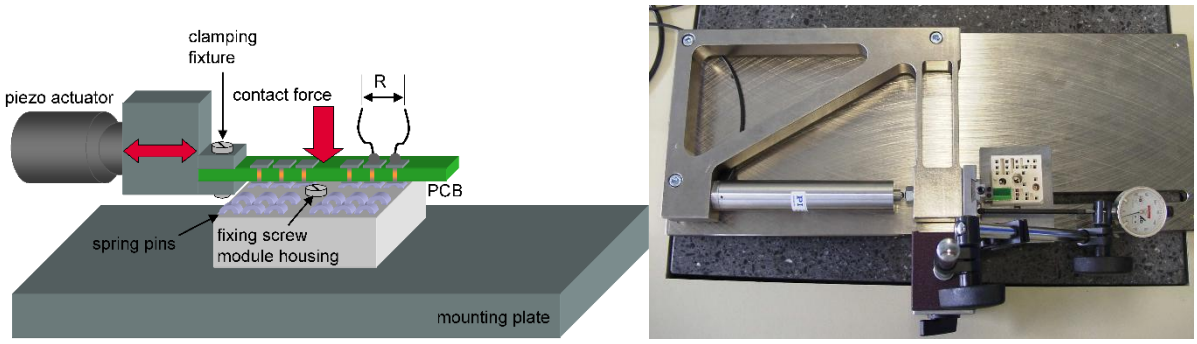


Figure 4.5.1 Schematic drawing and photograph of the micro-vibration test, exemplary test of MiniSKiiP springs

According to [4.26.], a spring contact is considered "good" if the contact resistance after 100k movements is < 10mΩ. The springs of the 2nd generation MiniSKiiP will survive more than 4.5 million movements.

4.5.3 Contact-to-PCB temperature cycling test

In this test, the contact of a power semiconductor module is exposed to extreme temperature fluctuations when mounted or soldered. The solder contact breaks due to its rigid connection after about half the test period, the flexible spring contact survives the test of 2000 temperature cycles from -40°C to +125°C.

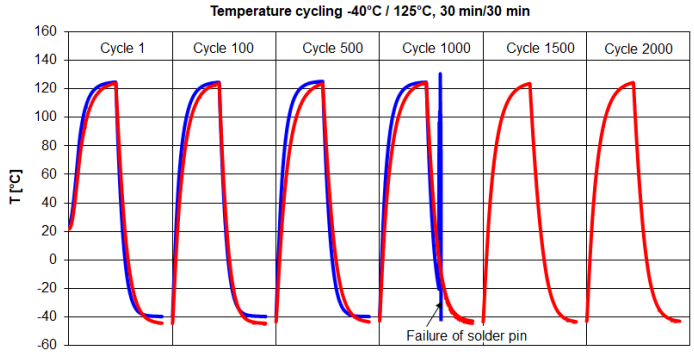


Figure 4.5.2 Contact reliability comparison of solder pin and spring contact (HAL-Sn PCB, Ag spring pin, Ni / Au-flash DBC) after mounting on a PCB subject to temperature cycling.

4.5.4 Corrosive atmosphere (pollution gas) test

In a sealed chamber, components are exposed to aggressive atmosphere for several hundred hours. This is an accelerating test which shall simulate the corrosive effect of environmental impact with the aid of extreme ambient conditions. The corrosion can occur on the chip's metallisation and guard rings, on interconnections (e.g. Al bond wires) or at the terminal contacts.

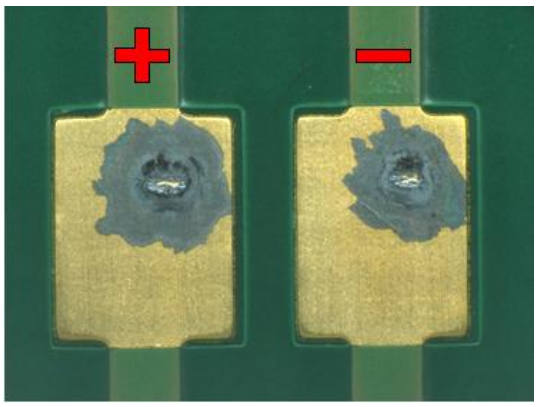


Figure 4.5.3 Contact area after pollution gas test of MiniSKiiP springs on a PCB (3ppm H2S, 40°C, 80% RH, 2000h, 15V)

Figure 4.5.3 shows the contact surfaces of a MiniSKiiP PCB after successful testing. In order to test simultaneously whether there is the hazard of electromigration for this combination of metals (PCB / spring contact), voltage is applied to the sample. There are no signs of electromigration visible (ion migration towards the electric field). What is visible are grey spots on the Ni / gold flash of the PCB because of the corrosive atmosphere caused by the tarnish protection of the spring and black traces of oxidation. These are largely symmetrical around the contact point. The metal / metal contact areas in the middle are clearly visible as well. Owing to the high pressure of the springs against the landing pads, these are almost hermetically sealed against the outer atmosphere. Reliable contact will also be ensured after the test [4.27.].
Whereas in the early 2000s the focus was on the salt spray test, probably due to requirements from offshore applications, resistance to hydrogen sulphide (H_2S) has become increasingly important in recent years. H_2S can be found in the atmosphere of sewage treatment plants, in the petrol industry or paper mills.
Typical test conditions are at 85°C, 85%RH and 50ppm H_2S an atmosphere. Test duration is 720h and to stimulate dendrite growth (see Figure 4.5.4) a DC voltage is applied to the devices (600V for 1200V devices, 1200V for 1700V devices). As this is not a standard test, modules with improved robustness against H_2S are often specially labelled.

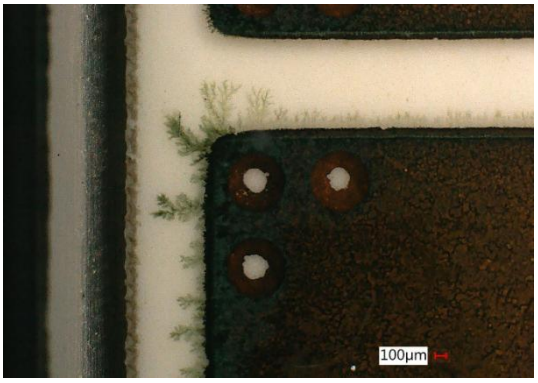


Figure 4.5.4 Copper dendrites at a DBC after H_2S test

4.5.5 Cosmic Ray test

The likelihood for cosmic ray failures under application-close conditions must be extremely low to be acceptable for the user, typically in the range of 0.1 FIT to 100 FIT per device. Average test durations to observe 5 failures are shown in the graph below.

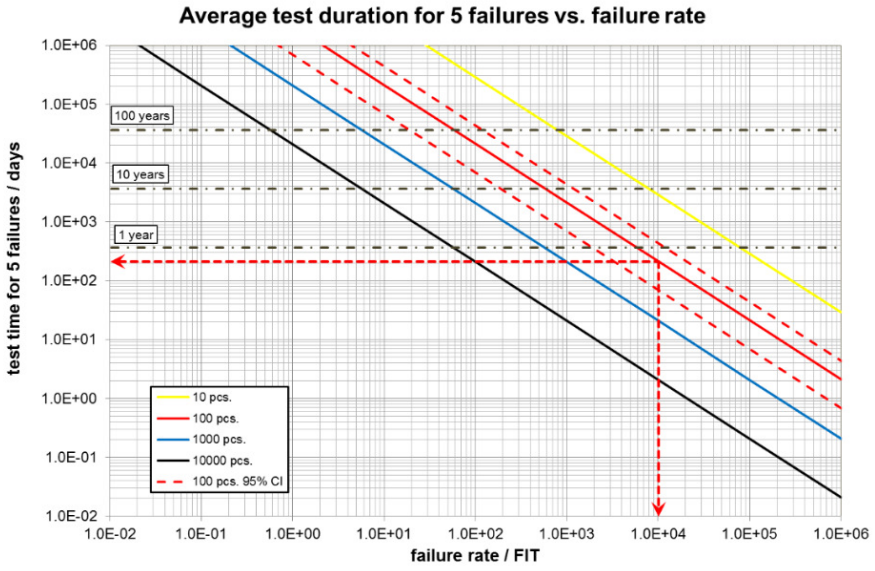


Figure 4.5.5 Average test duration to obtain five failures at a specific failure rate for different sample sizes with non-accelerated lab tests at sea level

As can be seen from Figure 4.5.5, the measurement of such low failure rates with a certain statistical significance requires extremely long test durations or a very large sample size. In order

to determine the failure rate with limited effort in equipment and time, it is best measured in accelerated measurements. The most obvious approach is to move an experiment to high altitude, where the particle flux is increased. The advantage of this approach is the constant presence of a realistic spectrum of cosmic neutrons, and several manufacturers use this approach by testing, e.g., at the German mountain Zugspitze (2962m above sea level (a.s.l.)) or at the Jungfraujoch (3466m a.s.l.) in Switzerland. However, the drawback is a tedious accessibility and an acceleration factor hardly above 10.
By contrast, a particle accelerator can provide high energy neutrons (or protons) at intensities up to a factor of 10^{10} above the natural intensity. Such acceleration factors allow to measure failure rates below one 1 FIT / device in under an hour. The Figure 4.5.6 shows the test time under these accelerated conditions in dependence on the failure rate.

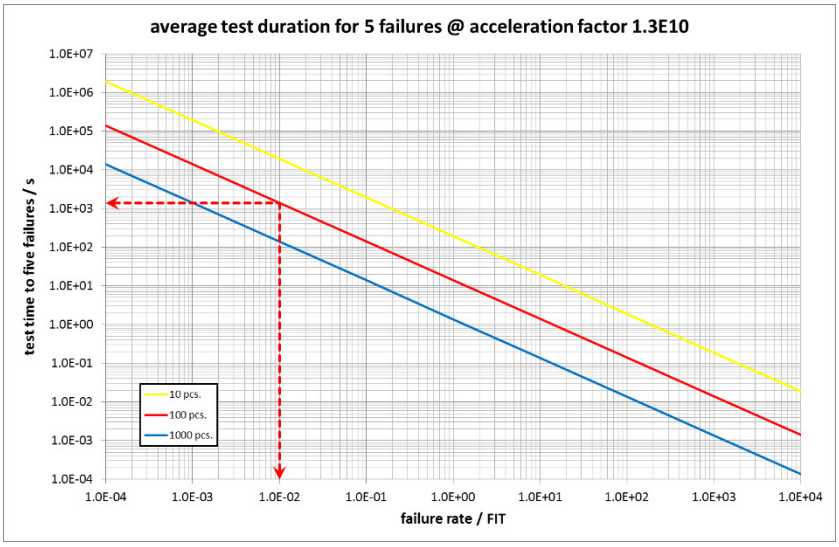


Figure 4.5.6 Average test duration to obtain five failures at a specific failure rate for different sample sizes with an acceleration factor of 1.3 x 10^{10}

In this way, the ruggedness of a device technology can be characterized in dependence on the applied blocking voltage, as demonstrated in [4.17.]. With some additional effort, also the temperature dependence of the failure rate can be determined.
In these measurements, CAL diodes for example turn out to be very rugged against cosmic rays. The failure rate in dependence on the voltage for a device with 1700V nominal blocking voltage is shown in Figure 4.5.7. Some more data and example of how to use it different applications is given in [4.22.].

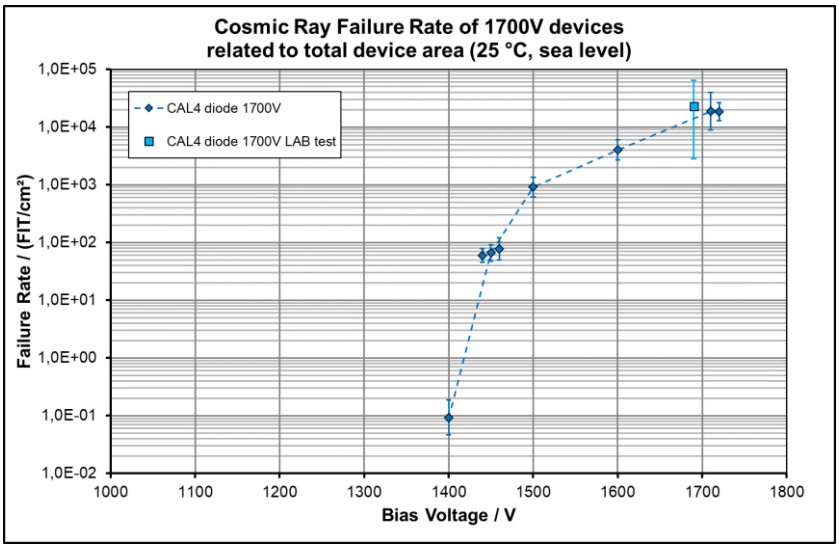


Figure 4.5.7 Cosmic ray failure rate of the 1700V CAL I4F diode technology

The interpolation between measured data points is typically done with the following formula:

$$\lambda(V) = \lambda_1 \left(\frac{\lambda_2}{\lambda_1}\right)^{\frac{V-V_1}{V_2-V_1}}$$

This corresponds to straight lines in the logarithmic plot above.
As 1700V devices are typically used up to 1300V DC link voltage, one can state that the device is virtually immune to this failure mechanism. By measuring this data for our products, it is possible to state the expected cosmic ray failure rate of Semikron Danfoss modules in the field.

4.5.6 ESD immunity tests

The module manufacturer qualifies the Electrostatic Discharge (ESD) immunity of power modules with IGBT or MOSFET and of gate drivers. Regarding the possible stress cases, a distinction can be made between the scenarios "handling and transport" and "function in operation".
These tests are carried out in accordance with the relevant standards, for example IEC 61000-4-2, IEC 60749-26 and IEC 61800-3. The ESD immunity test for handling/transport is intended to examine, evaluate and classify the susceptibility of power modules or drivers to damage or functional impairment due to defined electrostatic discharges during handling or transport.
Often a test setup according for the Human Body model is used. This model simulates a closed, conductive discharge current path through two terminals of a power module or PCB contacts, basing on the discharge of a human body. Due to the rather large ohmic resistance, the discharge current is essentially determined by this and not by parasitic capacitances and inductances. The current waveform is well damped and does not oscillate.
During the test, the test sample is not in operation. At power modules, every auxiliary and main contact is checked against every contact (if possible, also heat sink). At gate drivers for example, the test is carried out by direct contact discharge on all contacts and / or by air discharge on all surfaces and points that can be touched during assembly or service processes. The test voltage is increased in predetermined steps up to the required ESD level. After each voltage level, the test sample is to be checked for previously defined functionalities.
The ESD immunity test for function/operation is intended to examine, evaluate and classify the susceptibility of power modules or drivers to damage or functional impairment due to defined electrostatic discharges during operation. Direct contact discharge to conductive surfaces (metal housings, heat sinks, mounting bolts) as well as air discharge onto insulating surfaces are tested. If direct contact discharge is not possible, an indirect contact discharge test to a vertical coupling plate with pointed discharge electrode must be performed.
A test setup as per standard IEC 61000-4-2 (industry) or ISO 10605 (automotive) is typically carried out as a grounded desktop- or floor-standing appliance. The test sample must be arranged and connected in accordance with its functional requirements and, together with all cables, insulated from the reference ground plate.

4.6 References

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5 Cooling

5.1 Basics

The main focus will be on forced air cooling and liquid cooling in this chapter, since these types of cooling cover 95% of all power module applications. Other cooling methods, such as natural air convection or exotic technologies like evaporative or spray cooling will be mentioned.
Extensive heat build-up in power semiconductors caused by forward, switching and blocking losses has to be dissipated by means of heatsinks, which provide an expanded surface for convection and radiation, spreading the heat flow and adding some thermal mass to the system to damp transient thermal overloads. An advantage of having power modules in a system is that their internal insulation allows them to be mounted on a common heatsink. Non-isolated power semiconductor need one heatsink per switch. The heatsink may also take on some constructive functionality (case, chassis etc.).
Cooling by a heatsink works on the principle that the heat is transmitted to the coolant either by direct heat conduction or via a heat carrier. Coolants may be air, water or water-glycol mixtures, or less frequently oil. In most cases, the heat in a liquid-cooled system is finally also transferred to the air via a heat exchanger. The coolants are circulated by the effect of gravity or using fans or pumps.
The coolant temperature is referred here as ambient temperature T_a (Figure 5.1.1), because the thermal resistance $R_{th(s-a)}$ or $R_{th(r-a)}$ is determined with reference to coolant temperature. This sometimes leads to misunderstandings, especially in liquid cooled systems where the ambient air might have a different temperature than the coolant.
Figure 5.1.1 describes roughly the shares of $\Delta T_{(j-a)}$ for the main components in the thermal path from junction to ambient. The power dissipation is chosen in a way that $\Delta T_{(j-a)}$ = 100K so that it can be also read as a percentage. It shows also what power density you can expect with a simple air or liquid cooler and in which component can achieve the highest improvement with, for example, 10% lower R_{th}. It is not 1:1 reduction, because for example an improved TIM layer will reduce the heat spreading inside of the power module and will increase the $R_{th(j-c)}$ of the module for that reason.

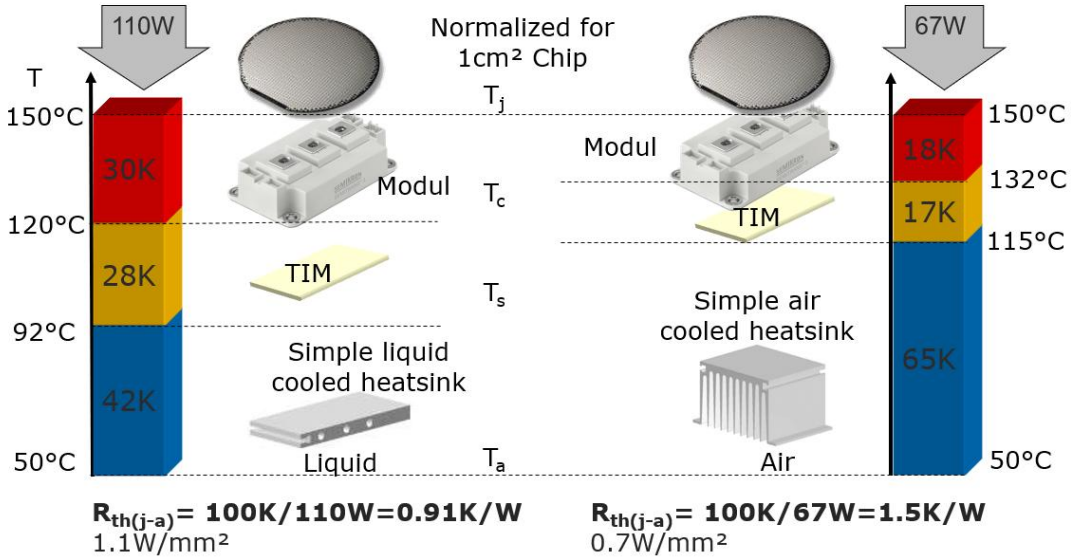


Figure 5.1.1 Shares of temperature differences for the main components in the thermal path from junction to ambient

5.2 Factors affecting thermal resistance

5.2.1 Number of heat sources

The number of heat sources spread across the heatsink has a crucial impact on $R_{th(s-a)}$. Unless explicitly specified otherwise, the values given by heatsink manufacturers apply to a large-area heat transfer across the entire mounting surface. The closer this ideal case is approached with a large number of distributed heat sources, the better this theoretical R_{th} value can be reached. Measurements are complex and time-consuming and manufacturer data on different configurations

is hard to come by. FEM simulations could be a solution, since these simulations are especially meaningful whenever relative comparisons are to be made with known parameters. Figure 5.2.1 depicts simulations [5.1] of the same heatsink comprising 1 x (right) and 3 x 62mm IGBT module(s) (left). For 3 modules the following applies:

$$R_{th(s-a)} = \frac{102°C - 40°C}{1800W} = 0.034K/W$$

The R_{th} of the same heatsink for identical ambient conditions will increase to the following value if just one module is mounted.

$$R_{th(s-a)} = \frac{74°C - 40°C}{600W} = 0.0566K/W$$

This is equivalent to a 65% increase. For some of their heatsinks, Semikron Danfoss specifies $R_{th(s-a)}$ in dependence of the number of modules and module size (Figure 5.2.2). Unless thermal impedances have been given for different layouts, they can be adjusted by weighting R_{thn} with a correction factor gained from the ratio of thermal resistances. The time constants of the thermal impedances will remain the same.

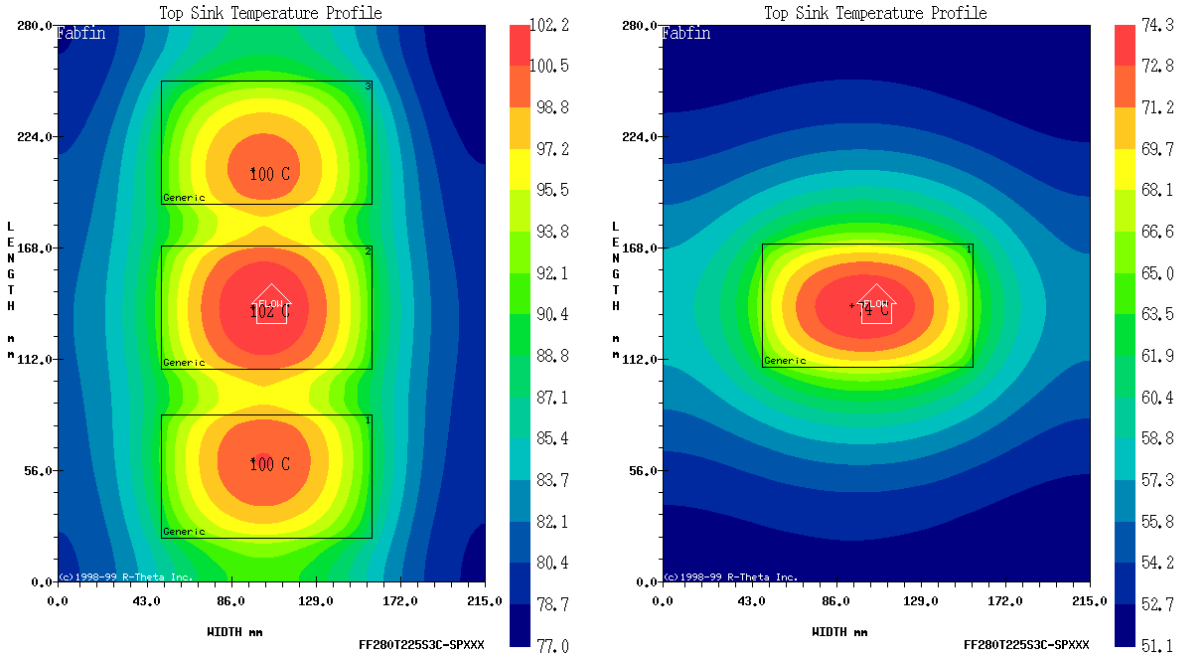
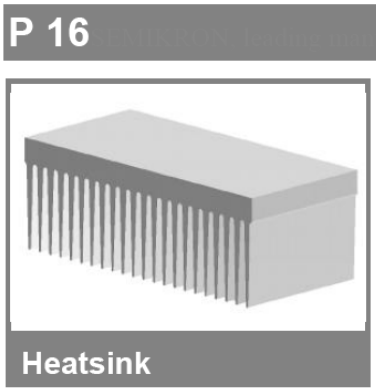


Figure 5.2.1 Simulation of heatsink performance for different numbers of components



Standard lengths	n	b / d Ø mm	R_{thha} K/W	R_{thha} with fan SKF 16B-230-01 K/W	w kg
P 16/170	3	20		0,05	4
P 16/200	3	20		0,046	4,7
	6	20		0,039	
	3	34		0,038	
	2	50		0,04	
	3	50		0,033	
P 16/300	6	34		0,036	7
	6	50		0,024	

Figure 5.2.2 Example of $R_{th(s-a)}$ as a function of quantity n and baseplate width b of the heat sources, given for an 215mm wide air cooled heatsink

5.2.2 Heat spreading

Heat spreading can be achieved either with good material heat conductivity, thick material layers or by using heatpipes in the heatsink itself. It can also be improved by spreading the heat sources evenly across the entire mounting area. This involves finding a compromise between compact design and good heat distribution. In the thermal simulation depicted in Figure 5.2.3, the thermal resistance $R_{th(s-a)}$ is reduced by 9% when the space between modules is increased from 0mm to just 18mm. The number and size of the sources of power dissipation are the same. Power dissipation amounts to 600 W per module and the ambient temperature is T_a = 40°C.

$$R_{th(s-a)0mm} = \frac{101°C - 40°C}{1800W} = 0.034K/W$$

$$R_{th(s-a)18mm} = \frac{96°C - 40°C}{1800W} = 0.031K/W$$

From a thermal point of view, a clearance of up to 3 cm would be desirable on an air cooler; this, however, would require a larger heatsink (→ $R_{th(s-a)}$ = 0.266K/W (-17%)). On a water cooler, this effect is less noticeable owing to its better heat dissipation. Here, a clearance of more than 1 to 2 cm will barely improve the cooling efficiency.

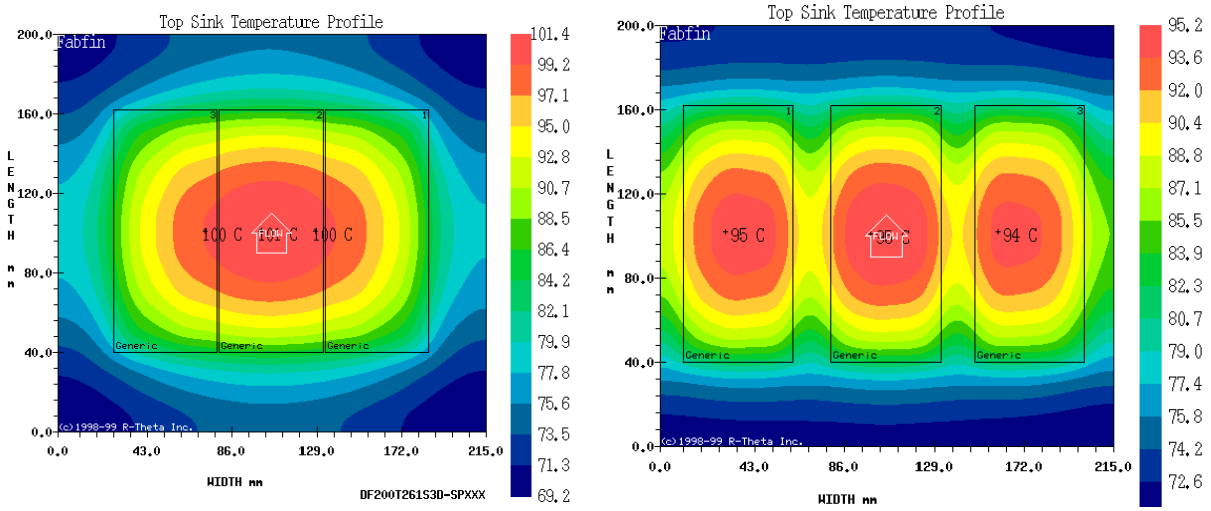


Figure 5.2.3 Effect of better distribution of heat sources across the heatsink surface, temperature simulation on the heatsink surface

Heatpipes

Heatpipes are used in order to transport heat effectively from the heat source to a remote location where the heat is dissipated to a cooling unit (cooling profile, heat exchanger). Alternatively, heatpipes are integrated into the root of the cooling profile to increase heat spreading inside a heatsink, thus reducing the thermal resistance $R_{th(s-a)}$.
Main advantages of the heatpipes are:

- their extremely high heat transport capacity (100 times, other sources say 1000 times higher than copper) with small temperature gradient
- no mechanically moved parts, i.e. no maintenance required - they can be produced in almost any shape.

Heatpipes consist of a hermetically sealed copper pipe that is filled with a liquid under reduced pressure. The inner wall of the heatpipe is clad with a capillary structure (wick). At the hot end the liquid will evaporate absorbing heat of evaporation; the vapour transports the heat to the cooler end where it condenses and dissipates the heat of evaporation to a heatsink or heat exchanger again. The liquid flows back to the hot end, which is supported by the capillary structure (Figure 5.2.4)

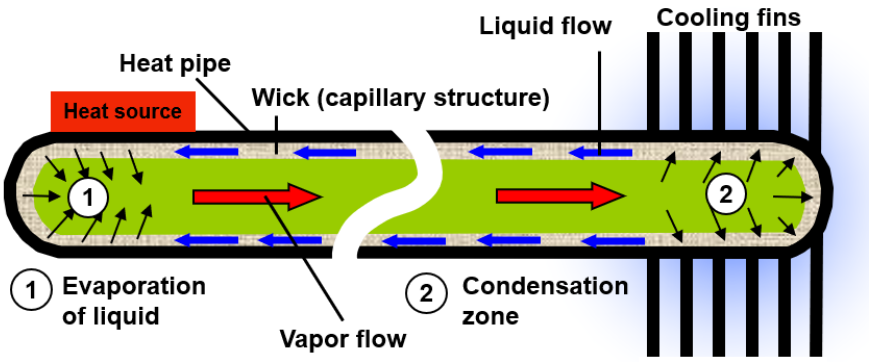


Figure 5.2.4 Principal schematic of a heatpipe. Since gas and liquid are almost in a balance in (1) and (2) and the same pressure is present, the temperatures in (1) and (2) are almost identical.

The capillary structure at the inside of the pipe wall (wick) is a porous structure which supports the capillary effect. It is made of metal foam or carbon fibre, for example. A variety of designs are common:

- sintered powder (highest cooling effect)
- enlarged surface at the inside pipe wall (weak capillary effect only) - grid or mesh structure (most frequently used).

The efficiency of a heatpipe depends on its mounting position. To work against gravity (i.e. evaporating at the top pipe end, condensing at the bottom end) is less efficient but possible if it has a sintered capillary structure. Different media are used as heat transport media, depending on the intended operating temperature range. The temperature range is generally limited: towards low temperatures by the freezing point of the heat transport medium; upwards by the critical point when a distinction between liquid and gaseous state of matter is no longer possible. Frequently used media in heatpipes are water (cannot be used below 0°C), acetone, alcohol, ammonia and fluorinated hydrocarbons.

5.2.3 Position of heat sources in relation to direction of cooling flow

Besides the number and distribution of heat sources on the heatsink, $R_{th(s-a)}$ also depends on the flow direction of the coolant. Figure 5.2.5 demonstrate this with the example of four different positions in relation to the air flow direction. Especially the position on the edge of air outlet is particularly unfavourable. The other three allow heat propagation in the air flow direction and use a larger portion of the heatsink surface, since heat propagation in the direction of air flow is stronger than in the opposite direction.

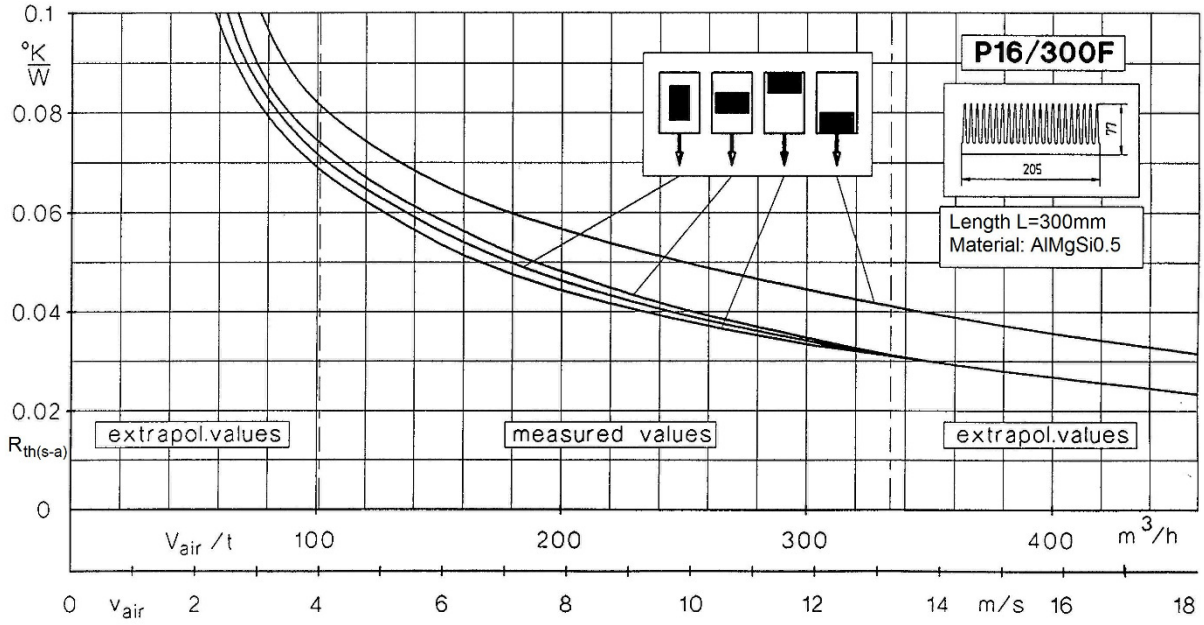


Figure 5.2.5 Thermal heatsink resistance $R_{th(s-a)}$ of a SKiiP assembly versus air flow and position of the SKiiP on the heatsink

5.2.4 Measuring points for determining R_{th}

In addition to all of the design influences, $R_{th(s-a)}$ also depends on the measuring point of the heatsink temperature. To understand correctly: the semiconductor doesn't get cooler, by measuring the temperature at a different point, but the number on paper that could be used for the inverter design is different. As can be seen in Figure 5.2.3, for example, the heatsink surface may have temperature differences of 30K or more. T_s should be measured at the same point for which the value of $R_{th(c-s)}$ or $R_{th(j-s)}$ of the semiconductor modules was specified; otherwise, the chain of thermal resistor from the junction to ambient air would be interrupted. Please note that you should always use the same reference point for comparative calculations in modules supplied by different manufacturers.
The most frequently used measuring point is those underneath the module in a drill hole to 2mm underneath the heatsink surface T_{s2} in Figure 5.2.6. But especially some older Semikron Danfoss modules with baseplate are specified beside the module [5.2].

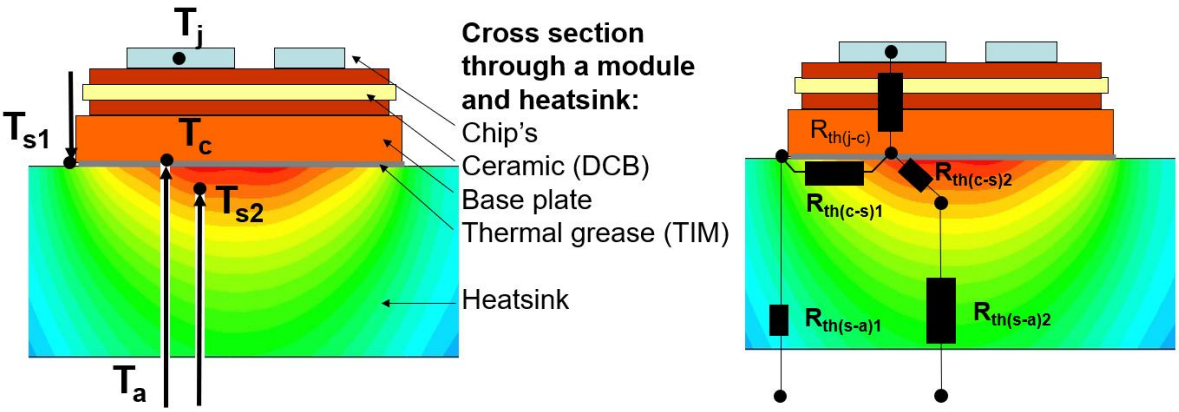


Figure 5.2.6 Measuring points T_{s1} and T_{s2} to determine $R_{th(c-s)}$ and $R_{th(s-a)}$ for a module with baseplate

At T_{s1} is the heatsink cooler than underneath the module. As a result, the temperature difference $\Delta T_{(c-s)}$ is high and $\Delta T_{(s-a)}$ is low. This results in a higher resistance $R_{th(c-s)1}$ and a lower $R_{th(s-a)1}$ compared to the other method where the heatsink temperature T_{s2} is taken underneath the module ($R_{th(c-s)2}$; $R_{th(s-a)2}$). The better the heatsink dissipates the heat, the greater the difference (water cooling ↔ air cooling). The advantage of method 1 - "next to the module" - is the better accessibility to the measuring point. Its disadvantage is the dependency of $R_{th(c-s)}$ on the heat spreading in the heatsink. A specially prepared heatsink is required for method 2. For heatsinks with long fins and small distances it is almost impossible to drill holes from the opposite in the root of the heatsink. The air flow between these fins could be disturbed if thermocouple wires also run along these fins. It is better to mill a trench on the surface into which the temperature sensors are placed and to seal the trench with thermally conductive material before the modules are mounted on it.
With liquid-cooled heatsinks, it is easier to drill a hole at the desired position, but care must be taken to ensure that there is no water channel at this point. Semikron Danfoss uses a specially prepared liquid-cooled heatsink for each module, with holes drilled under each chip position.

5.3 TIM materials

5.3.1 Basics

Semikron Danfoss provides several documents on the topic "Thermal Interface Materials" TIM in its download area [5.3], [5.4]. Some of the content is summarised below.
The main purpose of TIM is to displace the air between power module and a cooling surface (e.g. heatsink) to improve the heat flow and ensure a low $R_{th(c-s)}$. Electrical insulation could be the second purpose, but is not necessary for power modules. Therefore, it will not be discussed further here.

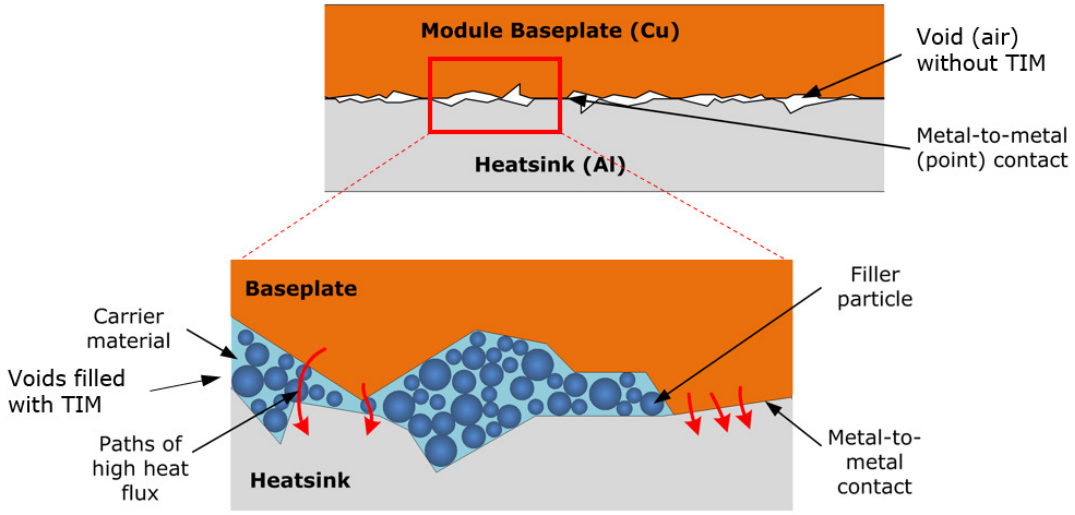


Figure 5.3.1 TIM between baseplate and heatsink to substitute air in the gaps

TIM has not good thermal conductivity (λ = 0.5 … 10W/(m·K)) compared to copper but it is 100 times better than air with λ_{air} = 0.02W/(m·K).
Selection criteria are mainly

- High thermal conductivity λ,
- Ability to adapt deformation by contact pressures,
- Minimal thickness in case of power modules
- Long-term stability, No ageing over time or leakage from the interface
- Easy handling and application to the surface
- Operating temperature

It should be mentioned that a higher λ in the TIM datasheet is not a guaranty for a low $R_{th(c-s)}$ if the contact resistance is high. Thermal conductivity is only representative for the bulk resistance and dominant for thick layers (e.g. 200µm). The contact resistance is in the same order of magnitude for thin layers (e.g. 20µm). The $R_{th(c-s)}$ value is determined by further effects:

- Surface finish of heatsink
- Applied thickness of thermal paste
- Thermal cycles after mounting
- Mounting pressure of module on heatsink
- Design of module (shape of baseplate, layout of chips, baseplate material, etc.)

Pastes and Phase Changer are available as pre-applied TIM from Semikron Danfoss, an overview about advantages and disadvantages gives Table 5.3.1.

	Principle	Advantages	Disadvantages
Pads, Foils, Sheets	One-layer systems (graphite), Multilayer systems (aluminium foils)	Filling wide gaps, high compressibility Easy to apply, can be isolating	Higher R_{th}, cost
Paste	Oils as carrier material and metal or metal oxide as filler	Thin Layer with low R_{th}, Low material and process costs	Difficult handling during mounting
Phase Changer	Wax like carrier material and metal or metal oxide as filler	Easy handling, low R_{th}, particles and dust are easy to remove	Most complicated to apply

Table 5.3.1 Overview thermal interface materials

While pastes are primarily used for baseplate-less modules due to the need of material flow during assembly process, phase change materials are preferred for baseplate modules.

5.3.2 Properties

The carrier material in a paste is generally categorized as a silicone or non-silicone type. In general, Semikron Danfoss recommends using silicone-based pastes as they are well-established, low-cost, high performing, and very reliable. However, some manufacturing facilities (particularly those associated with painting or other chemically sensitive processes) require the absence of

silicone. Therefore, silicone-free pastes are available where the carrier consists of a blend of synthetic fluids. For Phase Changer a wax like carrier material is used which is solid at room temperature and melts at about 45°C…50°C after mounting and initial heating.
The filler material is in most cases metal oxide, silver or graphite. While the filler material is important, equally important are the ratio of filler to carrier and the particle size (Table 5.3.2). High performance TIM often use relatively large particles (e.g. ~50µm) which can limit the minimum thickness, which is important because $R_{th(c-s)}$ is proportional to the thickness. Furthermore, pastes with high metallic filler content can be very viscous, which can cause problems during application and assembly. Since such a paste "flows" less when pressed between the module and the heat sink, it can lead to cracks in the ceramic substrate, especially in modules without a baseplate.

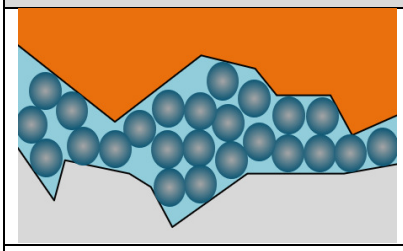
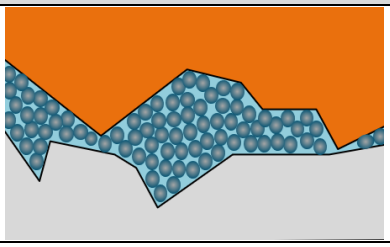
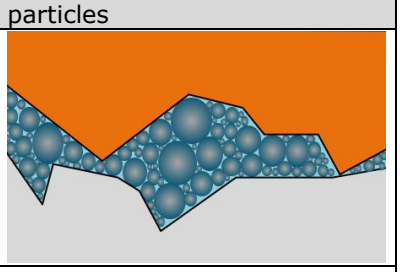
Uniform large particles	Uniform small particles	Distribution of large and small particles
		
low number and small heat paths, Minimum layer thickness defined by filler particle size	high number of heat paths, thin layer possible, But lot of contact resistances between particles	a high filling degree, big particles move in large gaps, small particles filling small gaps

Table 5.3.2 Choosing the right size of filler material particles

By choosing the right filler material und a mix of particle sizes, Semikron Danfoss has qualified a high-performance paste (HPTP) and two different phase change materials (Hala HT and Hala P8). Such a qualification process can take a year or more including

- reliability test under different environmental conditions
- storage test
- power cycle test
- optimisation of layer thickness and print pattern with R_{th}-measurement

An improvement of $R_{th(c-s)}$ compared to proven Wacker P12 can be achieved for

- HPTP by about 50%
- Hala P8 by 30%
- Hala HT by 20%

For the exact improvements see the individual product data sheets, there are two R_{th}-values given, one for the standard Wacker P12 and one for a better pre-applied TIM. Please note that for baseplate-less modules an $R_{th(j-s)}$ is specified where the $R_{th(c-s)}$ is only a part of it.
The two-phase change materials distinguish not only by the R_{th} improvement but also by the operation temperature. "HT" stands for higher temperature and an operation temperature (case temperature) of 125°C, while "P8" has the better thermal performance but only an operation temperature of up to 105°C.
With regards to $R_{th(c-s)}$ it should be also mentioned, that the TIM material has not reached its full effectiveness when first applied. It takes a while until it has moved in the right positions. A settling effect can be seen for pastes (faster) and Phase Changer (slower). The TIM will creep under the pressure of the mounting force. The time to the lowest R_{th} can be reduce by temperature Cycles. The effect can be seen in power cycle test as well. Within the first several 100 cycles the ΔT_j goes down because of settling effects. R_{th} Measurements are done after 3 thermal cycles between 20°C and 90°C.

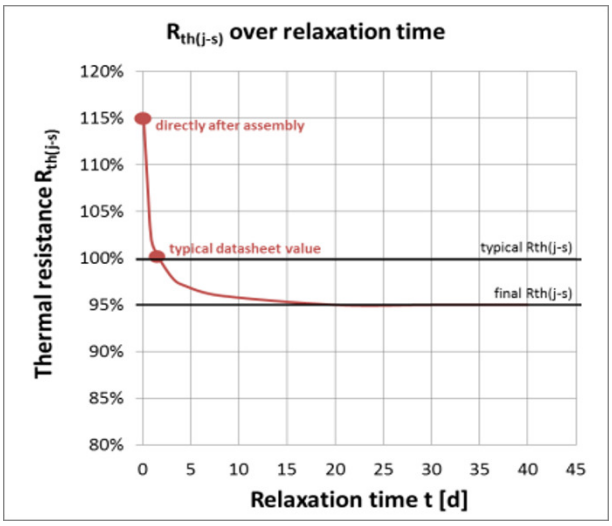


Figure 5.3.2 Typical change of the R_{th} over time

5.3.3 Application of TIM

In small series the TIM pastes can be applied by hand using a roller. This requires some experience. The layer thickness should be measured from time to time to get a feeling for the proper amount of paste.

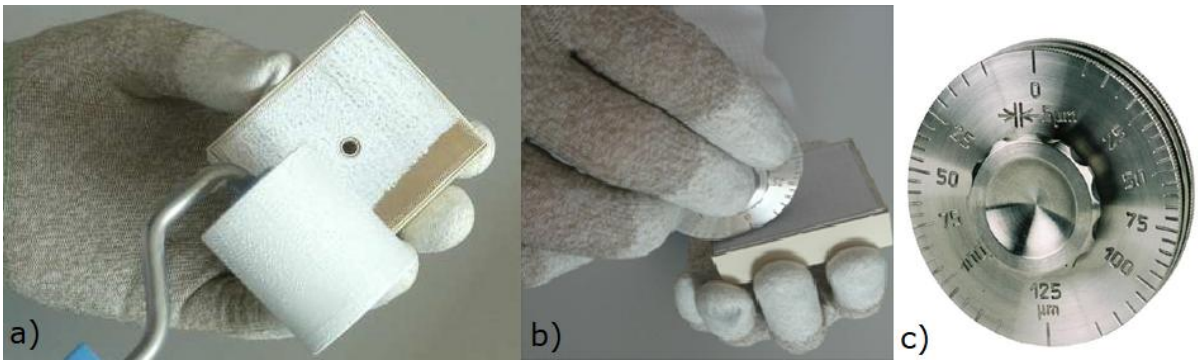


Figure 5.3.3 a) Application of thermal paste by a hand roller; b) and c) measuring the thickness using a rolling gauge

For larger series a printing process is recommended because of the reproducibility of applied layer thickness. Alternative the power modules can be bought with pre applied pastes or Phase Changer. Screen and stencil printing are as used printing processes. Screen printing is used for thinner layer down to 15µm and very small fill particles, while stencils are used for layer thicker than 40µm. In most cases screens apply uniform layer to the module or to mounting area on the heatsink, but in principle both print methods can use honeycomb as print pattern. Honeycomb size, thickness and distance are varied to optimise the thermal interface between power module and heatsink.

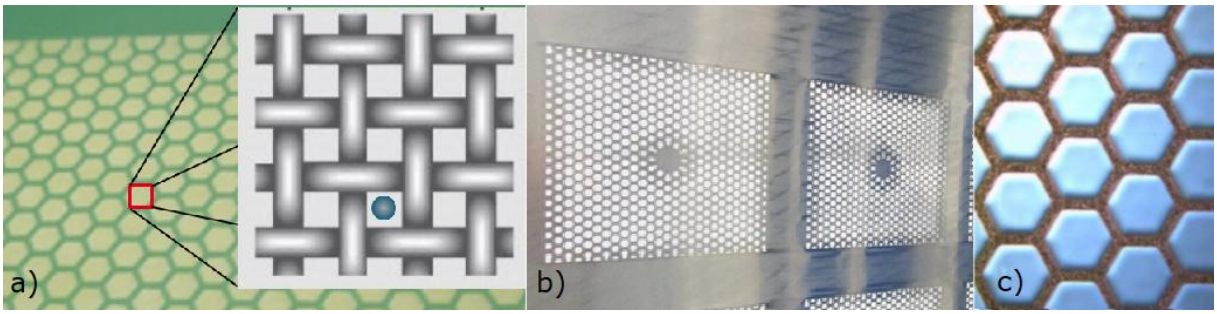


Figure 5.3.4 Screen a) and stencil b) printing are processes to apply TIM-layer, Honeycombs of paste c)

With the distance between the honeycombs the effective thickness can be changed also locally at places where less paste is necessary (see Figure 5.3.5). A larger distance produces a thinner effective layer thickness. For modules with pre-applied TIM a certain print pattern layout is

developed according to the baseplate bending (Figure 5.3.5) and pressure points for an optimized $R_{th(j-s)}$. This layout ensures a direct metal-to-metal contact of the module and heat sink in the area around the screw holes and edges. Only the air gaps created by the bending of the modules and the roughness are filled with thermal interface material. Even for the phase change material, in that case it is not necessary to retighten the screws after the phase change material has melted.

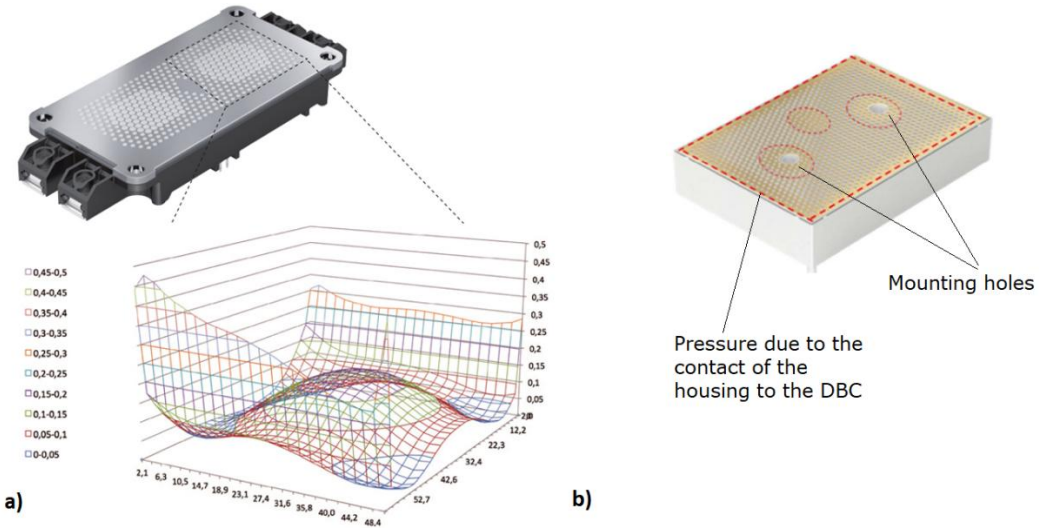


Figure 5.3.5 Optimized print pattern for lowest R_{th}, a) Phase Changer at a baseplate module and a screen of the baseplate profile; b) paste at module without baseplate

5.3.4 Recommended thickness

Given the various parameters that influence thermal resistance, it should be understood that the target paste thickness will vary depending on module type. Semikron Danfoss qualifies the module with an industry standard thermal paste (traditionally Wacker P12) and then specify a thickness. The target thicknesses are given in the Technical Explanations/Mounting Instructions for the product line in question (e.g. MiniSKiiP, SEMITOP, etc.). These thicknesses are valid for any thermal paste with similar physical characteristics to Wacker P12 (i.e. silicone paste with oxide carriers and density of ~2.1g/cm³) and are usually specified over a 5-20µm wide range.
The amount of TIM should be only enough to fill air-filled cavities, but not more. Just adding a thin layer of paste will quickly reduce the thermal resistance in the system, but adding additional paste beyond this will slowly raise the thermal resistance since the thermal conductivity of the paste is lower than the two metals in the interface (Figure 5.3.6).

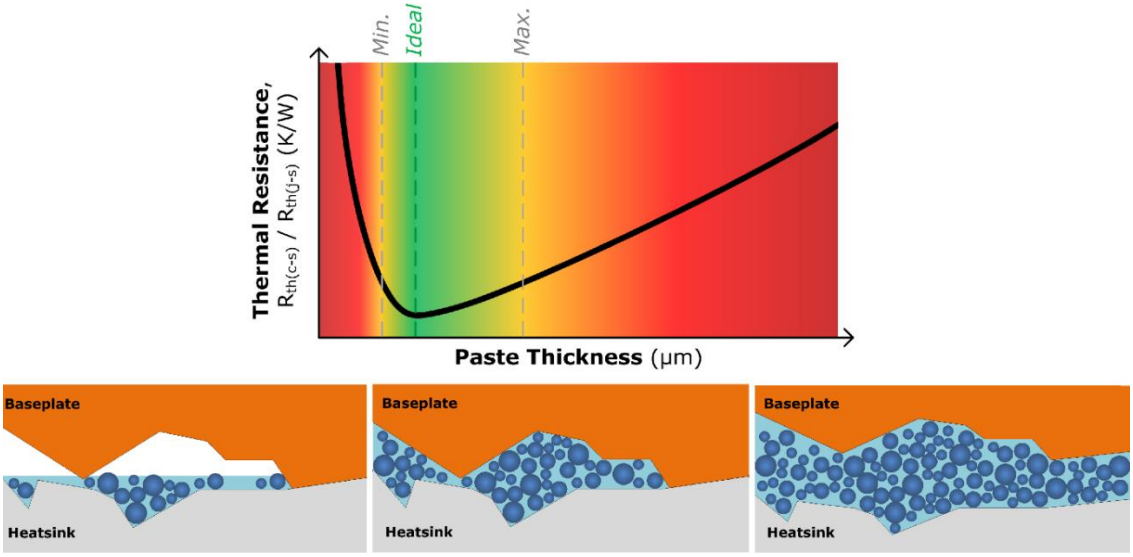


Figure 5.3.6 Influence of TIM layer thickness on $R_{th(c-s)}$

Considering tolerances, it is better to be on the right side of the optimum point, because if the amount of TIM is too low, the R_{th} might increase rapidly.

5.4 Cooling methods, heatsinks and application hints

5.4.1 Natural convection

With natural convection is meant that the heat is dissipated by the natural flow of air, i.e. by the rise of the heated air as a result of gravity. To a small extend it includes here also radiation, because this effect only plays an insignificant role in power electronics and there is therefore no separate chapter dedicated to it.

5.4.1.1 Cooling PCB mounted low-power components

For low power semiconductors (Discretes, TO or SMD packages), it is often sufficient to dissipate the heat via the case surface, the terminals and the tracks on the PCB. A thermal resistance junction to ambient $R_{th(j-a)}$ is specified for low-power components for through hole components with a specified length of the leads and PCB tracks are of a normal width (2-3mm). The R_{th} increases in proportion to the length of the wires and can be reduced by 25 to 30% by using extremely wide tracks. About 15W/(m²·K) can be dissipated with natural convection as a rule of thumb. That means to dissipate 1W with a maximum ΔT = 30K one would need about 22cm² area. Thicker copper traces improve the heat spreading (Figure 5.4.1)

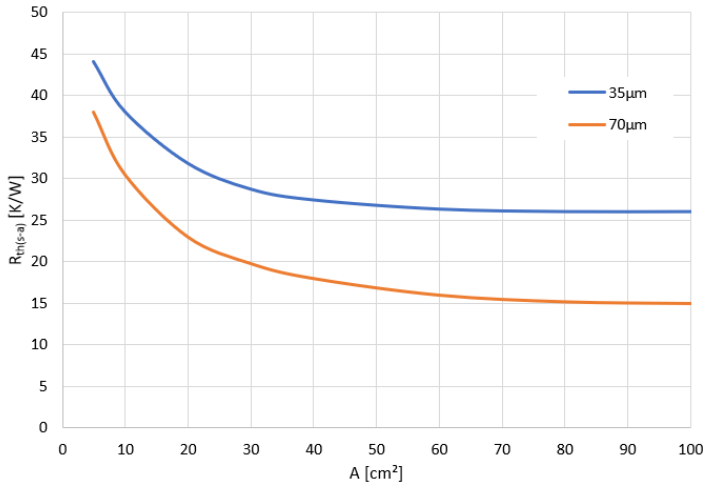


Figure 5.4.1 $R_{th(s-a)}$ of PCB with 35µm and 70µm copper lamination, single-sided cooling as a function of the area

If the power dissipation is slightly higher plastic cases can be mounted on to a cooling plate or chassis plate using a clamp. This increases the area and improves the heat spreading.
Sometimes, the thermal resistance $R_{th(j-r)}$ between the junction and a reference point r is specified for one of the terminals. During operation, the temperature T_r at these points and the power dissipation P that occurs in the component can be measured in order to check that the virtual junction temperature T_j does not exceed the maximum permissible value. The following applies:

$$T_j - T_r = P \cdot R_{th(j-r)}$$

Some low-power components are equipped with metal mounting surfaces (e.g. TO220) that are either connected to one of the terminals or are internally isolated. For such components, the junction to "case" thermal resistance $R_{th(j-c)}$ is given in the datasheet.

5.4.1.2 Cooling plates

Slightly higher rated power semiconductors (up to around 15A mean forward current) can be mounted onto cooling plates in order to dissipate the heat losses. If a terminal is electrically connected to the component case, the cooling plate has to be electrically insulated. If, however, the case (which can also be a plastic case with metal base or metal mounting plate) is isolated from the electric connections, the cooling plate may be, for example, a part of the equipment case or of the assembly chassis.
Figure 5.4.2 shows typical thermal resistances of cooling plates for different materials and material thicknesses in dependence of the area of the cooling plate. The plates are made of shiny metal and approximately square (ratio of both edge lengths not greater than 2:3). The component is positioned in the centre of the plate and considered as a point, means the contact surface of the component is relatively small in relation to the cooling surface.

Scaling factors for the case that the shape differs from a square or the temperature difference to ambient air is larger or smaller than 40K are given in Figure 5.4.3. The mounting position of the plate is vertically, in a way that a stream of air can develop along the plate. A horizontal position would obstruct the airflow and thus increase the resistance. If the plate is coated black, the thermal resistance R_{th} can be reduced up to 15% due to the improved heat radiation.

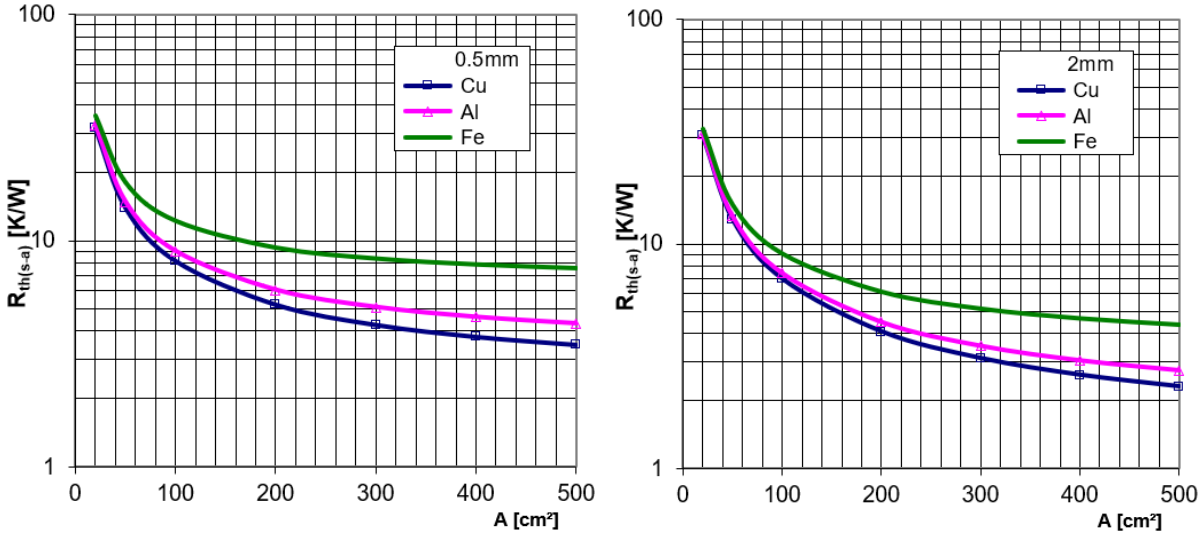


Figure 5.4.2 $R_{th(s-a)}$ for square cooling plates made of steel (Fe), aluminium (Al) and copper (Cu) over the area A for 0.5 mm plate thickness (left) and 2 mm plate thickness (right) for unobstructed airflow across the surface and approximately 40K temperature difference $\Delta T_{(s-a)}$

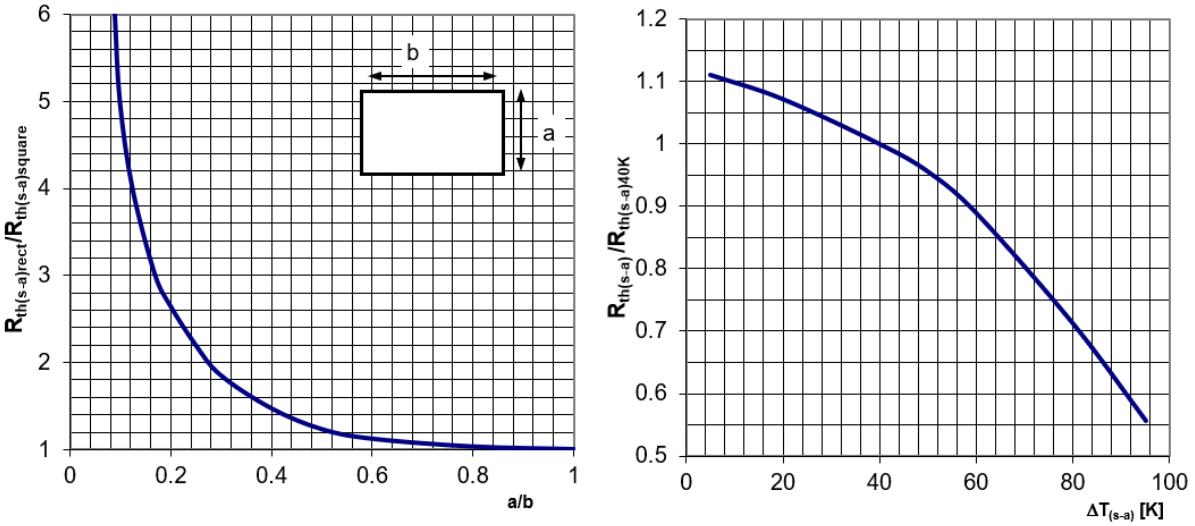


Figure 5.4.3 Relative change of $R_{th(s-a)}$ for non-quadratic cooling plates in dependence of side length ratio a/b (left); Relative change in $R_{th(s-a)}$ as a function of the temperature difference between cooling plate (T_s) and air (T_a) on a base of the 40K value

In order to determine the permissible power dissipation P, the thermal resistance of the cooling plate $R_{th(s-a)}$, the thermal resistance between component and cooling plate $R_{th(c-s)}$ and the internal component resistance $R_{th(j-c)}$ are to be added together. The following thus applies:

$$P_{max} = \frac{T_{j(max)} - T_a}{R_{th(j-c)} + R_{th(c-s)} + R_{th(s-a)}}$$

$T_{j(max)}$: maximum permissible junction temperature,
T_a: maximum expected temperature of the ambient air

It should be noted that the diagrams shown here are subject to numerous unknown influences. The only way to obtain reliable data about the thermal resistance of a particular cold plate is to take measurements on a device in an application-like setup.

5.4.1.3 Heatsinks

For higher power semiconductor components (e.g. more than 15A), cooling plates are no longer sufficient to fully utilise the current carrying capacity. Here, heatsinks or cooling profiles made of aluminium (in rare cases copper, too) with strongly ribbed surfaces are used (Figure 5.4.4).
This profiles often have thick mounting plates (roots) to improve the heat spreading and many fins in different direction to increases the area for convection and allow radiation. Some profiles are suitable both for natural convection (heat is dissipated by the natural flow of air, i.e. by the rise of the heated air as a result of gravity) and enhanced (forced) air cooling (cooling air is moved by a fan) others are optimised for one of these types of cooling.

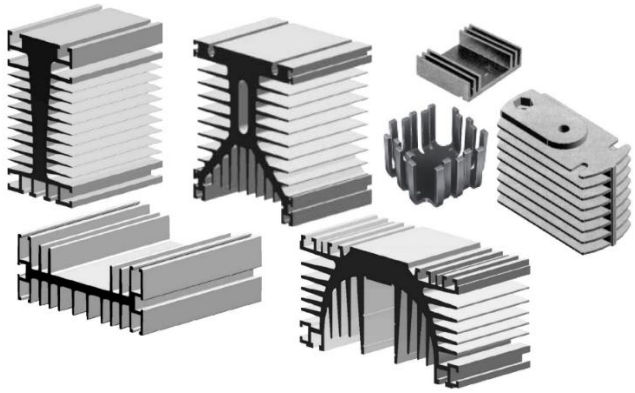


Figure 5.4.4 Examples of heatsinks and extruded cooling profiles for discrete power semiconductors, modules and disc type cells.

The thermal resistance of a heat sink is not a fixed parameter. In the case of natural convection, this value depends on the temperature difference between heat sink and air, i.e. on the power dissipated here. If power dissipation is increased, the heat sink is heated up more, i.e. the effective heat exchange areas are increased (Figure 5.4.5). If, for space reasons, several heat sinks are to be positioned on top of one another, care is to be taken that, in natural aircooled systems, the upper layers are fed warmer air than the others (cf. chapter 5.4.4).

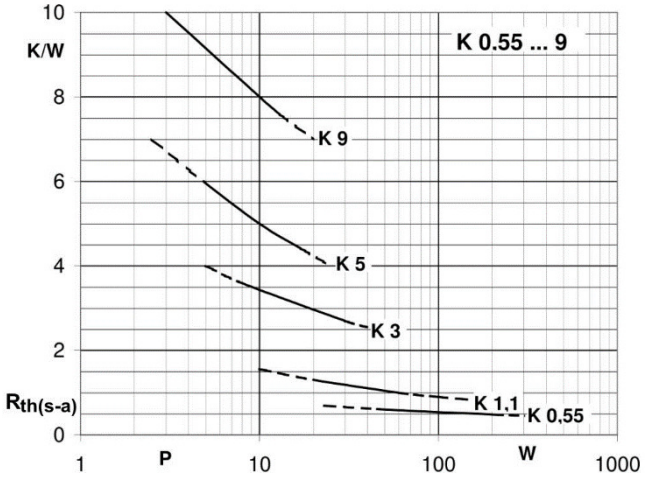


Figure 5.4.5 $R_{th(s-a)}$ in dependence of the dissipated power for several standard heatsink profiles

The heat sink is becoming a part of the electric circuit, if the mounting area of the housing is connected to one of the electric terminals of the semiconductor. This means the heatsink has to be isolated from the chassis and a permanent, good electric contact must be ensured. A nickel-plated copper plate can be inserted between the semiconductor component and the aluminium heat sink for that reason. If the heat sink itself is used as an electric conductor, the aluminium can be protected from contact corrosion using nickel or chrome plating. Before assembly, any existing aluminium oxide layers has to be removed from the assembly surface.
In addition to cast heat sinks, extruded profiles made of AlMgSi are often used to cool power semiconductors. Besides manufacturing-related benefits, these have the advantage that they can be cut from a long bar to any desired length and the thermal resistance of the heat sink can be "adjusted" to some extent. Figure 5.4.6 shows the $R_{th(s-a)}$ of a heat sink profile in various lengths

for a centrally mounted heat source. Longer heat sink profiles may also be equipped with several semiconductor components. With non-isolated components, the possibilities are inherently determined by the circuit chosen; only components with the same potential may be mounted on a common heat sink, e.g. the cathodes on + DC of a bridge rectifier.

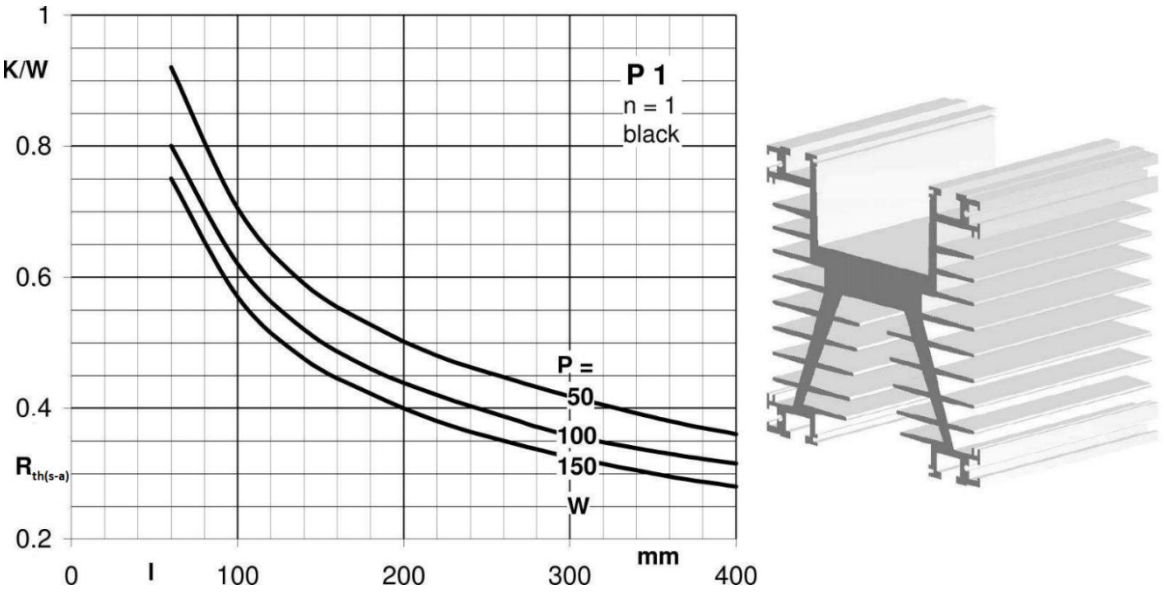


Figure 5.4.6 $R_{th(s-a)}$ for various lengths of P1 heat sink with one centrally mounted component and various power dissipation levels P for natural cooling

To determine the thermal resistance of the heat sink profile equipped with several components, the heat sink can be virtually sawn and the R_{th} determined for each constituent part. If the components are distributed evenly along the length of the profile, this results in better heat distribution. This causes the value $R_{th(s-a)}$ to decrease in relation to the value which would result if the entire power dissipation were concentrated on one single heat source. For the example in Figure 5.4.6 with 2 components of 50W each on one 200mm-long heat sink, this would result in:

$$R_{th(s-a)*} = \frac{R_{th(s-a)}(100\text{mm}, 50\text{W})}{2} = \frac{0.7\text{K/W}}{2} = 0.35\text{K/W}$$

By way of comparison, a single component with 100W on the heat sink of the same length (200mm) has $R_{th(s-a)}$ = 0.48K/W. The datasheets of some heat sink profiles show diagrams with $R_{th(s-a)}$ as a function of the profile length and power dissipation for n components mounted on the heatsink profile.
Disc type cells are inserted between two heat sink profiles to achieve double-sided cooling and consequently about half of the thermal resistance $R_{th(j-a)}$. The clamping device must be designed such that at least one of the heat sink fins is moveable so as to ensure that pressure distribution across the entire surface of the disc type cell is even (Figure 5.4.7).

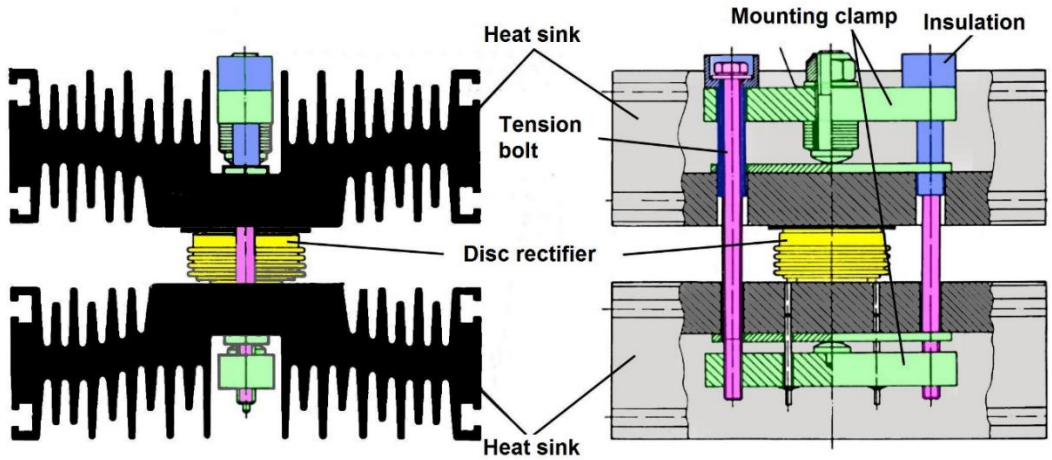


Figure 5.4.7 Double-sided cooling of disc type cell using two heat sink profiles

5.4.2 Forced air cooling

For higher power dissipation (e.g. greater than 50W) forced air cooling is frequently used. The air is blown through the heat sink profile using a fan / blower. Depending on the air flow volume, this reduces the heatsink $R_{th(s-a)}$ between one third and one fifteenth The R_{th} is now virtually independent of the power dissipation and the temperature difference between air and heatsink. Coating or blackening the heat sink does not bring any further improvement when forced cooling is used since convection is mainly responsible for the dissipation of heat. The $R_{th(s-a)}$, however, strongly depends on the volume of air flowing within the given time V_{air}/t or the mean cooling air velocity v_{air} (please note the capital letter "V" for Volume and small letter "v" for velocity). Velocity v_{air} multiplied by the effective inlet area A results in the cooling air volume per unit of time:

$$v_{air} \cdot A = \frac{V_{air}}{t} \quad \left[\frac{m^3}{h}\right]$$

The requirement here is a laminar flow. Between the fins of the heat sink, however, the air flow is normally turbulent. This is of advantage since this helps improve the heat transfer from the heatsink to the air. If there is turbulence, it won't be possible to obtain an accurate reading for the mean cooling air velocity. This is why this the specification of this value is of limited use only. Figure 5.4.8 compares the $Z_{th(s-a)}$ characteristics of natural and forced air cooling using the example of a P16 heatsink in different lengths (given after the slash in [mm]).

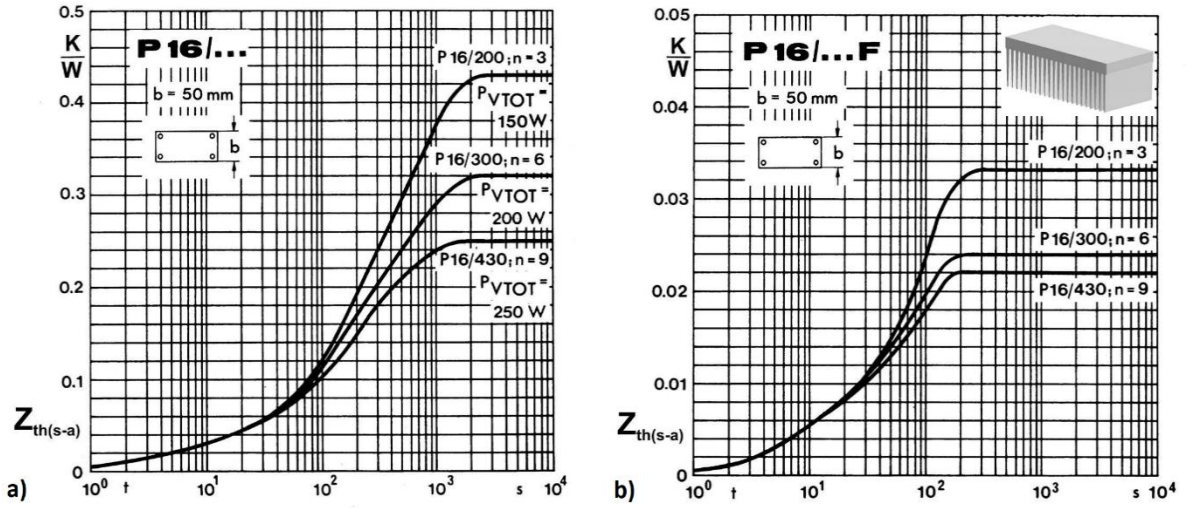


Figure 5.4.8 $Z_{th(s-a)}(t)$ characteristics for different P16-profile lengths and n heat sources; a) in case of free convection with different power dissipation values; b) for forced air cooling

The heat transfer coefficient α is much higher with forced air cooling than with free convection. The rated surface temperature of forced air-cooled heatsinks should not exceed 80...90°C at an inlet air temperature of 35…40°C (condition for datasheet ratings).

5.4.2.1 Cooling profiles

The heatsink material must display optimum heat conductivity and heat spreading (high coefficient of thermal conductivity λ) at reasonable material and processing costs. For this reason, aluminium is often preferred (λ = 247W/(K·m) for pure Al), but copper is also used to meet particularly high requirements (λ = 398W/(K·m)). The thermal conductivity dependence strongly on the material properties and the alloy necessary for a specific production process. In practice, Al heatsink material has λ values of between 150W/(K·m) (Al-die cast alloy) and 220W/(K·m) (AlMgSi extruded material). Heat spreading in the material has a considerable influence on the thermal efficiency of the heatsink. Therefore, optimised dimensioning is important for root thickness, number of fins, fin height and fin thickness:

- The root of a heatsink is the unfinned part of the mounting surface for the power modules where the heat is spread.
- The fins of an air heatsink are used to dissipate the majority of the heat to the environment by convection.

To determine optimised conditions for forced air-cooled heatsink profiles, heat conduction and convection can also be integrated by way of the fin height layout, which will result in the following formula on condition of some simplifications:

$$R_{th(s-a)} = \frac{1}{n \cdot \sqrt{\alpha \cdot U \cdot \lambda \cdot A} \cdot \left(\frac{1}{1+e^{-2\kappa}} - \frac{1}{1+e^{2\kappa}}\right)}$$

$$\text{with } \kappa = h \cdot \sqrt{\frac{\alpha \cdot U}{\lambda \cdot A}}$$

α: heat transfer coefficient U: fin circumference, λ: thermal conductivity,
A: cross-section of fins, h: fin height

Table 5.4.1 provides a rough overview of the design features of various types of heatsink.

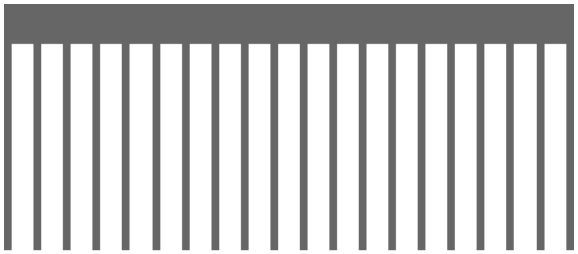
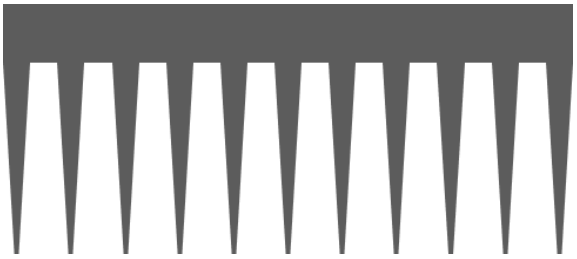
Thin root	**Thick root**
	
Many fins	Few fins
Lower $R_{th(s-a)}$	Higher $R_{th(s-a)}$
Small overload capability (pumps)	High overload capability (elevator)
Short time constants	Long-time constants
Little heat spreading	Good heat spreading
High pressure drop	Low pressure drop
Sensitive against dust	Less sensitive against dust
Sensitive against vibration	Robust against vibration

Table 5.4.1 Properties and selection criteria for different heatsink profiles

5.4.2.2 Pressure drop and air volume

$R_{th(s-a)}$ is mainly determined by the rate of air volume per time V_{air}/t. Of course, it is not just the static, but also the transient thermal resistance (thermal impedance) Z_{th} which is reduced by forced air cooling. Figure 5.4.8 shows $Z_{th(s-a)}$ characteristics for natural and forced air cooling of a 215mm wide standard heatsink profile (Semikron Danfoss type designation P16). Time behaviour also changes by a power of ten. While for natural air cooling the static R_{th} value is reached after 2000…3000s, it takes only 200...300s in the case of forced air cooling.
Increasing the number of fins and fin width will reduce the transfer cross section of the heatsink. As with increased heatsink length, the pressure drop in the cooling air Δp rises and the volumetric flow rate decreases. This is a counter-effect to extending the cooling surface. For this reason, each fan has an optimum with regard to flow cross section, heatsink length and volumetric flow rate. Heat dissipation is dependent on the fan properties, which are described in the fan characteristic $\Delta p = f(V_{air}/t)$ shown in Figure 5.4.9 for nominal voltage of 230V and lower tolerance level V_{nom}-10% = 207V.
The intersection of the characteristic fan curve and the pressure drop curves for the heatsinks $\Delta p = f(V_{air}/t, L)$ enables to determine the volume flow rate. Sufficient cooling should be ensured even when a minimum voltage is applied resulting in a lower air flow. The minimum air volume would be 300m³ in the example of a 280mm long heatsink (red curve) and 340m³/h at nominal conditions.

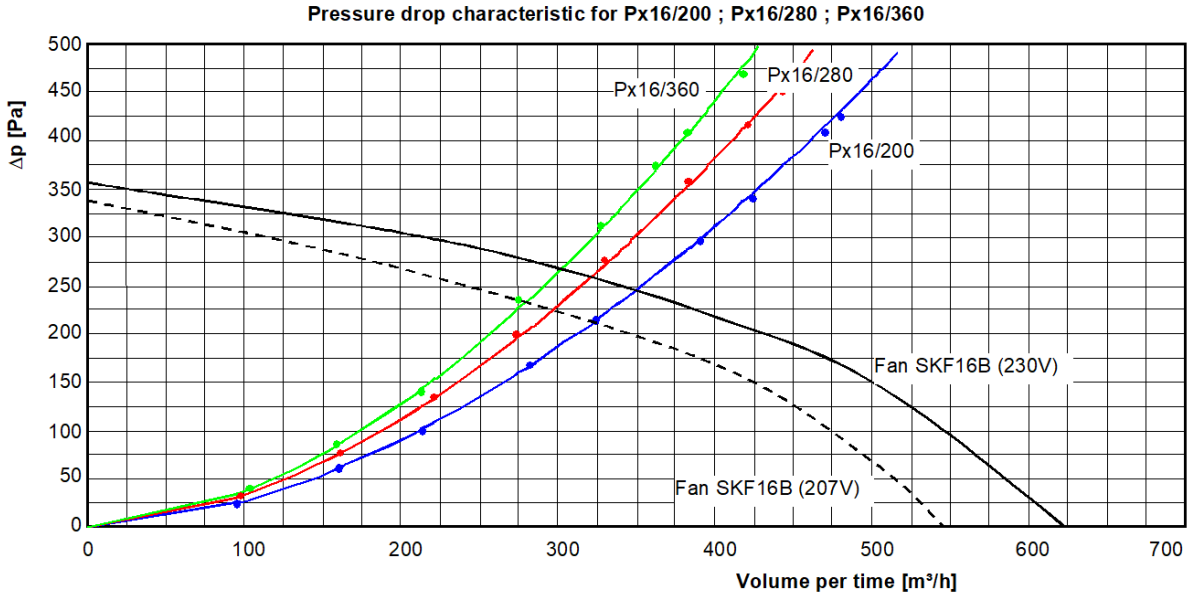


Figure 5.4.9 Cooling air flow of a Px 16/... heatsink profile for various heatsink lengths and fan characteristics

The $R_{th(s-a)}$ as a function of the flow rate is given in a second characteristic (Figure 5.4.10). The $R_{th(s-a)}$ would be 0.0275K/W for the 280mm long heatsink (red line) at 300m³/h respective 0.026K/W at nominal air volume.

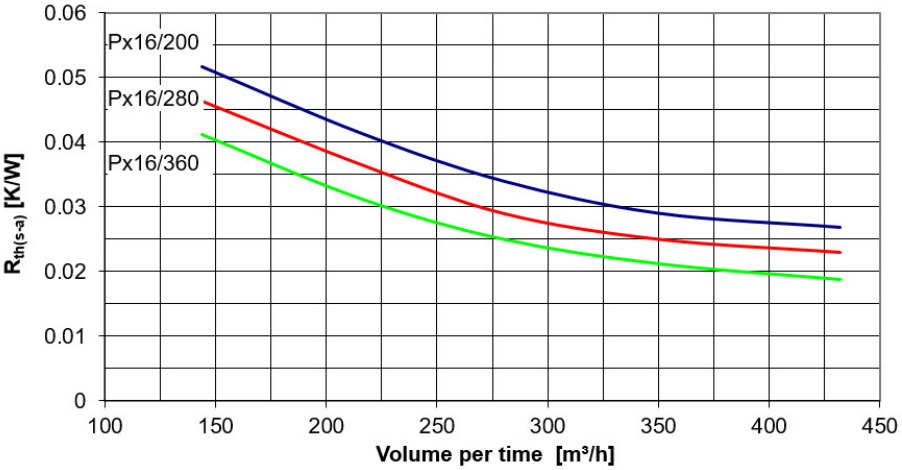


Figure 5.4.10 Characteristic curve of the Px16 heatsink as a function of the volumetric flow rate

Nearby a known operating point, $R_{th(s-a)}$ can be estimated as a function of the volume flow rate according to the following equation:

$$R_{th(s-a)2} = R_{th(s-a)1} \cdot \left(\frac{V_1}{V_2}\right)^K$$

K = 0.7…0.9

5.4.2.3 Fans (ventilators, blowers)

Fans produce the air flow required for air cooling. Depending on the kind of heatsink and application, different fan types are used (Figure 5.4.11). With enhanced cooling, it is important to ensure that the air forced by the fan actually flows through (i.e. between) the fins of the heat sink. Guiding sheets should be used to adapt the fan size to the inlet cross section of the heatsink.

Axial-flow fans

The spin axis of the axial rotor runs parallel to the air flow. The air is moved through the axial rotor which acts similar to an airscrew. The advantages of axial-flow fans are their relatively small dimensions in relation to the high air flow rate handled. Their disadvantage lower available pressure compared to radial-flow fans. Guiding sheets can be used to create a chamber to equalize

the pressure drop to prevent dead areas at the central motor position. As a rule of thumb, the length of the chamber should correspond to the diameter of the fan.

Radial-flow fans or centrifugal fans

Radial-flow fans (Figure 5.4.12) are used whenever, unlike axial-flow fans, a higher pressure drop for the same amount of air is necessary. The air is sucked in parallel or axial to the drive axis of the radial-flow fan, and deflected by 90° as a result of the rotation of the radial rotor and blown out in a radial direction. In order to minimise pressure losses caused by the high exit speed of air care must be taken to continue the air flow straight forward, e.g. by using a channel or diffuser.

Tangential or cross-flow fan

Cross-flow fans have an intake and blow-out slot across their entire length. Air is sucked into the interior of the rotor through the intake slot, where it is swirled, deflected and blown out highly homogenously. Cross-flow fans provide a high air flow rate even at low speeds and can therefore be constructed to emit relatively low noise. The rotor length and the outlet slot are matched to the heatsink width.



Figure 5.4.11 a) Axial-flow fan, b) Radial-flow fan, c) Cross-flow fan

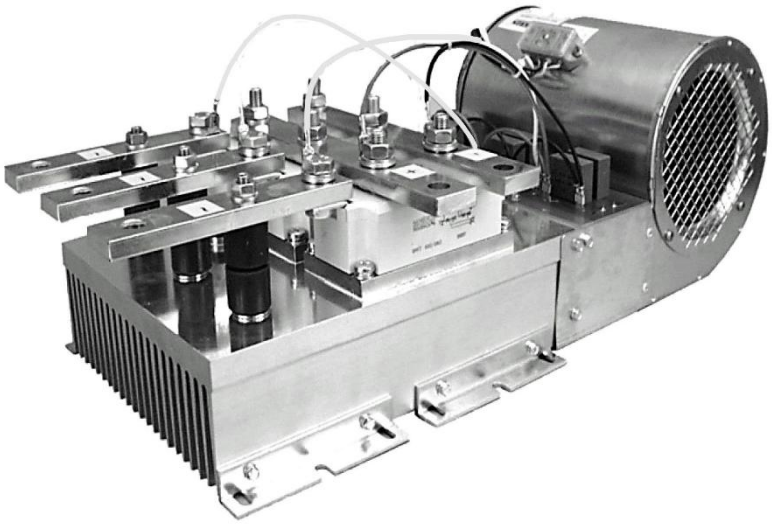


Figure 5.4.12 Set of 3 diode-half-bridge modules in a three-phase rectifier circuit on a cooling profile with radial-flow fan

5.4.2.4 Operating height

The amount of heat to be dissipated depends on the atmospheric pressure and the density of the cooling air. Air density, and hence cooling efficiency, decreases as the operating height increases. Decreasing air density deteriorates heat dissipation. Heatsink efficiency also deteriorates. To factor this in, it is necessary to reduce the inverter power, or to multiply R_{th} for thermal rating by a correction factor in accordance with Table 5.4.2 [5.4].

Height [m /ft]	Performance reduction	Correction factor for $R_{th(s-a)}$
0 / sea level	1	1
1000 / 3000	0.95	1.05
1500 / 5000	0.90	1.11
2000 / 7000	0.86	1.16
3000 / 10000	0.8	1.25
3500 / 12000	0.75	1.33

Table 5.4.2 Impact of operating height above sea level on thermal resistance

These performance constraints also apply to water coolers if the cooling water temperature is regulated by means of an air-cooled heat exchanger.

5.4.3 Liquid cooling

5.4.3.1 Disc type cells

With disc type cells the heatsinks are on electrical potential and used as terminals to connect cables or busbars. The discs are cooled from both sides. Deionised water, which is characterized by low electric conductivity, can be used in closed circuits. Freshwater has good natural electric conductivity. For this reason, in freshwater cooling systems for non-isolated components, sufficiently long water tubes have to be used between the outlet of one component and drain which is located at the earth potential as well as between the cooling components themselves. This is necessary to keep the leakage currents small. And yet, electrolytic (material) removal and accumulation effects cannot be avoided. If need be, sacrificial protection can be used. This sacrificial anode - rather than the heat sinks - would corrode and would have to be replaced at given intervals.

5.4.3.2 Power modules at a heatsink

Liquid cooling for power modules is typically used for very high-power inverters (MW range) as well as for medium power devices where already a liquid coolant circuit is available for other reasons (e.g. car drives, galvanic installations, inductive heating). In most cases, the inlet temperature of the coolant is up to 50...70 °C when the heat of the coolant is released directly into the atmosphere; in industrial plants with active heat exchangers, the temperature can be about 25°C. The temperature difference between heatsink surface and coolant, which is lower than for air cooling, may be utilised in two ways:

- increased power density, but with high dynamic ΔT_j of chip temperature per load cycle (for limits for module lifetime see chapter 4.3.1.5), or
- low chip temperature and increased reliability.

Figure 5.4.13 shows an example for liquid cooling with a 4-fold SKiiP4.



Figure 5.4.13 SKiiP4 with liquid cooled heatsink

The following factors influence the thermal resistance in a liquid cooler:

- the contact area to the coolant (e.g. number of cooling channels)
- the volumetric flow rate as a function of the pressure drop (5.4.3.5)
- the heat storage capability of the coolant (5.4.3.6)
- turbulence in the water flow
- heat conduction and spreading in the heatsink (heatsink material)
- the coolant temperature (5.4.3.3)

Enlarging the contact area of heatsink to coolant will result in improved heat transfer. The traditional cooler is subject to limitations with regard to the number of cooling channels. The pin-fin cooler features little columns protruding into the coolant, which enlarges the contact area and also ensures sufficient turbulence (Figure 5.4.14).

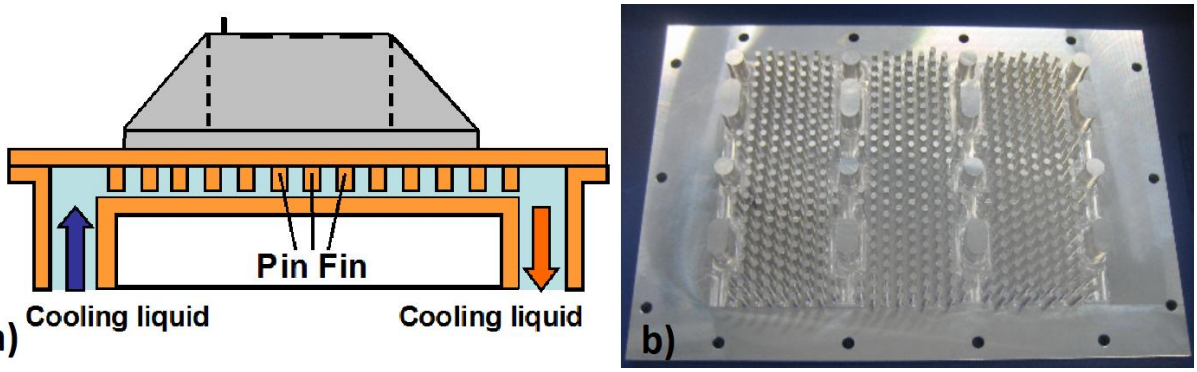


Figure 5.4.14 Pin-fin-liquid cooler to enlarge the heat transfer area; a) Schematic drawing; b) Photograph of the cooling side

The particular shape of the liquid cooler and a sufficiently high flow velocity creates a turbulent flow which substantially reduces the heat transfer resistance between heatsink and liquid (also see the spiral-shaped inserts in Figure 5.4.21 a)). Without turbulence, a liquid film is created on the cooler surface which impairs heat transfer. An optimisation of the fins with fluid simulation will provide the minimum $R_{th(s-a)}$ for a given pressure drop by adapting length, diameter, distance in between and shape of the pins.

Even more so than with air coolers, an even distribution of heat sources across the heatsink surface is important for low thermal resistance. Due to the high heat-transfer coefficient of some 1000W/(m²·K), the heat flow is dissipated to the cooling liquid with only minor cross-conduction. This means that essentially only those areas on which power semiconductor modules are mounted are used for cooling. Copper rather than aluminium as heatsink material will reduce the volume resistance, increase cross-conduction, thus also increasing the effective cooling area. A cooler made of copper allows for a reduction in $R_{th(j-a)}$ by approx. 20% for a standard IGBT module.

5.4.3.3 Direct baseplate cooling

This cooling method eliminates the thermal resistance of heatsink and thermal paste layer between the module and the cooling liquid by directly mounting the module and its base plate over an opening in the heatsink. The necessary sealing is ensured by an O-ring. $R_{th(j-a)}$ can be reduced by by 25% with this method compared to a watercooler with channels. Two different types can be implemented. With the first type, the module base plate has a structured surface (pin fins or meanders) which is immersed into the cooling liquid contained in a trough. For the second variant, the company Danfoss has introduced the term "ShowerPower®" [5.7]. At the time when it was introduced a plastic insert with many parallel holes in the heatsink opening created a turbulent and vertical flow which ensured good and even cooling (Figure 5.4.15 a)). The advantage of the latter solution is the low-cost manufacture of the plastic inserts as compared to structured base plates, while its disadvantage is the reduced contact area and the higher pressure drop. Nowadays the term ShowerPower® is used also for a structured baseplate with optimised meandering channels (Figure 5.4.15 b)).

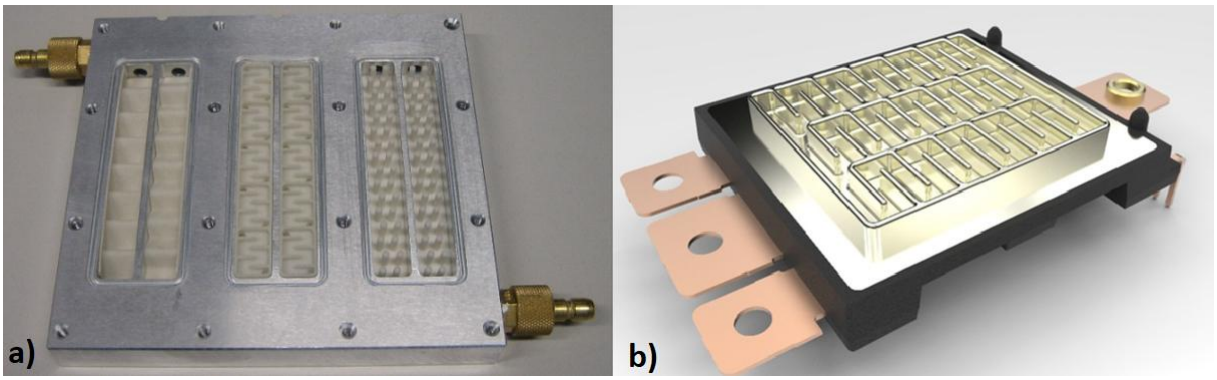


Figure 5.4.15 a) Test cooling plate with various inserts for direct base plate cooling, b) structured baseplate with meander like channels

Microchannel belongs to the direct baseplate cooling too. The baseplates are a special type of liquid cooler (Figure 5.4.16). In the DBC process, the microchannel cooler is furnished with several copper foils that are inserted between two DBC layers. These foils are punctured such that the holes are offset against each other. In the ceramic substrate of the bottom DBC layer there is a liquid inlet and outlet. Due to the offset bores in the sheet copper stack, a turbulent flow is created even at a low coolant flow rate, which ensures good heat transfer from the component being cooled to the cooling liquid. In this way, a very good cooling effect can be achieved with a relatively low pressure drop and little coolant. Two disadvantages might be the reason why it has not become popular so far

- the high risk that channels might get clogged up by dirt or deposits
- the steep temperature gradient within a module due to the low volume flow, which causes parallel chips to operate at different temperatures.

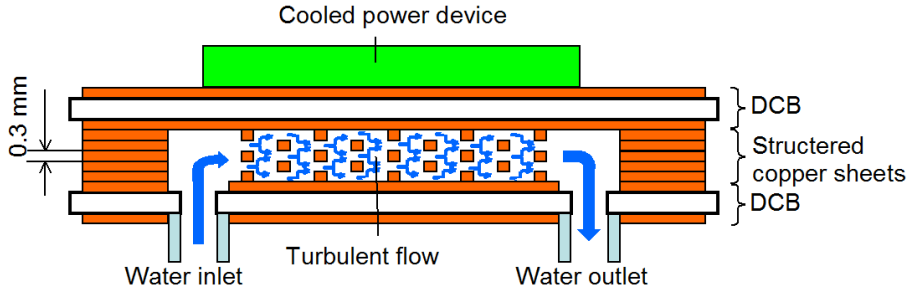


Figure 5.4.16 Drawing showing cross-section of a microchannel cooler

5.4.3.4 Influence of coolant temperature, volume and glycol concentration on $R_{th(s-a)}$

The relationships between $R_{th(s-a)}$ and coolant flow, temperature and water-glycol-mixture come from a study described in detail in [5.7]. The used heatsink is a profile with channels and turbulators like shown in Figure 5.4.13 and Figure 5.4.21 a).
The flow rate is usually the simplest parameter to increase, if a better thermal performance is needed. An increased flow rate leads to a higher velocity and heat transfer. Figure 5.4.17 shows the $R_{th(s-a)}$ as a function of the flow rate for different glycol concentrations and different fluid temperatures. At 2.5l/min the $R_{th(s-a)}$ doubles in comparison to 10l/min, this ration applies for both temperatures. For very high flow rates the improvement in thermal resistance becomes smaller and smaller.

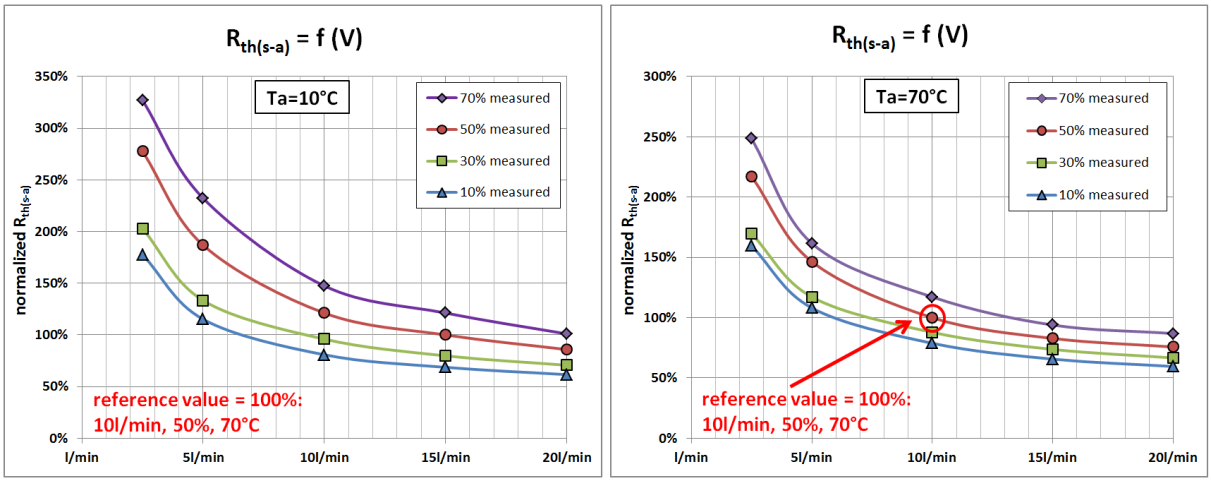


Figure 5.4.17 Normalized $R_{th(s-a)}$ as a function of flow rate

The influence of the mixing ratio on $R_{th(s-a)}$ comes from dynamic viscosity, which is higher for glycol than for water. The dynamic viscosity is indirectly proportional to the Reynolds number, which is a characteristic parameter for turbulent flow (large Re number = large turbulence = large heat transfer coefficient). Furthermore, the thermal conductivity, which is directly proportional to the heat transfer coefficient and the specific heat capacity is worse for glycol than for water.
Figure 5.4.18 shows the impact of different glycol concentrations on the $R_{th(s-a)}$ in relation to 50% glycol concentration. Means a 70:30% glycol:water mixture increases $R_{th(s-a)}$ at 10°C by more than 20% and at 70°C slightly less than 20%. It can be seen that the impact of glycol concentration is almost constant and therefore nearly independent of flow rate and fluid temperature.

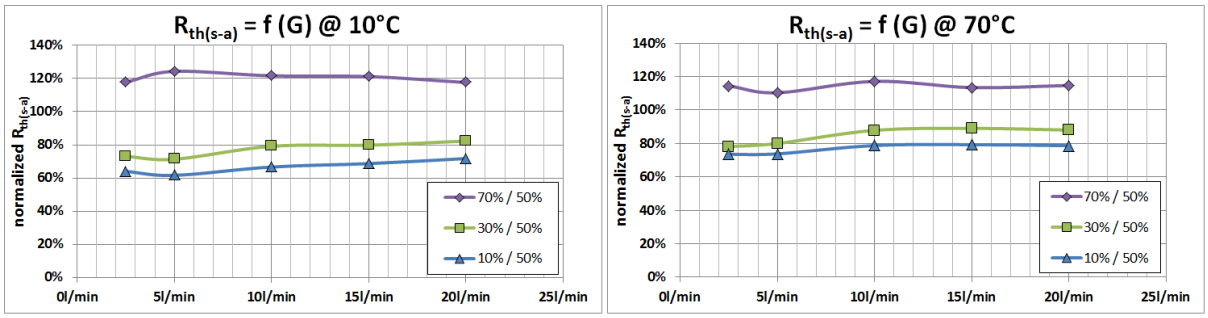


Figure 5.4.18 Normalized $R_{th(s-a)}$ as a function of glycol concentration G

The fluid temperature impact on the cooling and therefore on the $R_{th(s-a)}$ is explained by the temperature depending material properties of the fluid. The thermal conductivity of water increases for higher temperature, the thermal conductivity of glycol decreases for higher temperature. A mixture of 40% glycol and 60% water has a nearly temperature independent thermal conductivity in a temperature range of 0°C to 100°C. The specific heat capacity for pure water is nearly constant. A water-glycol mixture features an increasing specific heat capacity with increasing temperature, but stays always lower than the value of pure water.
Another important material property for cooling is the dynamic viscosity. The dynamic viscosity is smaller for pure water than for glycol. Furthermore, the dynamic viscosity is dependent on temperature. For higher temperature the viscosity decreases, which is improving the heat transfer coefficient.
Figure 5.4.19 shows two charts. The $R_{th(s-a)}$-correlation is shown in the chart on the left side for different fluid temperatures (10°C/70°C) and flow rates. That means the $R_{th(s-a)10°C}$ at 10% glycol concentration is about 11% higher than at 70°C and with 50% glycol concentration it is about 20% higher. The $R_{th(s-a)}$-difference between the fluid temperature of 10°C and 70°C is smaller for higher flow rates. Thus, the greater the flow rate, the lower the impact of the fluid temperatures.
The chart on the right side explains the relation between 10°C and 70°C fluid temperature and glycol concentration. By increasing the glycol concentration, the $R_{th(s-a)}$ increases for lower fluid temperatures.

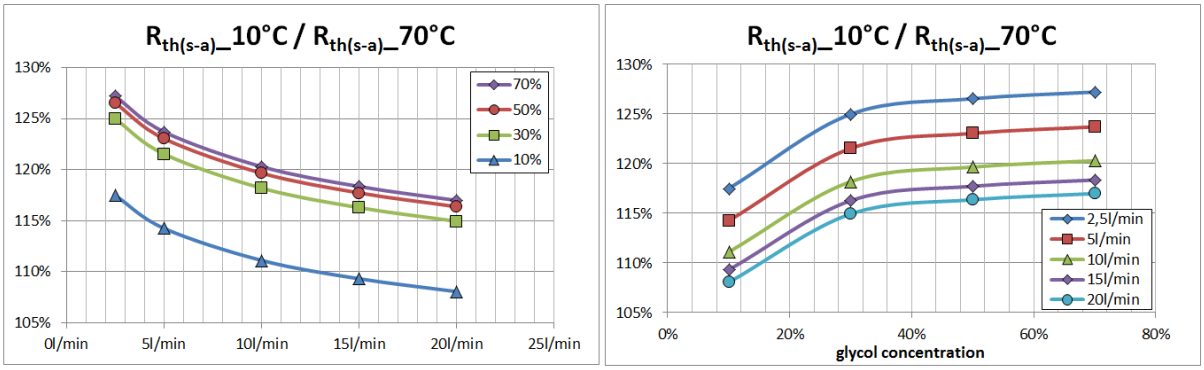


Figure 5.4.19 Normalized $R_{th(s-a)}$ as a function of flow rate and glycol concentration in the ratio of fluid temperature

Formulas to calculate $R_{th(s-a)}$ and $Z_{th(s-a)}$ for variating parameters based on a given nominal operating point are given in [5.7].

5.4.3.5 Pressure drop and test pressure

In a closed cycle, liquid flow from the heat source and back can be generated by gravity (the heated liquid has a lower density, thus rising upwards to the heat exchanger, the cooled water sinks down to the heat source again; thermosyphon cooling). In most cases, however, a pump is used to circulate the liquid. This means that the available pumping power can be used to set the required water volume. Increasing water volume causes the thermal resistance to drop, but the pressure drop across the cooling unit also increases.

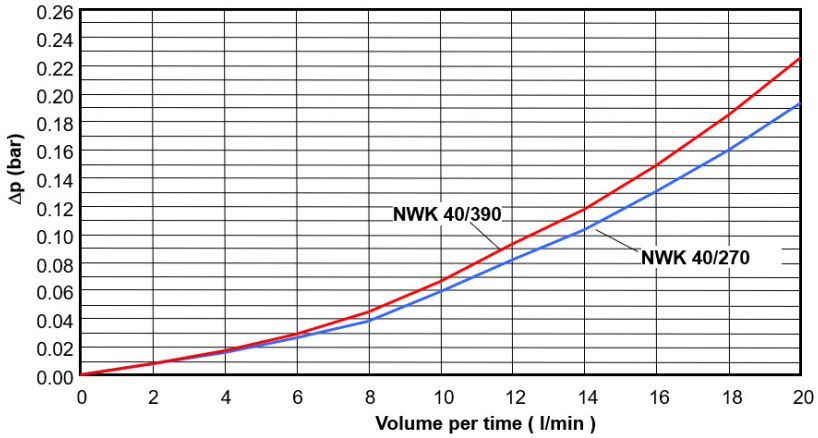


Figure 5.4.20 Pressure drop across a SKiiP3 water cooler (NWK40) for 2 different lengths (incl. 90mm end pieces) dependent on the volume flow rate (water-glycol mixture 50%:50%, diagonally opposite inlet / outlet, T_a= 55°C

The length specification in Figure 5.4.20 applies to a water-cooled heatsink profile including 90mm end pieces, e.g. …/390 means 300mm heatsink profile + 90mm end piece. This image also shows that an elongation of the profile by 66% from 180mm to 300mm will only increase the pressure drop by around 15%. It thus follows that the major part of the pressure drop is caused by the end pieces. This is not surprising, since there is narrowing in the cross section at the connection pieces, a surface for water distribution and 4 changes in direction which are responsible for the pressure drop. If a greater volume of water is to be pumped through the cooling circuit with reasonable pumping power, large pipe diameters are needed. In addition, care should be taken to ensure the following for the cooling cycle:

- no narrowing in the cross-section,
- no quick-release fasteners for the tubes,
- as few directional changes (elbows) as possible

The SKiiP systems with liquid-cooler supplied by Semikron Danfoss are subjected to a leak test at a test pressure of 6bar. The recommended operating pressure is ≤ 2bar.

5.4.3.6 Coolant properties, cooling circuit and chemical requirements

The typical cooling medium to be used for liquid cooling is a glycol (anti-freeze) and water mixture. More rarely, deionised water or insulation oil (fluorocarbons and PAO = synthetical hydrocarbons) is used. Due to its high specific heat capacity (c_p = 4.187kJ/(kg·K)) pure water would be generally preferred to oil or glycol for heat dissipation. Water can either form a closed circuit and be air-cooled by means of a heat exchanger or fresh water is used which runs off after flowing through the cooling unit. Fresh water is noticeably conductive, but this is of minor importance for semiconductor components with internal insulation, since the cooling water remains de-energized in contrast to non-insulated components.
It is important to choose a liquid that is compatible with the cooling circuit and provides either corrosion protection or a minimum risk of corrosion. To ensure corrosion protection in water-cooled aluminium heatsinks, the glycol content must amount to at least 10%. Manufacturers of antifreeze mixtures even call for a higher minimum glycol content to avoid undercutting the necessary concentration of corrosion inhibitors for non-ferrous metals. The hardness degree of the cooling water must not exceed 6. At least for coolant temperatures above 60°C we recommend using a closed cooling circuit. Some of the explanations and tables below dealing with coolants originate from an application manual by Lytron Inc. [5.6]. Table 5.4.3 provides recommendations regarding which metals and liquids are compatible in the cooling circuit.

	Water	**Glycol mixtures**	**Deionised water**	**Non-conductive liquids (Fluorinated, PAO)**
Copper	X	X		X
Aluminium		X		X
Stainless steel	X	X	X	X

Table 5.4.3 Heatsink materials and compatibility of liquids [5.6]

Fresh water

Water is the most effective cooling liquid due to its high thermal capacity. We recommend using a closed circuit. Depending on its chemical composition, fresh water or tap water may cause rust formation in metals. Chloride, for example, which can usually be found in tap water is corrosive. Fresh water should not be used for a liquid cooling circuit if it contains more than 25ppm of chloride or sulphates. The proportion of calcium and magnesium in water must also be observed, since both minerals cause limescale on metal surfaces, thus reducing the thermal performance of the heatsinks (Figure 5.4.21).

Minerals	**Recommended Limit**
Calcium	< 50 ppm
Magnesium	< 50 ppm
Chloride	< 25 ppm
Sulphates	< 25 ppm

Table 5.4.4 Recommended upper limits for ions in cooling water [5.6]

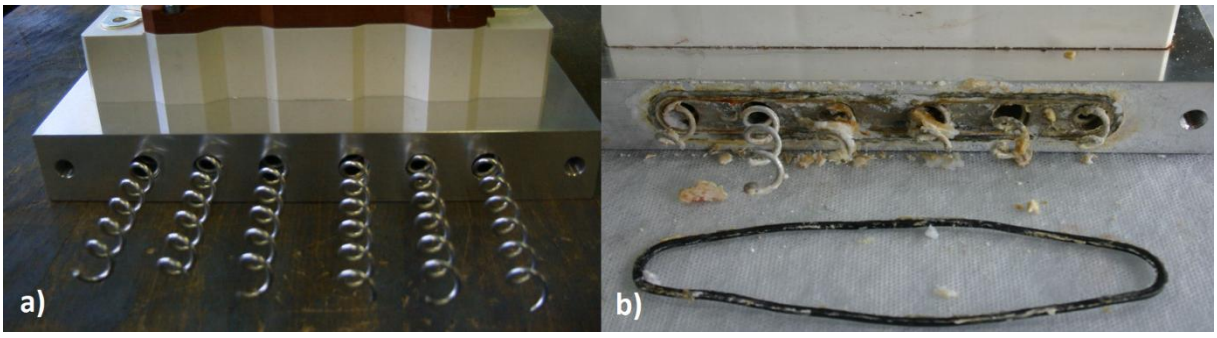


Figure 5.4.21 Cooling channels and turbulators (spirals); a) New; b) After extended use with unsuitable cooling liquid and heavy limescale

Deionised water

Deionised water was freed from ions such as natrium, calcium, iron, copper, chloride and bromide. The deionisation process removes harmful minerals, salts and other impurities which may cause corrosion or limescale. Compared to tap water and most other liquids, deionised water has a high electric resistance and is an excellent insulator. But it easily turns acid when it comes into contact with air. Carbon dioxide in air dissolves in water, thus resulting in an acid pH-value of approximately 5.0. Pressure compensation vessels must therefore be separated from air by means of a membrane. This limits the operating temperature range for the coolant between minimum and maximum. It may be necessary to use anti-corrosives in applications with deionised water. Connection pieces should be nickel-coated. Copper leads are incompatible with the use of deionised water for cooling plates or heat exchangers. Leads made of stainless steel are recommended.

Water-Glycol mixtures

Due to the corrosive effect of water and the often necessary frost-resistance, open or closed circuits with pure water are hardly ever used. The main reason for using water glycol mixture is the frost protection. From a thermal point of view, a glycol content as small as possible leads to the best thermal performance of the heat sink because the glycol reduces the cooling capability of the liquid. For determining the glycol concentration, the minimum temperature of the coolant liquid in the chiller is essential. An operation down to -40°C requires at least a 50% glycol concentration. Ethylene Glycol Water (EGW) and Propylene Glycol Water (PGW) are the two most frequently used solutions in liquid cooling applications. Ethylene glycol has positive thermal properties such as a high boiling point, low freezing point, stability across a wide temperature range, a relatively high specific heat capacity and thermal conductivity. It also features low viscosity, meaning the piping requirements are less strict.
PGW is used for applications where toxicity might be a problem. The glycol used in cars should not, however, be used in a cooling system or heat exchanger, since it contains a silicate-based rust inhibitor. These preventives may turn solid and cause deposits to form on the surfaces of heat exchangers, in doing so impairing their efficiency. Glycol solutions should contain an anticorrosion agent.
By adding glycol, for example, the heat retention capability of the coolant will diminish (e.g. 3.4 kJ/(kg·K) for an addition of 50% glycol and a coolant temperature of 40°C). Since the viscosity and specific weight of the coolant will increase, the thermal resistance from heatsink to coolant $R_{th(s-a)}$ will increase substantially together in line with the percentage of glycol. Compared to pure water, 10% glycol will cause an increase in R_{th} of around 15%, while adding 50% glycol will cause an increase of 50 to 60%. If the glycol content is increased to as much as 90%, R_{th} will double. Please note that these statements also depend on the flow conditions in the heatsink and the coolant temperature.

5.4.3.7 Mounting direction and venting

When setting up the cooling circuit, care must be taken that cooling is not blocked by air bubble build-up. The best mounting set-up therefore consists of vertical channels, while the worst is horizontal channels on top of each another, since the top channel accumulates the air bubbles (Figure 5.4.22).
The preferred flow direction is upwards with the inlet at the bottom and the outlet at the top in the control cabinet. This corresponds to the natural direction of movement of heated water and air bubbles. Loops in the water flow, i.e. an "up and down" arrangement in the cabinet is disadvantageous. In that case, vent valves would be required in the cooling circuit above the power semiconductors (Figure 5.4.23). After the cooling unit has been filled, a test run with the highest flow rate should be performed for an extended period of time (> 0.5 h) without exposing the unit to normal electrical operation. A high flow rate may remove existing air bubbles that might have been generated when the unit was first set up.
When designing parallel cooling circuits, steps must be taken to ensure that the pressure drop is the same in all parallel channels (same number and length of heatsinks, tubes, number of directional changes). The inertia of water in the direction of flow must be observed, since this is responsible for straight water flow, even if equally long parallel paths turn off sideways. Baffles to feed water into the branching channels must be used.

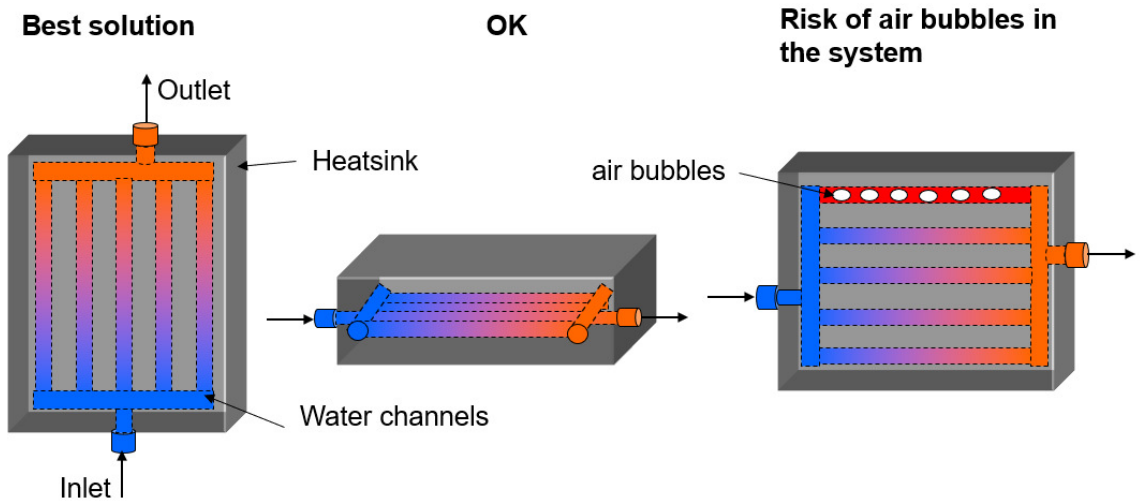


Figure 5.4.22 Proposed arrangement of liquid cooler

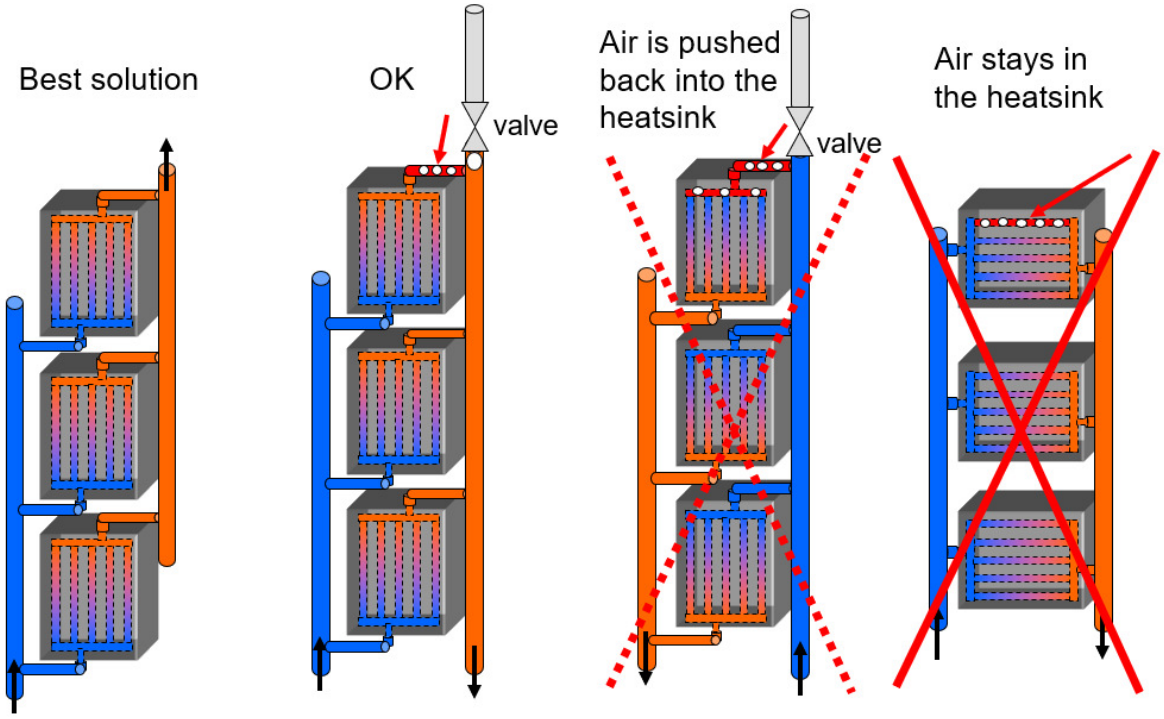


Figure 5.4.23 Setting up the liquid cooling circuit

5.4.3.8 Further possibilities of liquid cooling

Phase transformation cooling

Phase transformation cooling utilises the fact that a given heat quantity (evaporation heat) - the amount of heat depends on the liquid - is required to evaporate a liquid in order to transform the liquid heat carrier into a gaseous state. If the gas condenses, this heat quantity will then be dissipated again. If you manage to keep this cycle of evaporating and condensing going in a closed vessel, large heat quantities may be transported from the point of evaporation to the point of condensation. Gravity and capillary forces will be sufficient to keep the heat carrier moving; pumps are not necessary. Various kinds of cooling equipment use phase transformation for heat transport.

Evaporative cooling

The coolant evaporates at the hot spots, e.g. a power module, gas bubbles will rise and condense on the colder case or separate condenser (Figure 5.4.24).
CAUTION: If the heat flow density is too high, a compact layer of vapour may be created at the heat source. This interrupts the thermal contact between heat source and liquid, meaning that cooling will be abruptly stopped (Leidenfrost effect).

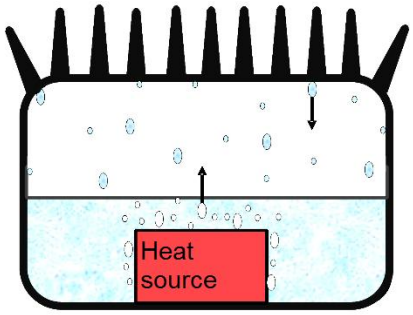


Figure 5.4.24 Principle of evaporative cooling

Spray cooling, jet cooling

These cooling methods use the principle of spraying the liquid coolant onto the surface either as droplets or jet (Figure 5.4.25). To some extent, the heat of evaporation is utilised here, too. Cooling may be applied from one side or both sides. The coolant evaporates at the spot where it hits the surface and condenses at colder spots. Typical coolants are often inert liquids, such as fluorinated hydrocarbons which are available with a wide range of boiling points. Water cannot be used for direct spraying onto chips, because its electric conductivity gets too high even after short use, and this would cause shorting at the chip edges.
It is advantageous if the coolant hits the chip directly, since this will result in optimum cooling directly at the point of heat generation and the exchange of coolant at the spot which is to be cooled occurs rapidly. The disadvantages of spray and jet cooling are the low amounts of evaporation heat produced by the fluorinated hydrocarbons, the complexity of the cooling arrangement, the high pressure of 3 to 15bar prevailing in the entire cooling system and the risk of nozzle clogging (Ø diameters of some 0.1 millimetres). Another problem is the densely packed bond wires lying side by side which often obstruct direct spraying of the chips.

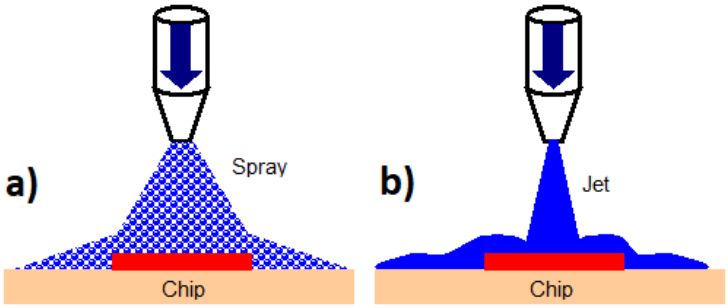


Figure 5.4.25 Principle of spray cooling (a) and jet cooling (b)

5.4.4 Thermal stacking

When several heatsinks are arranged in series with regards to the coolant flow, here called thermal stacking, the reduction in coolant flow rate resulting from the increased pressure drop and pre-heating of the coolant for the units at the coolant outlet has to be considered in the calculations (Figure 5.4.26).

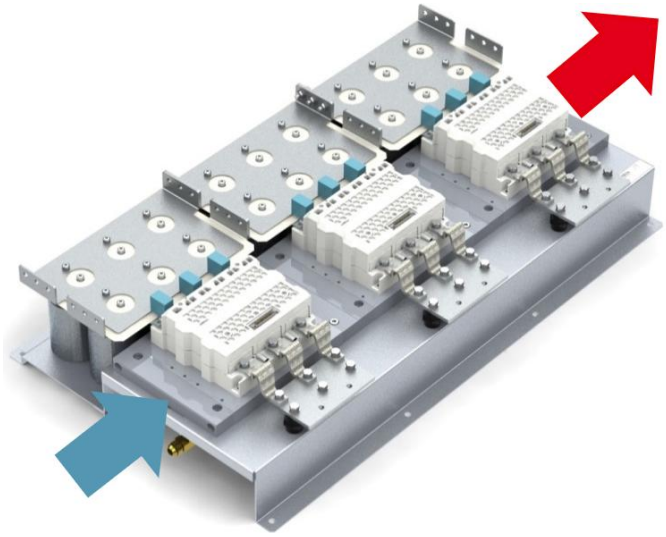


Figure 5.4.26 "Thermal stacking" of 3 SKiiP IPM with liquid cooling

The following two methods are suitable for calculating pre-heating.
a) Determining a thermal impedance $Z_{th(a\text{-}a')}$ between measuring points at the heatsink 1, 2 and 3
b) Calculating coolant pre-heating; the coolant outlet temperature from the first module is the inlet temperature at the second one etc.

5.4.4.1 Implement an additional thermal impedance

A power dissipation $P_{tot(n)}$ of a heat source lead to a temperature increase. This is nothing different as a thermal resistance $R_{th(a\text{-}a^*)}$ or a transient thermal impedance $Z_{th(a\text{-}a^*)}$. In order to determine this, the temperature differences between two adjacent heatsinks (Figure 5.4.26 Inlet 1 → middle position 2 → outlet 3) must be determined for a given power dissipation. As time passes, the second and any following heatsink will get warmer than the unit directly in front. This temperature difference divided by the component power dissipation results in $Z_{th(a\text{-}a^*)2}$ for the second heatsink. For this part of the transient thermal impedances, 1 R/Tau element is sufficient in most cases. The following known correlation applies to component 1 in the direction of coolant flow:

$$Z_{th(s-a)} = \sum_{\nu=1}^{n} R_\nu \cdot \left(1 - e^{\frac{-t}{\tau_\nu}}\right)$$

To take into account the preheating of component 2, an additional element for the temperature difference between heat sinks 1 ("a") and 2 ("a*") is introduced. If the losses of the heat sources are not identical the losses must be weighted.

$$Z_{th(s-a)2} = \sum_{\nu=1}^{n} R_\nu \cdot \left(1 - e^{\frac{-t}{\tau_\nu}}\right) + \frac{P_{tot1}}{P_{tot2}} \cdot R_{th(a-a^*)} \cdot \left(1 - e^{\frac{-t}{\tau_{a-a^*}}}\right)$$

For component 3 and any additional one, this applies by analogy

5.4.4.2 Calculating pre-heating for air cooling

The basic idea behind this method is to retain the well proven basic equations of temperature calculation and re-determine the coolant inlet temperature for the "n-th" element only. This can easily be done using the heat storage capability of the coolant. Both the specific weight and the heat storage capability are temperature-dependent, which is why there is a temperature coefficient for pre-heating in the equation.

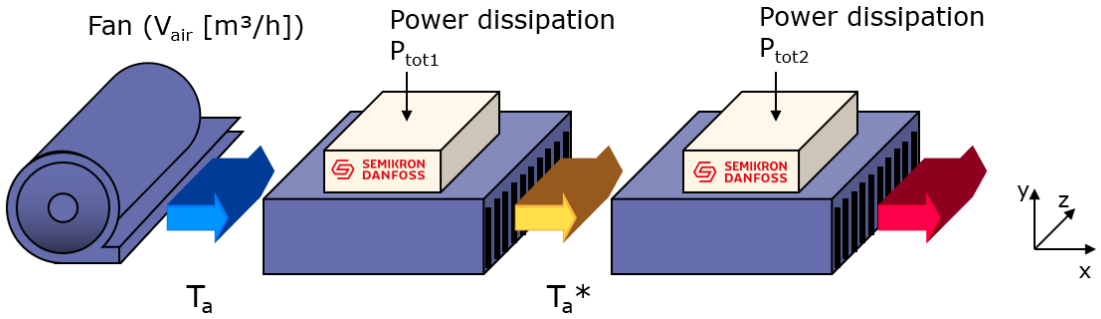


Figure 5.4.27 Thermal stacked, air-cooled layout, split into sectors with different air pre-heating

The general formula is:

$$T_a^* = T_a + \left(\frac{1}{c_p \cdot \rho} + TC_c \cdot T_a\right) \cdot \frac{P_{tot1}}{V_{air}}$$

c_p:	Specific heat capacity of air [kJ/(K·kg)]
ρ:	Density of air [kg/m³]
TC_c:	Temperature coefficient of the specific heat capacity
T_a*:	Coolant temperature for the second heat source
P_{tot1}:	Total power dissipation of heat source 1

Adapted to an average atmospheric pressure of 1 bar, a basic temperature of 0°C and the conversion to a specification for the volumetric flow rate in [m³/h], the following results

$$T_a^* = T_a + (2.807 + 0.01 \cdot °C^{-1} \cdot T_a) \frac{°C \cdot m^3}{W \cdot h} \cdot \frac{P_{tot1}}{V_{air}} \cdot K_{ing}$$

K_{ing}: Correction factor for uneven heat profile at the outlet of heatsink 1 (1…1.25)

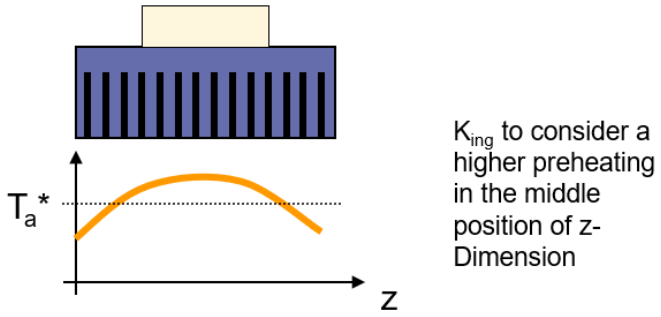


Figure 5.4.28 Uneven temperature profile of the exiting air over the fan cross section if heat sources are arranged centrally

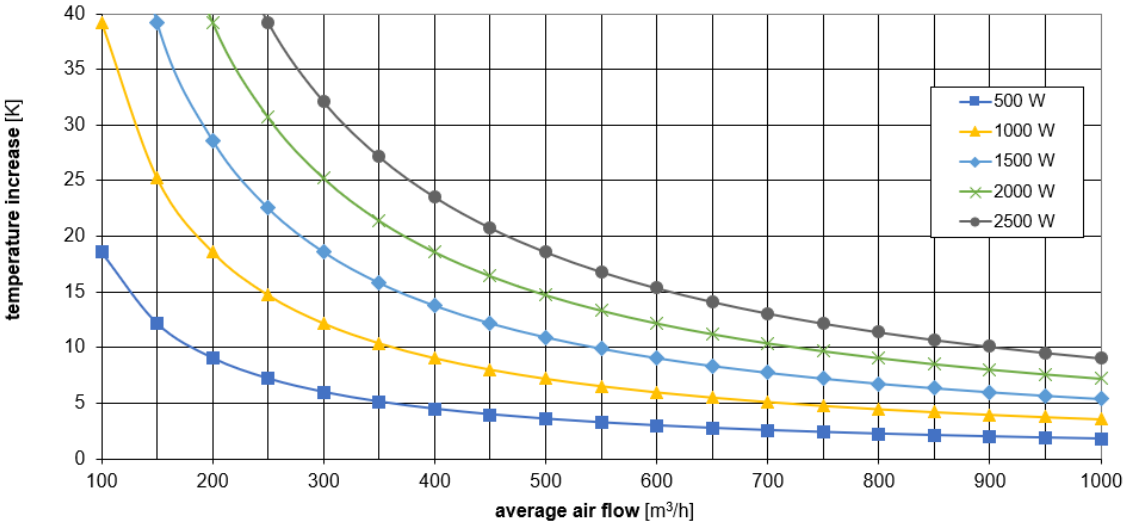


Figure 5.4.29 Temperature difference between incoming and outgoing air as a function of power dissipation and the volume flow, T_a = 40°C

5.4.4.3 Calculating pre-heating for liquid cooling

In principle, the same basic equation applies to thermal stacking for liquid cooling as for air cooling: However, it must be taken in mind that the dynamic viscosity changes as a function of the temperature. The heat capacity for a 50:50 water/glycol mixture and an adaptation to the flow rate in [l/min] results in:

$$T_a{}^* = T_a + (0.0174 - 0.000013 \cdot °C^{-1} \cdot T_a) \frac{°C \cdot l}{W \cdot min} \cdot \frac{P_{tot1}}{V_{coolant}}$$

For pure water, the specific heat capacity and the temperature coefficient will change to:

$$T_a{}^* = T_a + (0.0133 - 0.000008 \cdot °C^{-1} \cdot T_a) \frac{°C \cdot l}{W \cdot min} \cdot \frac{P_{tot1}}{V_{coolant}}$$

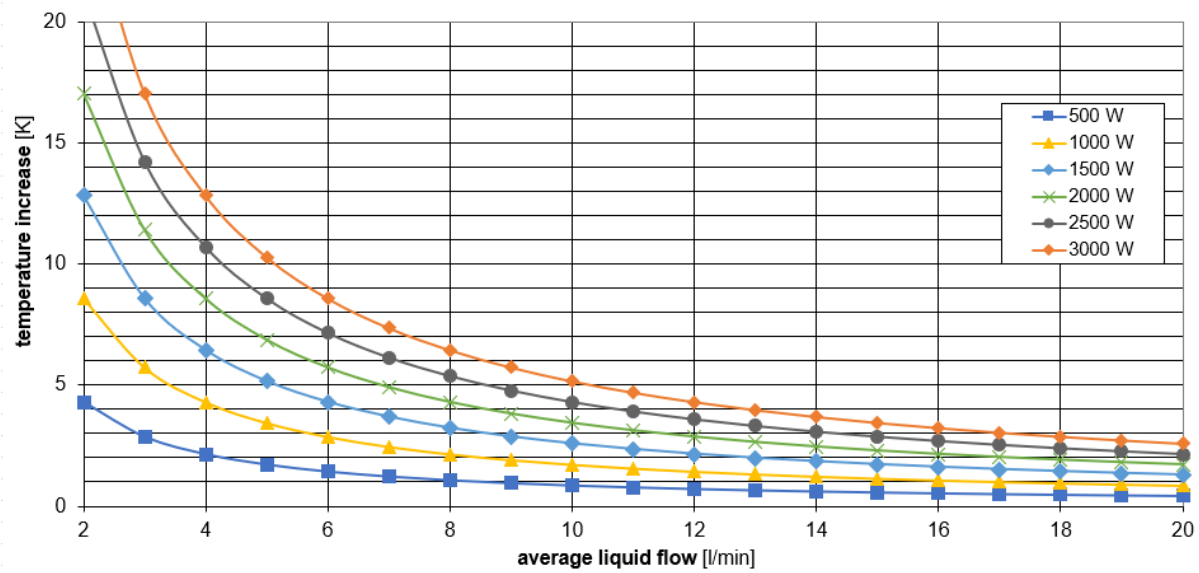


Figure 5.4.30 Temperature difference between water/glycol mixture flowing in/out as a function of the power dissipation and the flow rate, Ta = 25°C, 50% glycol

5.5 References

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[5.3] S. Hopfe, Technical explanation „Thermal Interface Materials" Semikron Danfoss, 2019

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[5.7] R. Eisele, K.K. Olesen, F. Osterwald, "ShowerPower — Brausestrahl versus traditionelle Flüssigkeitskühlung", Elektronik Praxis 10/2008

[5.8] M. Kind, application note AN15-001 "Estimation of Liquid Cooled Heat Sink Performance at Different Operation Conditions", Semikron Danfoss, 2015

6 Thermal Design and Simulation

6.1 Basics of power loss calculation

The functional switches in power electronics (transistors, diodes or thyristors) operating in a switched mode, taking on various static and dynamic states in cycles. Losses occur in the on- and off-states and in the transition between them as soon as current flows and a voltage is applied simultaneously at the semiconductor. The different kind of losses are categorised in Figure 6.1.1. Losses heating up the semiconductor. A suitable power semiconductor rating and cooling measures must be taken to ensure that the maximum junction temperature specified is not exceeded in any time of the converter operation. Exceptions to this are short circuit and surge current events where T_{jmax} is usually exceeded. Such events may, however, happen very seldom during the entire component lifetime. Following such cases, the components must be allowed sufficient time to cool down. In addition to T_{jmax}, lifetime considerations have to be done, because temperature changes and too high power density can limit the expected operational life.

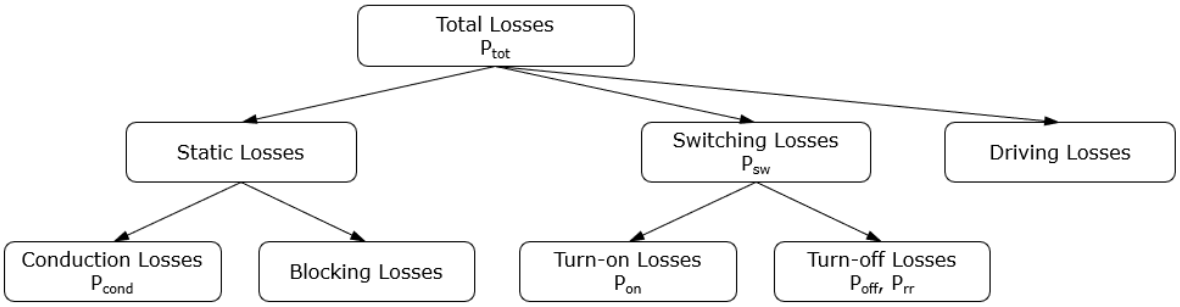


Figure 6.1.1 Overview about power semiconductor losses

Blocking losses are negligible for semiconductors with blocking voltages ≤ 1700V. Driving losses needs to be considered only for low voltage MOSFET and applications with switching frequencies of 100kHz and above. Both are not in the focus of this application manual. Focus is on conduction and switching losses, which dominating in the applications typical for power semiconductors offered by Semikron Danfoss.
Furthermore, it can be distinguished between low frequency (rectifier) applications with mainly only conduction losses and applications with active switched semiconductors in which switching and conduction losses have to be considered. The explanations in this chapter refer to IGBT modules. All of the considerations and calculations can also be applied to MOSFET, provided the designation indices are replaced by those for MOSFET. MOSFET do not have a threshold voltage for the on-state characteristic, meaning that these terms are omitted from formulae (V_{CE0} → V_{DS0} = 0). In reverse mode (freewheeling diode), a differentiation must be made as to whether only the body diode is conductive or whether the MOSFET has also been actively turned on for freewheeling operation in reverse direction.
The formulas given here for power loss and temperature calculation are for a rough estimation of these values and a quick cross-check of the simulation results, which is always recommended. Of course, simulation (see 6.3) is more convenient, offers more options and is the preferred way for loss and temperature calculation.

6.1.1 Rectifier and AC controller

In line rectifiers and thyristor AC controllers are conduction losses dominant, switching losses are neglected. Here, the switching losses at 50Hz are around 1...2% of the conducting losses and are thus covered by the design reserve. Increasing switching losses and the lower temperature ripple at higher frequencies (200…300Hz) compensate one another to some extent. For even higher frequencies, however, current derating is necessary. At 500Hz, for example, additional switching losses of 15…20% must be taken into account in addition the conduction losses. The following general formula is used to calculate the conduction losses as an average value:

$$P_{av} = V_{F0}(T_j) \cdot I_{FAV} + r_F(T_j) \cdot {I_{FRMS}}^2$$

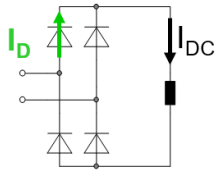
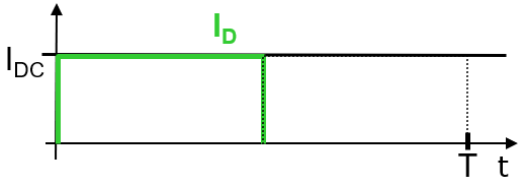
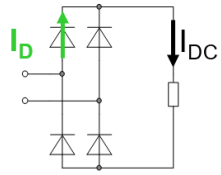
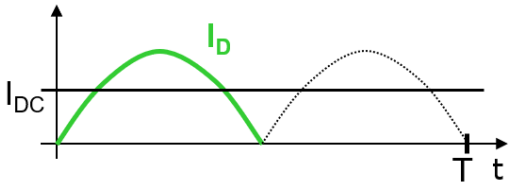
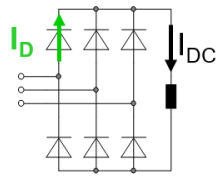
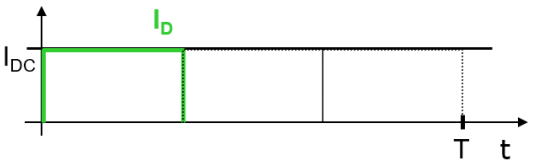
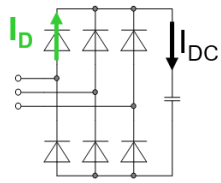
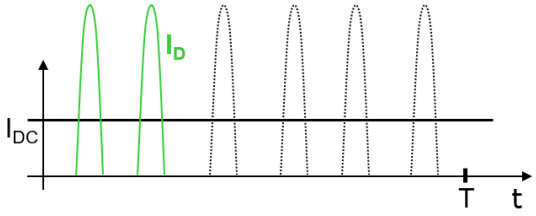
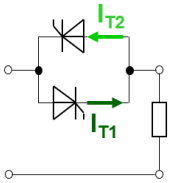
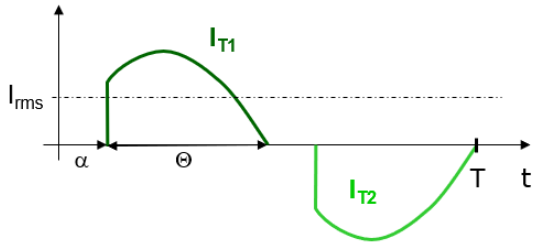
Description	Circuit	Waveform	Formfactor
Single phase, inductive load			$F_i = \frac{\frac{I_{DC}}{\sqrt{2}}}{\frac{I_{DC}}{2}} = \frac{2}{\sqrt{2}} = \sqrt{2}$
Single phase, resistive load			$F_i = \frac{\pi}{2} = 1.57$
Three phase, inductive load			$F_i = \frac{3}{\sqrt{3}} = \sqrt{3}$
Three phase, capacitive load			$F_i = 2 \ldots 2.5$
Single phase, resistive load			$F_i \sim \sqrt{2.5 \cdot \frac{180°}{\Theta}}$

Table 6.1.1 Diode bridge rectifier and AC-controller with different loads, current waveforms and corresponding form factor

For typical current waveforms as shown in Table 6.1.1 it is usual to use a form factor F_i:

$$F_i = \frac{I_{FRMS}}{I_{FAV}}$$

The loss formula for diodes is than simplified to:

$$P_{av} = V_{F0}(T_j) \cdot I_{FAV} + F_i^2 \cdot r_F(T_j) \cdot I_{FAV}^2$$

and for thyristors accordingly:

$$P_{av} = V_{T0}(T_j) \cdot I_{TAV} + F_i^2 \cdot r_T(T_j) \cdot I_{TAV}^2$$

For thyristors the conduction angle Θ varies with phase control. As a guidance a few form factor values are given in Table 6.1.2. But honestly are the cut sinus halfwaves as in the last example of Table 6.1.1 are rarely found in real applications. As soon as an inductance is in the circuit the leading edge is delayed and current is still flowing even if the input voltage becomes negative.

α	30°	60°	90°	120°	150°	165°
Θ	150°	120°	90°	60°	30°	15°
F_i	1.66	1.88	2.22	2.78	3.98	5.65
F_i^2	2.75	3.53	4.93	7.72	15.86	31.93

Table 6.1.2 Form factor values for different conduction angles of thyristors

The forward characteristic of the rectifier is simplified by a line approximation (dashed lines in Figure 6.1.2) for that purpose. The cross point with the x-axis is called V_{F0} for diodes or V_{T0} for thyristors. The slope is the forward resistance r_F respective r_T.

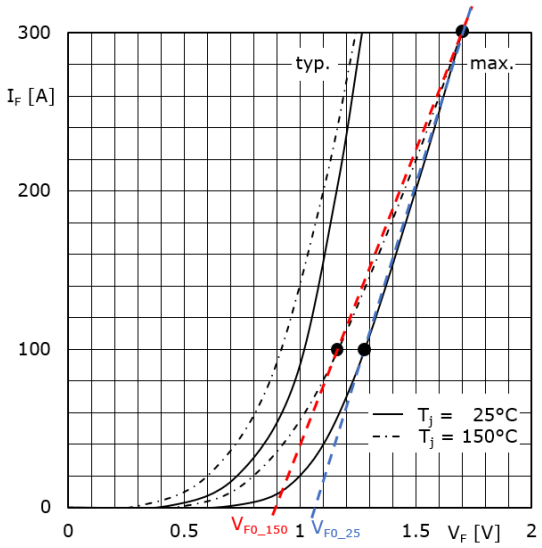


Figure 6.1.2 Forward characteristic of a 100A rectifier diode

For rectifiers it is advantageous to apply the lines at nominal current and 3x nominal current, because in a bridge rectifier the semiconductor is operated in that range. In the example is at 150°C:

$$V_{F0\_150} = 0.9V$$

$$r_{F\_150} = \frac{1.7V - 0.9V}{300A} = 0.00267\Omega$$

A temperature coefficient can be calculated for both parameters using the room temperature and high temperature characteristic (e.g. 25°C and 150°C in Figure 6.1.2). The V_{F0}, V_{T0} and r_F, r_T values can be found in the datasheet tables as well.

$$TC_{VF0} = \frac{V_{F0\_150} - V_{F0\_25}}{\Delta T_j} = \frac{-0.17V}{125K} = -0.00136V/K$$

$$TC_{rF} = \frac{r_{F\_150} - r_{F\_25}}{\Delta T_j} = \frac{0.00057\Omega}{125K} = 4.56 \cdot 10^{-6}\Omega/K$$

$$P_{av} = \left(V_{F0\_25} + TC_{VF0} \cdot (T_j - 25°C)\right) \cdot I_{FAV} + \cdot \left(r_{F_{25}} + TC_{rF} \cdot \left(T_j - 25°C\right)\right) \cdot {I_{FRMS}}^2$$

With this average power dissipation only T_{jav} can be calculated. The actual losses p(t) follow the current waveform and cause a temperature swing with line frequency. The difference between $T_{jmax}(t)$ and T_{jav} is for 50…60Hz applications normally factored in by some safety margin, e.g. by using the maximum forward characteristic instead of typical. Nevertheless, for high F_i-values caused by capacitive load or by large firing angles in thyristor circuits the swing of the virtual junction temperature has to be taken into account when determining the limiting value of the mean forward current. In such cases simulation tools should be used to see the effect on losses and temperatures.

6.1.2 DC/DC converter

Active switched semiconductors like IGBT or MOSFET are used in DC/DC converters and the losses are made up from conduction and switching losses. The formulas here using subscripts for IGBT and freewheeling diode. They also apply for MOSFET, the expression with V_{CE0} in the conduction loss formula disappears.

$$P_{av\_IGBT} = P_{cond\_IGBT} + P_{sw\_IGBT}$$

$$P_{av\_D} = P_{cond\_D} + P_{sw\_D}$$

The forward characteristics are simplified again with a line approximation like shown in Figure 6.1.2 for the rectifier. The only difference is that the line is applied to two points at nominal current and 25% of nominal current to derive V_{CE0} and r_{CE} for the IGBT respective V_{F0} and r_F for the freewheeling diode FWD. Examples for calculation of average and RMS current are given in Table 6.1.3. In the simple case, the current may have a rectangular shape if it flows continuously, or a triangular shape if it does not flow continuously, or it may be composed of such shapes. The formulas to calculate conduction losses for IGBT and FWD in a DC/DC converter are similar to them given for rectifier.

$$P_{cond\_IGBT} = \left(V_{CE0\_25} + TC_{VCE0} \cdot (T_j - 25°C)\right) \cdot I_{CAV} + \cdot \left(r_{CE_{25}} + TC_{rCE} \cdot (T_j - 25°C)\right) \cdot {I_{CRMS}}^2$$

$$P_{cond\_D} = \left(V_{F0\_25} + TC_{VF0} \cdot (T_j - 25°C)\right) \cdot I_{FAV} + \cdot \left(r_{F_{25}} + TC_{rF} \cdot (T_j - 25°C)\right) \cdot {I_{FRMS}}^2$$

The calculation of IGBT and diode conduction losses is based on an ideal duty cycle, no switching times are considered.

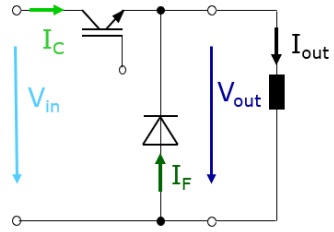
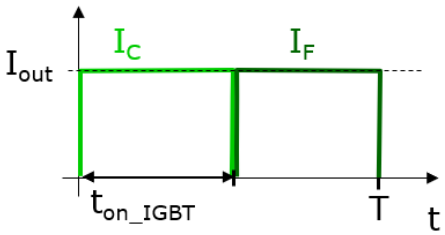
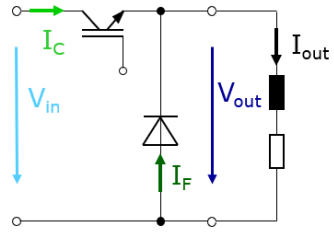
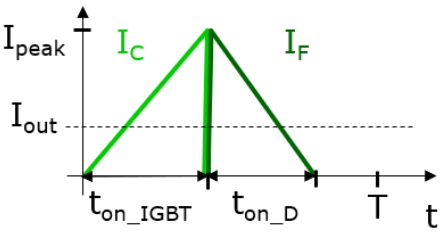
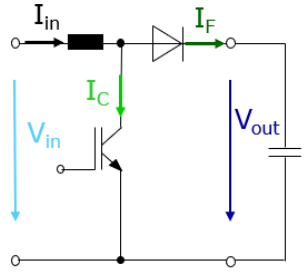
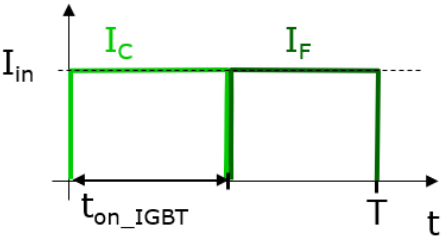
Circuit	**Waveform**	**I_{av}, I_{RMS}**
Buck Converter (Chopper), continuous current (inductive load) 		$I_{CAV} = I_{out} \cdot \frac{t_{on\_IGBT}}{T}$ $I_{CRMS} = I_{out} \cdot \sqrt{\frac{t_{on\_IGBT}}{T}}$ $I_{FAV} = I_{out} \cdot \frac{T - t_{on\_IGBT}}{T}$ $I_{FRMS} = I_{out} \cdot \sqrt{\frac{T - t_{on\_IGBT}}{T}}$ $T = \frac{1}{f_{sw}}$ $E_{on}, E_{off}, E_{rr} = f(I_{out}, V_{in})$
Buck Converter (Chopper), non-continuous current (ohmic inductive load) 		$I_{out} = \frac{I_{peak}}{2} \cdot \frac{t_{on\_IGBT} + t_{on\_D}}{T}$ $I_{CAV} = \frac{I_{peak}}{2} \cdot \frac{t_{on\_IGBT}}{T}$ $I_{CRMS} = \frac{I_{peak}}{2} \cdot \sqrt{\frac{t_{on\_IGBT}}{3 \cdot T}}$ $I_{FAV} = \frac{I_{peak}}{2} \cdot \frac{t_{on\_D}}{T}$ $I_{FRMS} = \frac{I_{peak}}{2} \cdot \sqrt{\frac{t_{on\_D}}{3 \cdot T}}$ $E_{off} = f(I_{peak}, V_{in})$ $E_{on}, E_{rr} = 0$
Boost Converter, continuous current 		$I_{CAV} = I_{in} \cdot \frac{t_{on\_IGBT}}{T}$ $I_{CRMS} = I_{in} \cdot \sqrt{\frac{t_{on\_IGBT}}{T}}$ $I_{FAV} = I_{in} \cdot \frac{T - t_{on_{IGBT}}}{T} = I_{out}$ $I_{FRMS} = I_{in} \cdot \sqrt{\frac{T - t_{on\_IGBT}}{T}}$ $E_{on}, E_{off}, E_{rr} = f(I_{in}, V_{out})$

Table 6.1.3 DC/DC converter circuits, current waveforms and formulas used to calculate losses

In the case of continuous flowing current with rectangular shape it is also common to calculate the conduction losses with the duty cycle DC_{IGBT}.

$$P_{cond\_IGBT} = \left(\left(V_{CE0\_25} + TC_{VCE0} \cdot (T_j - 25°C)\right) \cdot I + \cdot \left(r_{CE_{25}} + TC_{rCE} \cdot \left(T_j - 25°C\right)\right) \cdot I^2\right) \cdot DC_{IGBT}$$

$$P_{cond\_D} = \left(\left(V_{F0\_25} + TC_{VF0} \cdot (T_j - 25°C)\right) \cdot I + \cdot \left(r_{F_{25}} + TC_{rF} \cdot \left(T_j - 25°C\right)\right) \cdot I^2\right) \cdot (1 - DC_{IGBT})$$

with:

DC_{IGBT}:	$\frac{t_{on}}{T}$ (=V_{out}/V_{in} for Buck converter; =1-V_{in}/V_{out} for Boost converter)
I:	Switched current (I_{out} for Buck converter, I_{in} for Boost converter)

Values for switching losses are given at rated conditions (reference values) in the datasheets. They must be converted to the operating point in the circuit. The two basic circuits – step down converter and boost converter - are the basic elements of numerous, more complex applications.

$$P_{sw\_IGBT} = f_{sw} \cdot (E_{on} + E_{off}) \cdot \left(\frac{I}{I_{ref}}\right)^{Ki} \cdot \left(\frac{V}{V_{ref}}\right)^{Kv} \left(1 + TC_{Esw}\left(T_j - T_{ref}\right)\right)$$

$$P_{sw\_D} = f_{sw} \cdot E_{rr} \cdot \left(\frac{I}{I_{ref}}\right)^{Ki} \cdot \left(\frac{V}{V_{ref}}\right)^{Kv} \left(1 + TC_{Err}\left(T_j - T_{ref}\right)\right)$$

f_{sw}:	Switching frequency
I:	Switched current (I_{out} for Buck converter, I_{in} for Boost converter)
V:	Switched voltage (V_{in} for Buck converter, V_{out} for Boost converter)
I_{ref}, V_{ref}, T_{ref}:	Reference values of switching loss measurements in the datasheet
K_i:	Exponent of switching loss current dependency (IGBT~1, FWD~0.6)
K_v:	Exponent of switching loss voltage dependency (IGBT~1.3, FWD~0.6)
TC_{Esw}, TC_{Err}:	Switching loss temperature coefficients (IGBT~0.003/K, FWD~ 0.006/K)

6.1.3 PWM converter

Figure 6.1.3 shows simplified characteristics of an converter phase for a sinusoidal pulse width modulation (PWM).

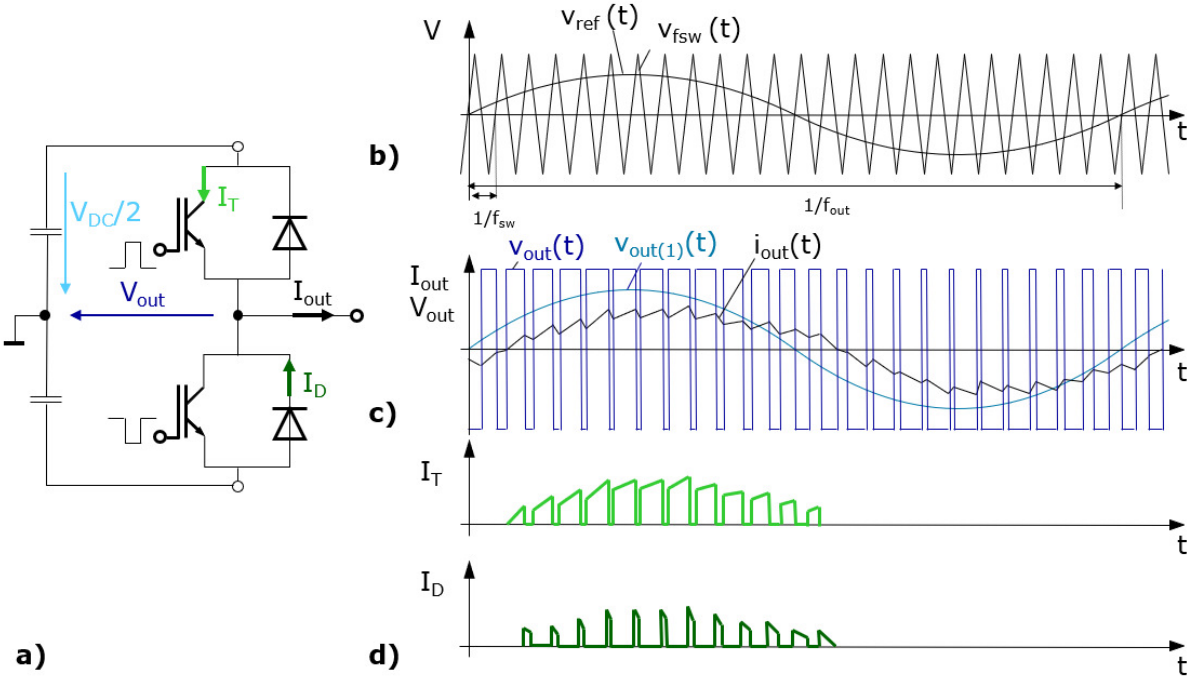


Figure 6.1.3 a) One phase of a PWM converter, b) pulse pattern generation by sinus-delta-comparison, c) output current and pulsed output voltage and first harmonic, d) transistor and diode current of the positive halfwave

According to the classical PWM the pulse pattern is generated by comparing a sinusoidal reference voltage V_{ref} to a delta-shaped control voltage V_{fsw} (Figure 6.1.3 b)). V_{ref} sets the fundamental frequency f_{out} and the control voltage sets the switching or pulse frequency of the switches fsw. The intersections of reference and control voltage trigger a switching event in the converter phase. The TOP switch is ON if $V_{ref} > V_{fsw}$ and OFF in the other case. TOP and BOTTOM switches using inverted signals. Amplitude of V_{ref} determines the amplitude of the output voltage or the degree of converter modulation. Up to a ratio of $V_{ref} = V_{fsw}$ it is called linear modulation, where the modulation factor $m \leq 1$. The modulation factor refers to the virtual neutral point of the load (phase-neutral) and a virtual centre point of the DC link voltage. It expresses the ratio between the fundamental amplitude of the AC voltage (L-GND) and 50% of the DC link voltage.

$$m = \frac{\hat{V}_{out(1)}}{\frac{V_{DC}}{2}}$$

$\hat{V}_{out(1)}$ is the amplitude of the fundamental harmonic of the phase voltage to neutral

Modulation ratios > 1 are possible by overmodulation or injecting higher harmonics, like 3rd harmonic in space vector modulation (SVPWM).
The phase shift between the fundamental harmonics of AC current and voltage is described by the angle φ. In inverter mode (energy flow from DC to AC) $\cos(\varphi) > 0$ applies; in rectifier mode (energy flow from AC to DC) $\cos(\varphi) < 0$ applies, i.e. it is negative.
The current and voltage waveforms for TOP-IGBT and BOTTOM-diode will turn out to be identical compared to BOTTOM-IGBT and TOP-diode but time shifted by 180° due to the symmetrical structure of the converter circuit. It is therefore enough to consider just one IGBT and one diode with regard to loss evaluations. Inverter losses can then be determined by multiplying the result by the corresponding number of IGBT/diodes (4 - single-phase or 6 - three-phase). In contrast to the calculations made in chapter 6.1.2, duty cycle, load current and junction temperature are not constant under static circuit conditions, but vary depending on the fundamental frequency of the AC side (e.g. 50Hz). This means that the switching losses and on-state power dissipation of IGBT and diodes vary in time and call for a more in-depth analysis of system power losses. Precise results can thus only be expected insofar as the simplifications made are applicable, or deviations are still acceptable [6.2].
The following simplifications are assumed:

- switching times and dead time t_d between TOP/BOT-switch are neglected;
- junction temperatures are nearly constant during one period (permissible f_{out} = ~ 50Hz);
- linear modulation;
- the switching frequency ripple of the output current (sinusoidal) is neglected $f_{sw} >> f_{out}$;

The voltage-time area of $2 \cdot t_d \cdot V_{DC}/2$ multiplied with f_{sw} would be missing in the output voltage. A controller will balance the missing voltage by lengthening the control pulses, so that the voltage required to obtain the desired current value is also present at the inverter output. The calculation of the modulation factor m from the output voltage allows for t_d to be omitted as a source of error. Conventional PWM will switch at the maximum number of possible commutation points in time, thus causing a maximum of switching losses. Other control methods can omit selected switching events, thus showing lower switching losses than calculate using the formulae below. The linearization of the IGBT output characteristic using line approximation results in the following expression for the temporal correlation of the saturation voltage v_{CEsat}:

$$v_{CEsat}(i,t) = V_{CE0} + r_{CE} \cdot i(t) = V_{CE0} + r_{ce} \cdot \hat{I} \cdot \sin(\omega \cdot t)$$

The solution of the integral

$$p(t) = \int_0^T v_{ce}(i,t) \cdot i(t) dt$$

leads for the conduction losses of the IGBT to

$$P_{cond\_IGTB} = \left(\frac{1}{2\pi} + \frac{m \cdot \cos(\varphi)}{8}\right) \cdot V_{CE0}(T_j) \cdot \hat{I} + \left(\frac{1}{8} + \frac{m \cdot \cos(\varphi)}{3\pi}\right) \cdot r_{ce}(T_j) \cdot \hat{I}^2$$

$$V_{CE0}(T_j) = V_{CE0_{25}} + TC_{VCE0} \cdot (T_j - 25°C)$$

$$r_{ce}(T_j) = r_{CE_{25}} + TC_{rCE} \cdot (T_j - 25°C)$$

and for the diode

$$P_{cond\_D} = \left(\frac{1}{2\pi} - \frac{m \cdot \cos(\varphi)}{8}\right) \cdot V_{F0}(T_j) \cdot \hat{I} + \left(\frac{1}{8} - \frac{m \cdot \cos(\varphi)}{3\pi}\right) \cdot r_f(T_j) \cdot \hat{I}^2$$

The solution for the switching losses is simple as long as the switching losses are linear dependent from the current. For nonlinear dependencies a product sum remains in the formula which is also called a "Gamma function" (γ). Linear dependency can be assumed with an acceptable error for the IGBT (K_i=1 → γ=2).

$$P_{sw\_IGBT} = f_{sw} \cdot (E_{on} + E_{off}) \cdot \frac{1}{2\pi} \cdot \left(\frac{\hat{I}_{out}}{I_{ref}}\right)^{K_i} \cdot \left(\frac{V_{DC}}{V_{ref}}\right)^{K_v} \cdot \left(1 + TC_{Esw} \cdot (T_j - T_{ref})\right) \cdot \underbrace{\int_0^{\pi} \sin^{K_i}(\alpha) d\alpha}_{\gamma(K_i)}$$

$$P_{sw\_D} = f_{sw} \cdot E_{rr} \cdot \frac{1}{2\pi} \cdot \left(\frac{\hat{I}_{out}}{I_{ref}}\right)^{K_i} \cdot \left(\frac{V_{DC}}{V_{ref}}\right)^{K_v} \cdot \left(1 + TC_{Err} \cdot (T_j - T_{ref})\right) \cdot \underbrace{\int_0^{\pi} \sin^{K_i}(\alpha) d\alpha}_{\gamma(K_i)}$$

$\hat{I}_{out}$	is the amplitude of the fundamental harmonic of the phase current
I_{ref}, V_{ref}, T_{ref}	Reference values of the switching loss measurements in the data sheet
K_i:	Exponent of switching loss current dependency (IGBT~1, FWD~0.6)
K_v:	Exponent of switching loss voltage dependency (IGBT~1.3, FWD~0.6)
TC_{Esw}, TC_{Err}:	Switching loss temperature coefficients (IGBT~0.003/K, FWD~ 0.006/K)
γ(K_i):	numerical solution of gamma function =2(K_i=1); =2.3 (K_i=0.6)

For a numerical solution and especially in case that the boundary condition "junction temperatures are temporally constant" is not valid anymore (e.g. at low inverter output frequencies) a different approach should be used. The 360deg of a period of the output frequency are divided into small segments. Within one segment the current and the duty cycle DC_{IGBT}, DC_D (conduction time) is constant (see Figure 6.1.4). This allows the usage of the formulas of the Buck converter for conduction and switching losses (see 6.1.2).

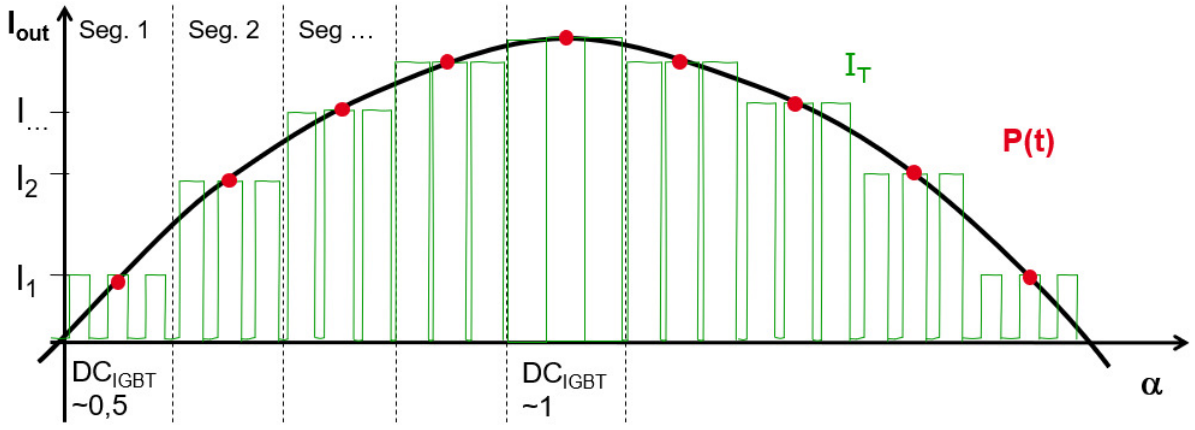


Figure 6.1.4 Calculation of the losses for an inverter period as a function of time p(t) with an example for m=1 and cos(φ)=1

$$p_{cond_{IGBT}}(t) = \left(\left(V_{CE0\_25} + TC_{VCE0} \cdot (T_j(t) - 25°C)\right) \cdot i_n + \cdot \left(r_{CE_{25}} + TC_{rCE} \cdot \left(T_j(t) - 25°C\right)\right) \cdot {i_n}^2\right) \cdot DC_{IGBT_n}$$

The duty cycle for each segment varies with the angle α.

$$DC_{IGBT_{(1\ldots n)}} = f(m, \alpha) = \frac{t_{on\_IGBT(segment\ 1\ldots n)}}{T_{sw}} = \frac{1}{2} \cdot (1 + m \cdot \sin(\alpha))$$

$$p_{sw_{IGBT}}(t) = f_{sw} \cdot (E_{on} + E_{off}) \cdot \left(\frac{i_n}{I_{ref}}\right)^{Ki} \cdot \left(\frac{V}{V_{ref}}\right)^{Kv} \left(1 + TC_{Esw}\left(T_j(t) - T_{ref}\right)\right)$$

$$p_{IGBT}(t) = p_{cond_{IGBT}}(t) + p_{sw_{IGBT}}(t)$$

Instead of multiplying the switching energies with normalized current and voltage operators it is also possible to use lookup tables with $E_{on,off} = f(i,v)$. Conduction and switching losses for the FWD diode are calculated in the same way.
A parametric study has shown, that with 60 segments (6deg) almost no difference in losses and temperatures can be seen compared to a continuous calculation of each physical pulse with PWM frequency. The result of this segment wise calculation is the power dissipation as a function of time p(t) and with this it is possible to calculate the junction temperature ripple caused by the inverter output frequency and even T_j during 0Hz operation.

6.2 Calculating the virtual junction temperature

6.2.1 Thermal equivalent circuits

The terms 'thermal resistance' and 'thermal impedance' have already been explained in chapter 3.2.3. This section deals with the types of modelling only. Even in times of high computer performance and finite element simulation, simple equivalent circuits are still widely used. In many cases is the calculation of junction temperatures based on simplified thermal equivalent circuit diagrams (Figure 6.2.1) in which three-dimensional structures are mapped to one-dimensional models. This will inevitably result in errors, since thermal connections between different components inside one housing or on one heatsink are dependent on time as well as on the electric operating point of the components (e.g. distribution of losses between diode and IGBT). More complex models with a matrix composed of coupling elements are impractical and difficult to parameterise [6.1]. If such effects have to be considered more closely, FEM simulations are preferred to the analytical approaches presented here.

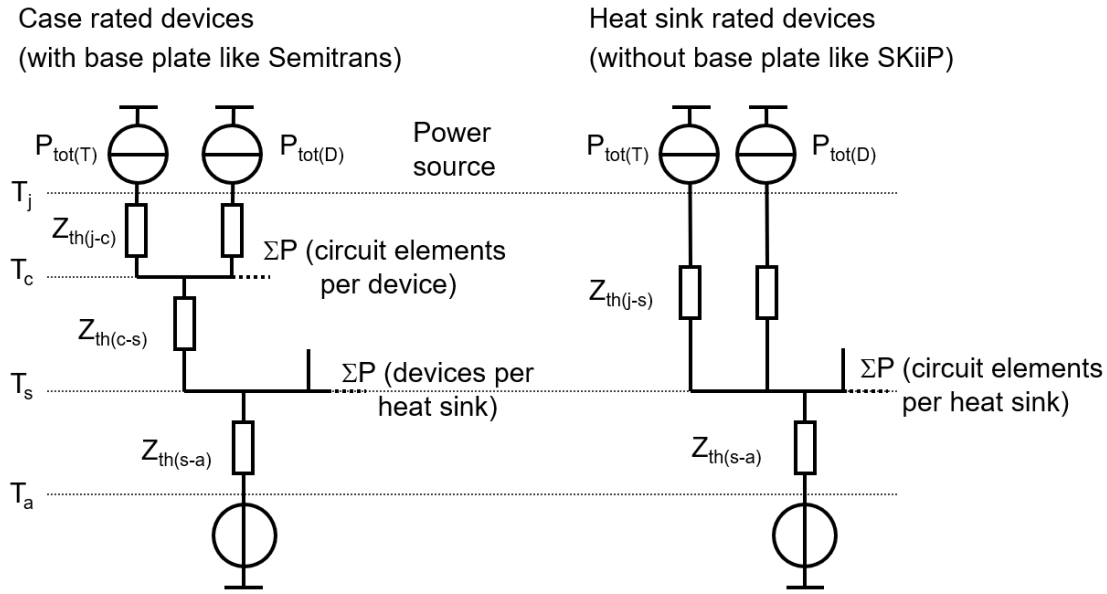


Figure 6.2.1 Simplified thermal equivalent circuit diagram of IGBT and freewheeling diode in a power module: for module with copper base plate (left), for module without base plate (rigth).

To obtain thermal equivalent circuit diagrams, electrical analogies to thermal parameters are used. The sources of power dissipation $P_{tot(T/D)}$ correspond to current sources, constant temperature levels are represented by voltage sources and RC elements are used to represent the thermal impedances $Z_{th(x-y)}$.
In power modules with base plate, the transistor and inverse diode are soldered onto a common copper substrate, thus being thermally coupled. For the purpose of simplification, we assume a common case temperature. The losses of all internal components in the module must be dissipated through the thermal impedance $Z_{th(c-s)}$ (Figure 6.2.1 left). IGBT losses will heat the base plate and thus the diode, too, even if the diode itself does not produce any losses. Several modules on one heatsink will all contribute to heat up the heatsink, meaning that we also assume a uniform heatsink temperature in this case.

Modules without base plate have a low thermal coupling inside the module. We can assume a common heatsink temperature in that case (Figure 6.2.1, right). Component losses are directly dissipated to the heatsink, meaning that, together, all of the components heat up the heatsink. This simplification produces always failures because there are baseplate modules with switches of 2cm distance or more and without thermal coupling and on the other hand modules without baseplate and only 1mm distance with strong thermal coupling. As a rule of thumb, we can assume that the thermal coupling disappears if the distance is greater than 3x the thickness of the materials underneath. For example, 1mm DBC + 3mm copper baseplate = 4mm, means the distance should be greater than 12mm. It depends also on the cooling system.
Since T_s is measured at a certain point in order to determine $\Delta T_{(s\text{-}a)}$, the value for $R_{th(s\text{-}a)}$ only applies to this measuring point (see chapter 5.2.4). Other measuring points will result in different values. To simplify analysis, a uniform heatsink temperature for all components is often assumed in layouts containing several modules. Losses occurring in all of the heat sources on the heatsink are dissipated through the common $R_{th(s\text{-}a)}$.
Two equivalent circuit diagrams are quite common when mapping thermal impedance: the ladder-type "physical" equivalent circuit diagram (Figure 6.2.3, left, "Cauer network") and the chain-type "mathematical" equivalent circuit diagram (Figure 6.2.3, right, "Foster network"). At first glance, both types are equally useful. If a step-function response in a black box were "measured", it wouldn't be possible to determine which of the equivalent circuit diagrams was used (Figure 6.2.2).

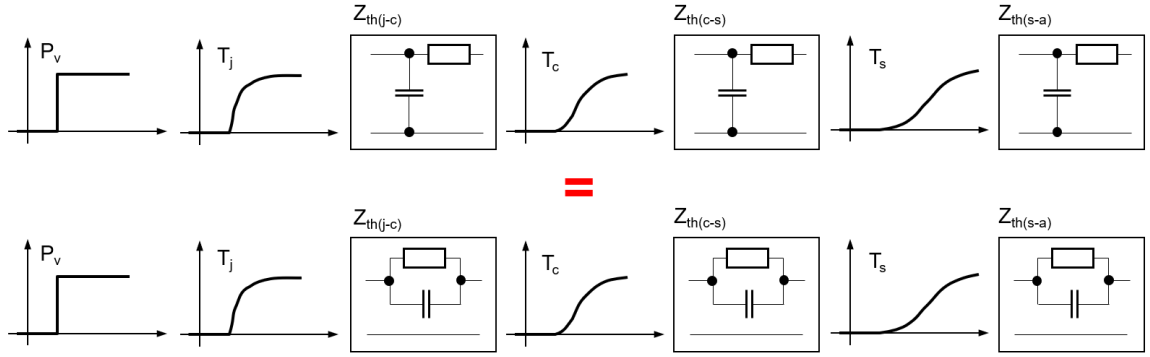


Figure 6.2.2 Mapping thermal impedance with the aid of equivalent circuit diagrams

The smallest error is produced in subsequent calculations if the entire system is measured in one shot as a complete system. The time-dependent temperature differences of T_j, T_c, T_s and T_a can be used to determine the blocks for thermal impedances $Z_{th(j\text{-}c)}$, $Z_{th(c\text{-}s)}$ and $Z_{th(s\text{-}a)}$, which are represented as four poles. To obtain a ladder-type equivalent circuit diagram, the geometrical dimensions and material properties are employed. Subsequent adjustments are often necessary in order to adapt the calculated functions to the measured results. In this way, the physical relation gets somewhat lost. To obtain the chain-type equivalent circuit diagram, the factors and time constants for the exponential function are determined by means of formula manipulation.

$$Z_{th(x-y)} = R_{th1} \cdot \left(1 - e^{\frac{-t}{\tau_{th1}}}\right) + R_{th2} \cdot \left(1 - e^{\frac{-t}{\tau_{th2}}}\right) + \cdots + R_{thn} \cdot \left(1 - e^{\frac{-t}{\tau_{thn}}}\right)$$

The number n of summands and the values for R_{thn} and T_n are chosen such that a sufficient approximation of the curve shape can be produced with a reasonable amount of calculations involved, irrespective of the physical structure. The basis for determining values of R_{th} and T_{th} is the existing (measured) Z_{th} curve. Mathematical programs and spreadsheets such as Excel (→ Solver) are able to solve equation systems with a large number of unknown elements by setting the sum of error squares to zero (0) for a large number of interpolation nodes, as shown in the following equation.

$$\left(Z_{th(x-y)}(t_n) - \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-t_n}{\tau_\nu}}\right)\right)^2 = 0$$

In order to rule out absurd solutions, a constraint must define R_{th} and $T_{th} > 0$. The number of R_{th}/T_{th} pairs can be increased until the desired accuracy has been achieved.
The main advantage of the exponential function is that it can be easily used for temperature calculation, the formula can be solved in one step analytical. Semikron Danfoss specifies the power module parameters for $Z_{th(j\text{-}c)}$ or $Z_{th(j\text{-}s)}$ in the form of 2 to 6 R_{th} and T_{th} elements.

It is possible for both equivalent circuits to line up the sub-blocks determined in the overall system and determine the intermediate temperatures T_c, T_s. Where things go wrong, however, is when one block from the chain of thermal impedances is to be replaced by another. Heat spreading produces feedback to the preceding blocks. For example, this is the case if parameterisation has been done on a very good water cooler and in the real application the component is mounted on a poor air cooler. Nevertheless, for the sake of simplicity, $Z_{th(s-a)}$ is still often replaced by the user of power modules. Because in the application is a different heatsink used than for the product qualification. A reason why it can be done is the high difference in the time constants of a power module and a heatsink.

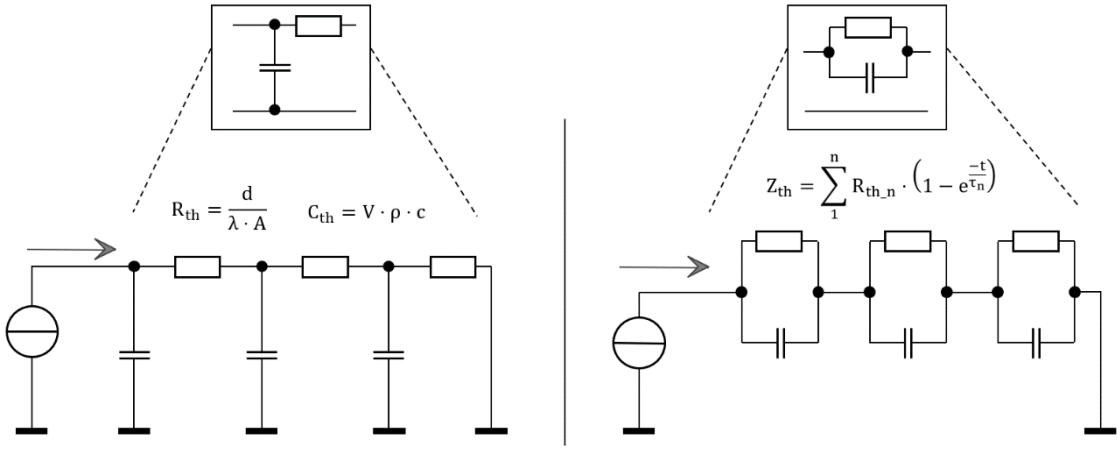


Figure 6.2.3 Representation of the four-pole blocks as a thermal equivalent circuit; left: ladder-type "physical" equivalent circuit diagram (Cauer network); right: chain-type "mathematical" equivalent circuit diagram (Foster network)

Notes on the use of the Foster network:

- The nodes in the network in Figure 6.2.3, right do not represent system temperatures.
- The R and C elements cannot be assigned to any physical components.
- The sequence of the RC elements within a block can be interchanged.
- They cannot be connected in series with a resistance.
- Do not think physically, like "the TIM layer is a 2-dimensional contact resistance and has no capacity", true is that the temperature difference $\Delta T_{(c-s)}$ has a large time constant and therefor a large capacity in the equivalent circuit $Z_{th(c-s)}$

6.2.2 Models with coupled networks

In some cases, are the simplifications of the above-mentioned equivalent networks not allowed. Especially if operating conditions with very uneven loss distribution between switches have to be considered. This is for example the case with 0Hz operation of a three-phase converter in which one switch can operate continuously at the peak of the output current.
In order to justify the higher effort through better accuracy, the measurements should be carried out in the final converter system consisting of a power semiconductor module and heat sink. In Figure 6.2.4 an example of a model for an IGBT halfbridge is shown. The Z_{th} values are measured in reference to a built in T-sensor. One switch (e.g. $IGBT_{TOP}$) is heated up by a DC current and after switching off the self-impedance $Z_{th(j-r)I\_TOP}$ and the coupling impedances to the 3 other switches is measured. $Z_{th(j-r)D\_BOT-I\_TOP}$ represents the temperature increase of the BOT diode caused by the TOP IGBT. The procedure is repeated for the other three switches in turn. In the model represents the voltage source a temperature difference caused by the losses of another switch multiplied by the coupling impedance. The coupling can be negative, if for example the losses of the TOP-IGBT reduce the temperature difference $\Delta T_{(j-r)}$ for the BOT-IGBT.

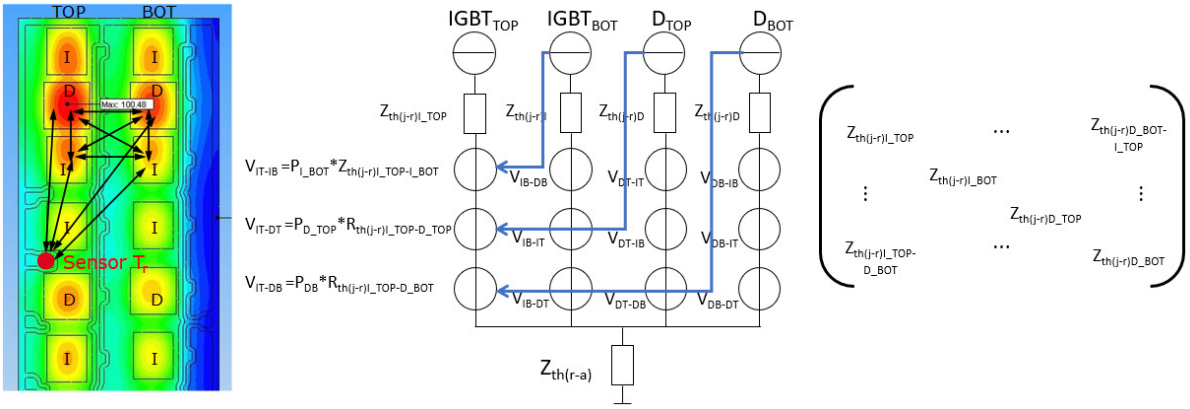


Figure 6.2.4 Example of a full coupled model for an IGBT halfbridge with reference to a built in temperature sensor

6.2.3 Stationary conditions

After losses have been calculated, temperatures during stationary operation can be calculated using the thermal resistances R_{th} (= final value of the Z_{th} curves). Temperature calculation is performed starting with the ambient temperature from the outside to the inside (Figure 6.2.5).

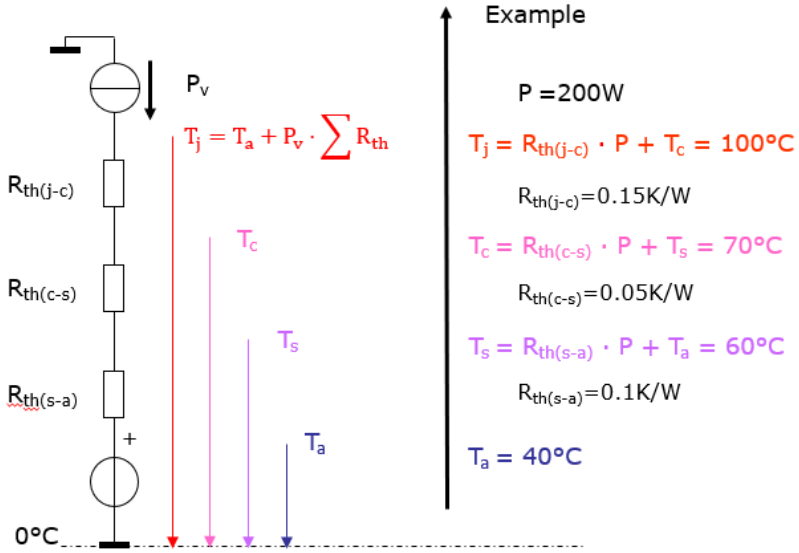


Figure 6.2.5 Temperature calculation under stationary conditions

If there is more than one source of power loss on a heatsink, the individual losses of all n_1 components are added up (e.g. 6 IGBT and 6 freewheeling diodes of a 3-phase converter); this total loss is used to calculate the heatsink temperature.

$$T_s = n_1 \cdot (P_{IGBT} + P_D) \cdot R_{th(s-a)} + T_a$$

Modules with base plate show good thermal coupling between their components, the thermal resistance $R_{th(c-s)}$ is specified for the entire module, which is why all sources of power loss n_2 in the module are added up to calculate the case temperature (e.g. 2 IGBT and 2 freewheeling diodes in a halfbridge module):

$$T_c = n_2 \cdot (P_{IGBT} + P_D) \cdot R_{th(c-s)} + T_s$$

This way of modelling can result in too high temperatures if for example in a half-bridge module just one IGBT and its spatially separated freewheeling diode is used, or if IGBT and parallel inverse diode are close by but produce losses time-shifted. If $R_{th(c-s)}$ is only specified for a single component (e.g. the IGBT), the thermal coupling of the copper base plate with the inverse diode is neglected. In this case, modelling in combination with simultaneous losses in IGBT and diode will produce an error with temperatures that are too low.
The junction temperature is finally calculated from the losses of the single component and its thermal resistance to the case for modules with base plate, or to the heatsink for modules without base plate. For IGBT this is, for example:

$$T_{j\_IGBT} = P_{IGBT} \cdot R_{th(j-c)} + T_c$$

$$T_{j\_IGBT} = P_{IGBT} \cdot R_{th(j-s)} + T_s$$

All semiconductor losses are temperature-dependent, meaning that chip temperature and losses are coupled. In the simplest case, losses are calculated at the maximum junction temperature. This will ensure that you are on the safe side, since most losses increase with temperature. In an improved procedure, losses are determined iteratively at the calculated T_j. For this loop that can easily be programmed, the starting value is the power dissipation at ambient temperature (Figure 6.2.6). This value allows for an initial approximation of the junction temperature. At this temperature, a new, more precise loss value is produced. After 3 to 4 iterative loops, the final value will have been reached in most cases.

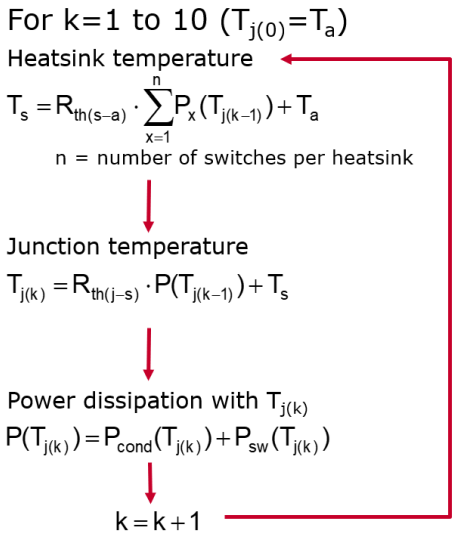


Figure 6.2.6 Loop used to calculate temperature-dependent semiconductor losses for a module without base plate

6.2.4 Junction temperature as a function of time with different load pulses

6.2.4.1 Single pulse

Higher current loads are permitted during short-time operation of the power semiconductors than specified in the datasheets for continuous operation. What must be ensured here, however, is that the maximum junction temperature under the defined conditions does not exceed the limit value for T_{jmax}. T_j is calculated with the aid of the thermal impedance Z_{th}. For pulses in the millisecond range, it is sufficient for $Z_{th(j-c)}$ to be considered at a constant case temperature Tc. In the range up to 1s, it is possible to work with the module impedance $Z_{th(j-s)} = Z_{th(j-c)} + Z_{th(c-s)}$ and constant heatsink temperature. In longer pulse sequences, the total impedance $Z_{th(j-a)} = Z_{th(j-s)} + Z_{th(s-a)}$ should be used.

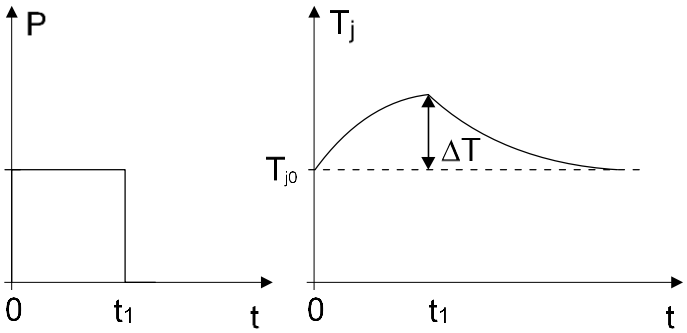


Figure 6.2.7 Time curve of power dissipation and junction temperature in the event of a single power dissipation pulse

The junction temperature change at the moment t_1 at the end of a single power dissipation pulse is calculated by:

$$\Delta T_j(t_1) = P \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-t_1}{\tau_\nu}}\right)$$

The following applies to the junction temperature curve during the cooling phase:

$$\Delta T_j(t > t_1) = P \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-t_1}{\tau_\nu}}\right) - P \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-(t-t_1)}{\tau_\nu}}\right)$$

The ΔT_j is mend as a temperature difference to a fixed reference temperature, e.g T_s using $Z_{th(j-s)}$ in that case.

6.2.4.2 Sequence of different load pulses

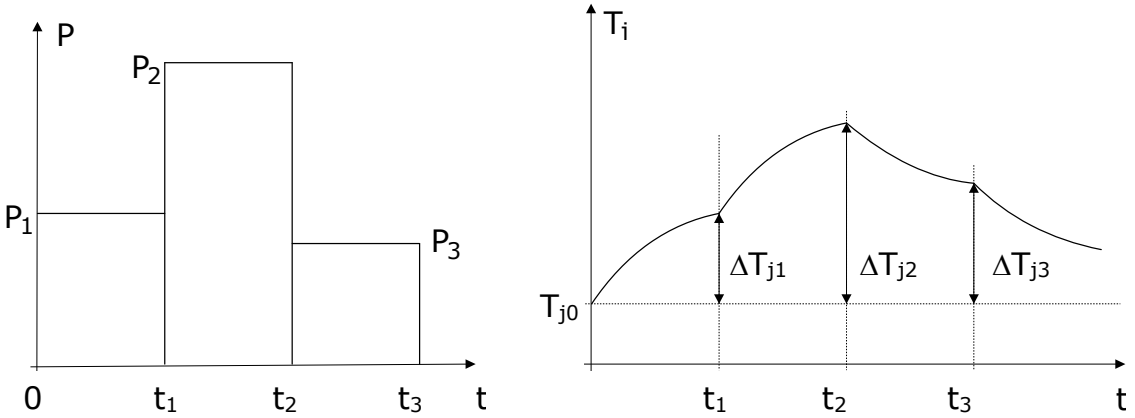


Figure 6.2.8 Junction temperature as a function of time for a sequence of 3 power dissipation pulses.

The junction temperature change at the moment t_1 is to be calculated in the same way as for the single pulse. For a junction temperature change at the moment t_2, the following applies:

$$\Delta T_j(t_2) = P_1 \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-t_2}{\tau_\nu}}\right) + (P_2 - P_1) \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-(t_2-t_1)}{\tau_\nu}}\right)$$

The understanding is that P_1 is applied ongoing till t_2 and a second pule of power dissipation with the magnitude of P_2-P_1 is starting at the time t_1. This is repeated for any following load pulse. Junction temperature difference to a reference temperature at the moment t_m is calculated with:

$$\Delta T_j(t_m) = \sum_{\mu=1}^{m} (P_\mu - P_{\mu-1}) \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \left(1 - e^{\frac{-(t_2-t_1)}{\tau_\nu}}\right)$$

6.2.4.3 Series of equal load pulses

A special case is a sequence of equal load pulses like in a S2 operation of a drive (Figure 6.2.9). The average junction temperature T_{jav} results from the product of stationary heat resistance $R_{th(j-a)}$ and the average total loss $P_{av} = P_{pulse} \cdot t_p/T$. This value is obtained by averaging the power dissipation per pulse over the entire length of a period T.

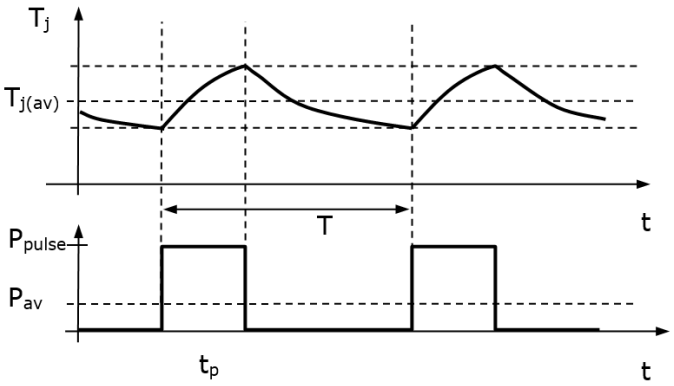


Figure 6.2.9 Temperature and losses of a periodic load

The maximum junction temperature at the end of the loss pulse $P(t_p)$ results from

$$\Delta T_j(t_p) = P_{pulse} \cdot \sum_{\nu=1}^{n} R_{th\nu} \cdot \frac{\left(1 - e^{\frac{-t_p}{\tau_\nu}}\right)}{\left(1 - e^{\frac{-T}{\tau_\nu}}\right)}$$

Which temperature difference and therewith which Z_{th} has to be considered depends on t_p. $Z_{th(j\text{-}c)}$ is sufficient for times less than 100ms, adding a temperature difference to a constant case temperature. For less than a few seconds $Z_{th(j\text{-}s)}$ has to be used and for longer durations $Z_{th(j\text{-}a)}$.

6.2.4.4 Mission profiles

Theoretically a mission profile could be divided into a large number of power pulses with different magnitude and the formula from 6.2.4.2 is used to calculate T_j. The failure would depend on the granularity of the pulse sequence division. For several hundred time steps the formula becomes huge and the computing time long. A mission profile consists often of tens or hundreds of thousands time steps which is not solvable with these equations anymore.
Therefore, a different approach is used, in which only the change of the temperature across the thermal capacity of Foster-element x (Figure 6.2.10) is calculated from timestep m to the following timestep m+1:

$$\Delta T_{jx}(t_{m+1}) = \Delta T_{jx}(t_m) \cdot e^{\left(\frac{-\Delta t_m}{Tau_x}\right)} + R_{thx} \cdot P_{IGBT}(t_{m+1}) \cdot \left(1 - e^{\left(\frac{-\Delta t_m}{Tau_x}\right)}\right) \qquad |x = 1 \dots n$$

$$\Delta T_{j-ref} = \sum_{x=1}^{n} \Delta T_{jx}$$

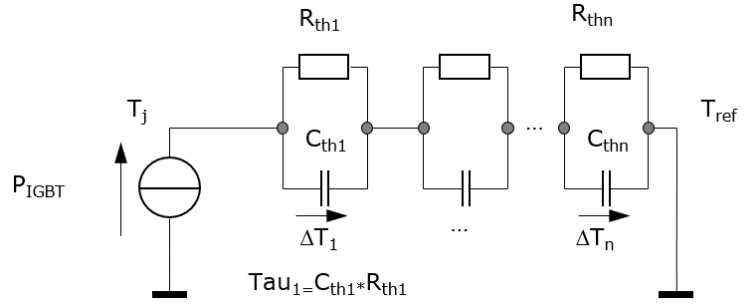


Figure 6.2.10 Schematic of the Foster-elements of a thermal impedance between junction and a reference point

The temperature difference a time "m+1" is stored may be used as input for the loss calculation at t=m+2 and temperature at t=m+2 is calculated. In this way an ongoing time function of $T_j(t)$ is calculated and the complete history is implemented in the voltage across the capacity. The formula becomes even more simple with constant time steps Δt_m because than the exponential function becomes a constant value and the formula is simplified to

$$\Delta T_{jx}(t_{m+1}) = \Delta T_{jx}(t_m) \cdot K_1 + R_{thx} \cdot P_{IGBT}(t_{m+1}) \cdot (1 - K_1) \qquad |x = 1 \dots n$$

6.2.5 Junction temperature at fundamental frequency

The calculation of the junction temperature determined by the fundamental frequency of the converter output current is only efficient if performed using computer-aided methods. Both thermal system and electrical system equations have to be solved iterative in stacked loops in order to calculate T_j over a sine half-wave. Figure 6.2.11 shows $p_{IGBT}(t)$ and the average power dissipation in an IGBT, as well as the resulting junction temperature characteristics for different fundamental output frequencies as the result of a simulation ("→0Hz" stands for "approaching 0Hz").

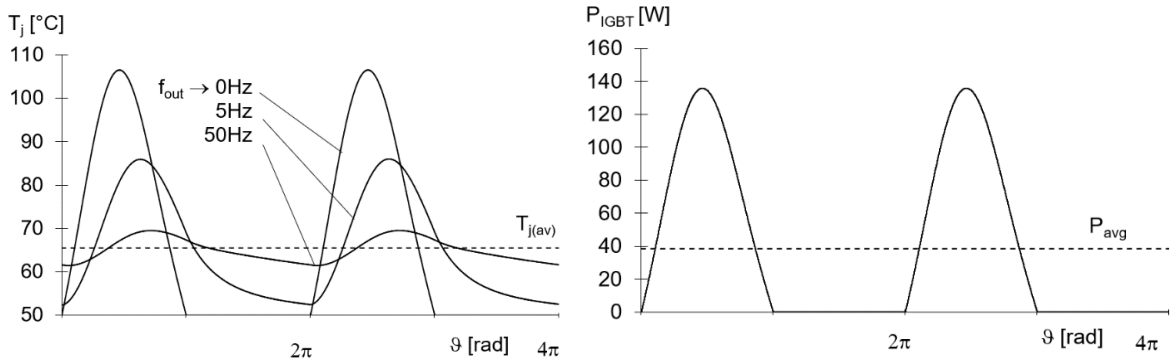


Figure 6.2.11 Simulated junction temperature and power dissipation characteristics of a 1200V, 50A IGBT in inverter mode for different fundamental output frequencies; [6.1] V_{DC} = 540V; I_{1RMS} = 25A, f_{sw} = 8kHz; cos(φ) = 0.8; m = 0.8; T_s = 50°C

In this example, the maximum junction temperature exceeds the average value by just about 4…5K at a frequency of 50Hz. For low frequencies $T_{j(av)}$ is no longer permitted to determine the thermal layout of the system because of its far higher maximum value. Therefore, the minimum frequency at rated power output is a critical parameter for converters besides overcurrent. When the frequency decreases, the maximum temperature will rise despite constant mean losses. An explanation for this is the fact that the thermal time constants of power semiconductors are below one second and thus within the range of normal converter output frequencies. When frequencies are high, the thermal capacitances of the semiconductor (case) still average the temperature characteristic. When frequencies are low (2 →0Hz), the junction temperature follows the power dissipation. This results in high temperature swings around the mean temperature. Consequently, the permissible output current RMS value for a defined power module will decrease with lower frequencies.
A particularly critical case with regards to the thermal stress of power modules is the voltage- and frequency-controlled starting process of a three-phase motor drive supplied by an converter. Figure 6.2.12 shows a simulated example.

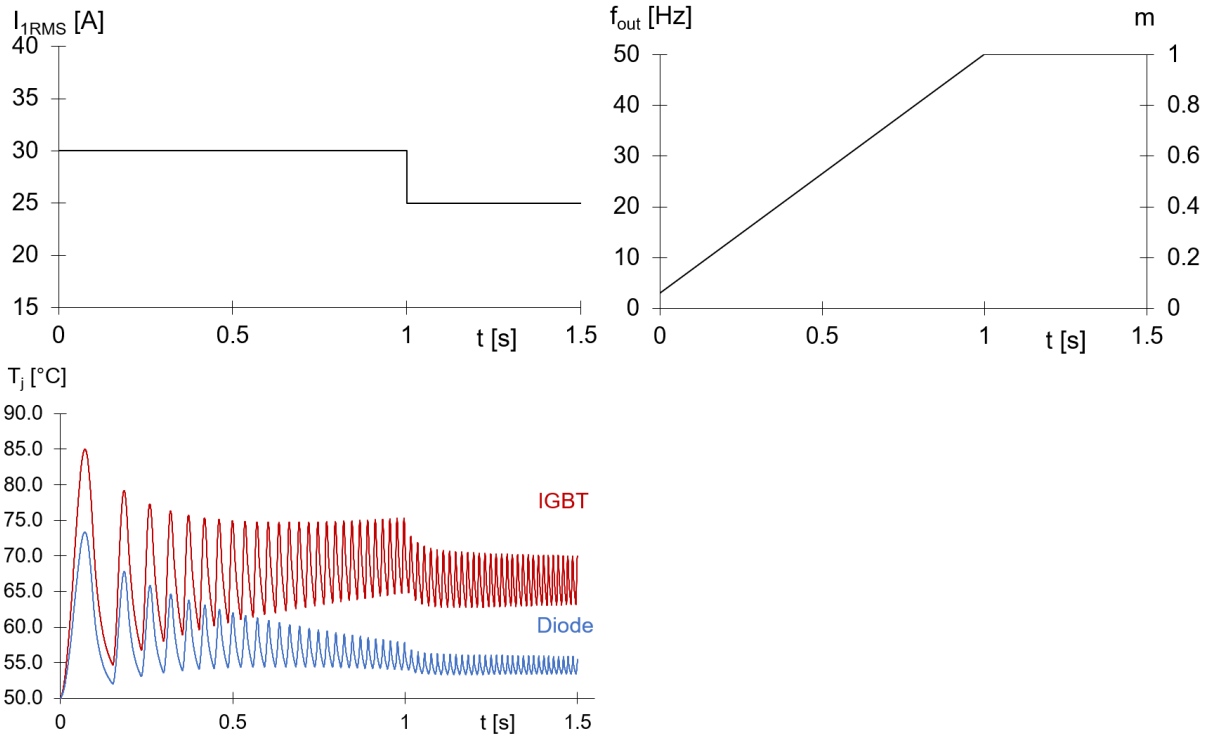


Figure 6.2.12 Starting process of a three-phase motor drive (parameters as in Figure 6.2.11) [6.1]

In some application (electrical cars, cranes, robots) inverter operation at an output frequency of f_{out} = 0Hz can be a limiting case. The use of calculated average values of a period is no longer permitted because the period is infinite at f = 0Hz. "Infinite" applies if the dwell time in this condition is far greater than the thermal time constants of the system. Besides of the not valid formula definition, it is extremely problematic to generally assume an even distribution of losses on the heatsink, whereas in this case it is only one of the 6 switches that produces the major part of the losses. Theoretically, one switch might switch a direct current at the very moment when the current and losses reach their maximum. The thermal model of Figure 6.2.3 with a common heatsink node for the three-phase converter is also no longer valid.
The loss calculation $p_{IGBT}(t)$ from chapter 6.1.3/Figure 6.1.4 and the temperature calculation of chapter 6.2.4.4 can be combined to calculate the temperature swing caused by the inverter output frequency or even 0Hz operation. The thermal model should be adapted to a single switch $Z_{th(j-a)}$ or cross couples model like in chapter 6.2.2.

6.3 Software SemiSel®

6.3.1 Software philosophy, simulator basics and model structure

As a service to support customers with product selection and loss and temperature calculations the former SEMIKRON has introduced the free software program SemiSel to its homepage [6.3] to enable customers to perform numerous simulations with power electronic switches under a wide range of operating conditions. This program went live in 2001 and has been continually expanded and improved since then. The description below refers to the functions included in version 5 of the program. SemiSel is a Web-Browser based simulator.
The software can be used as an anonymous or registered user. The principal functionality is the same for both. By registering, the user has the ability to save and reload simulations as well as change some key parameters for the semiconductor models. He also gets the option to download a desktop version of the software.
The calculation possibilities that the tool offers range from simple product suggestions for one nominal operating point, enables a heatsink specifications and complex calculations for complete load cycles. One of the main criteria when developing this program was to have a simple user interface that would enable users to quickly familiarize themselves with the program and produce quick "estimations" on the required component application at the same time.
This tool is suitable for the following:

- selecting power semiconductors when designing new converters;
- specifying the necessary cooling measures;
- calculating efficiency rates;
- calculating maximum temperatures and thermal cycles for module life time calculations;
- comparing products with different semiconductor technologies and of different generations;
- selecting the optimum price-to-performance-to-size ratio by comparing existing degrees of freedom in the system design (switching frequency, cooling measures, overload capability);
- risk assessments as regards variation in both components and electric circuit parameters.

Some of the pros and cons of this type of calculation and simulation tool in comparison to commercial circuit simulators are listed in the table below.

Advantages	Disadvantages
High-level availability thanks to free access via the Internet	Limited to key application, e.g. PWM converters, suitability for new developments in the field of circuit technology and niche applications is limited
High-speed thanks to analytical calculations using behavioural models and special algorithms	Switching behaviour (time functions of current and voltage) including over-voltages, SOA, influence of parasitics and so on cannot be investigated;
Product database continuously updated and maintained by manufacturer	Limited user access for manipulation of device parameter
Application engineers' expertise in the area of power semiconductors made available to a broad range of users	User has no influence on the calculation algorithms used, but must assume they are suitable for his purpose and trust in their accuracy

Table 6.3.1 Pros and cons of online simulation tools for loss and temperature calculations

The philosophy of the software and the principal flow chart has not changed since the beginning

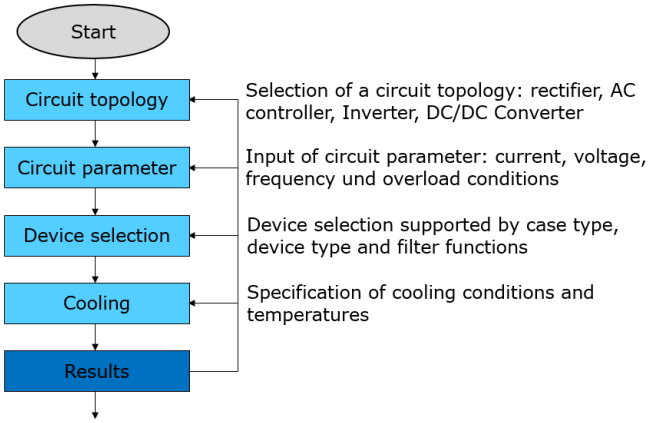


Figure 6.3.1 Flowchart for using SemiSel software

The user interface follows some simple rules. At the headline is a navigation bar which can be used to jump between the steps of the simulation process. Dark blue is the active element, light blue are selectable options or steps, grey are elements which are inactive because some input is missing. In the right corner is the simulation and profile menu to load and save your simulation input data (results are not saved) in the cloud or at your hard disk (e.g. to share files with others), to export results to PDF report or for editing profile.

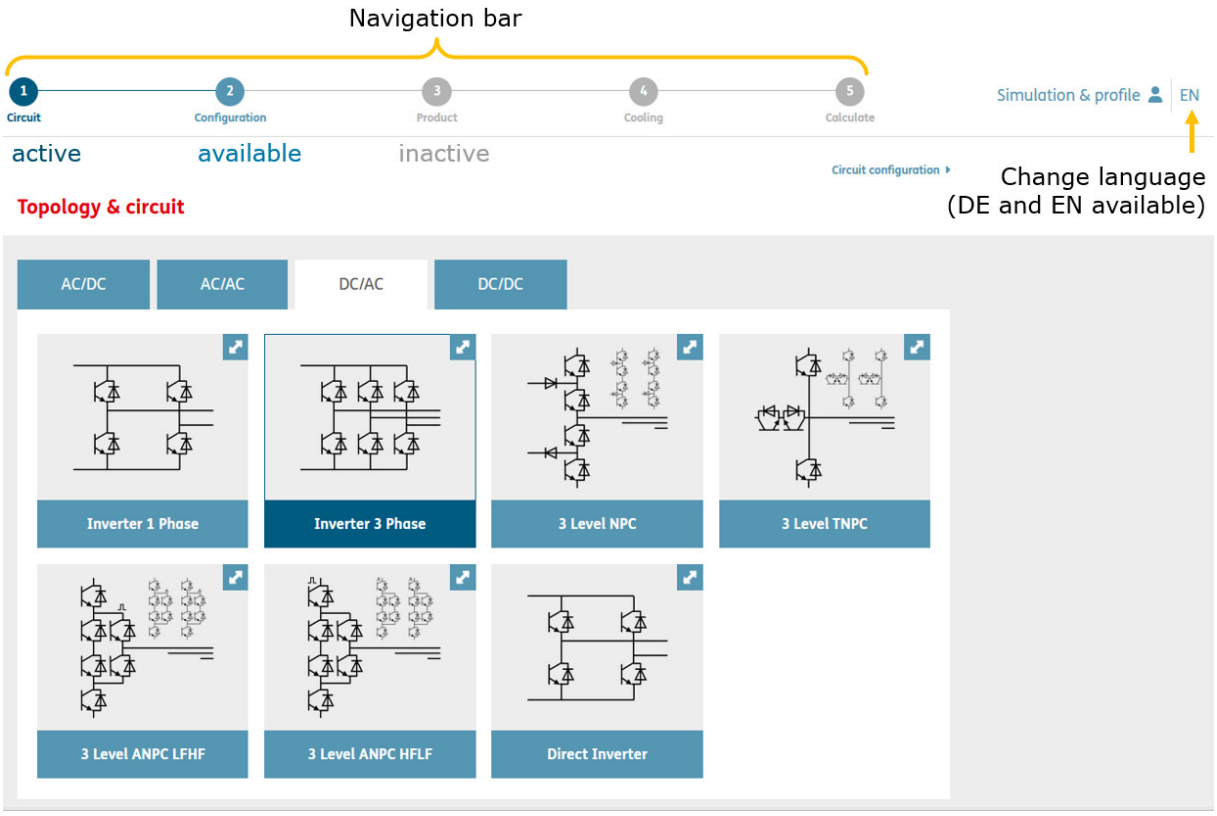


Figure 6.3.2 SemiSel user interface

Although the philosophy and flowchart have remained the same, the product database and simulation engine have undergone massive changes over time. All electrical parameters for the semiconductors are specified in look-up tables and the thermal models can distinguish between coupling conditions at low frequency or high frequency.
The loss calculation has been split into two main time domains:

- Losses and temperatures during periodical functions
- Losses and temperatures during overload and mission profiles

Details are described in the following.

6.3.1.1 Losses and temperatures during periodical functions

A uniform method for loss calculation is used for all switches and in all circuits like DC/DC converter, rectifier or PWM converter. For each of that circuits a periodic function of the output current can be defined. This periodic function is sampled with a certain number of points at which the loss calculation is performed. Conduction losses and switching losses (if present) are calculated temperature dependent for the actual conditions at any point. In Figure 6.3.3 is shown how the conduction losses are calculated. The forward characteristics are given in lookup tables and the forward voltage is calculated by interpolation between the four nearest points around the required current value and the calculated T_j. The interpolation is repeated until the loop of loss and temperature calculation does not change anymore.

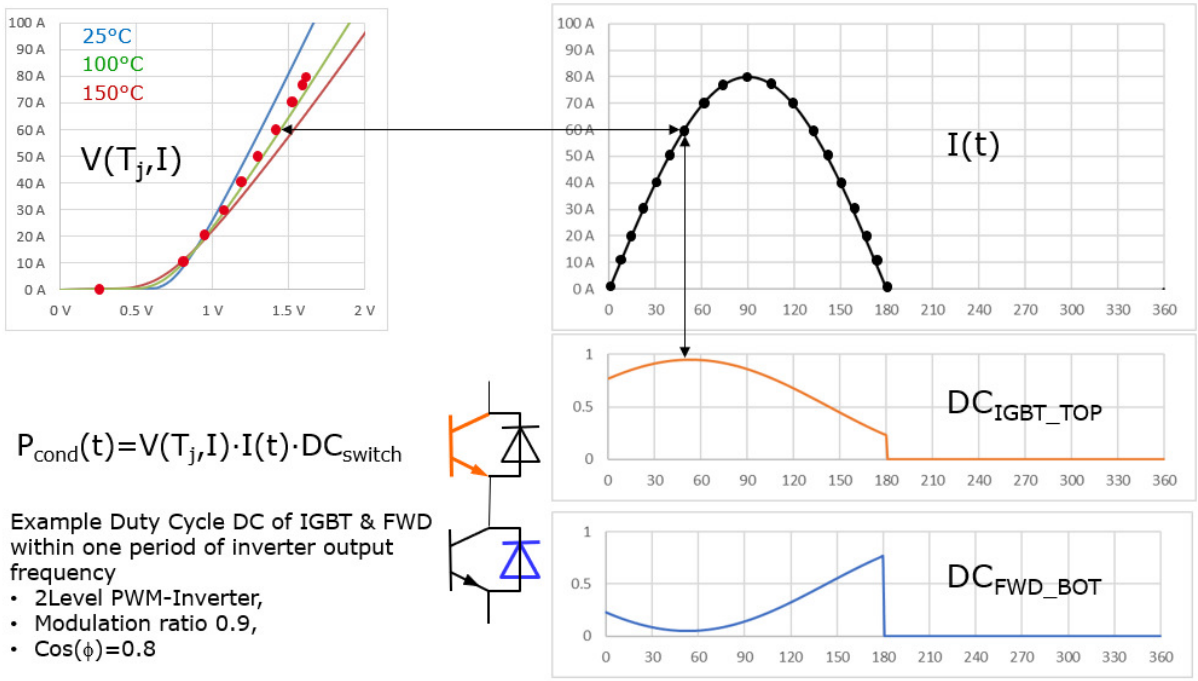


Figure 6.3.3 Calculation of conduction losses for periodical functions

The same procedure is done for the switching losses as shown in Figure 6.3.4. Switching losses are normally given in a four-dimensional matrix with E = f(T_j, I, V_{CC}). The fourth dimension is R_G but this has to be set in advance and cannot be changed during simulation.

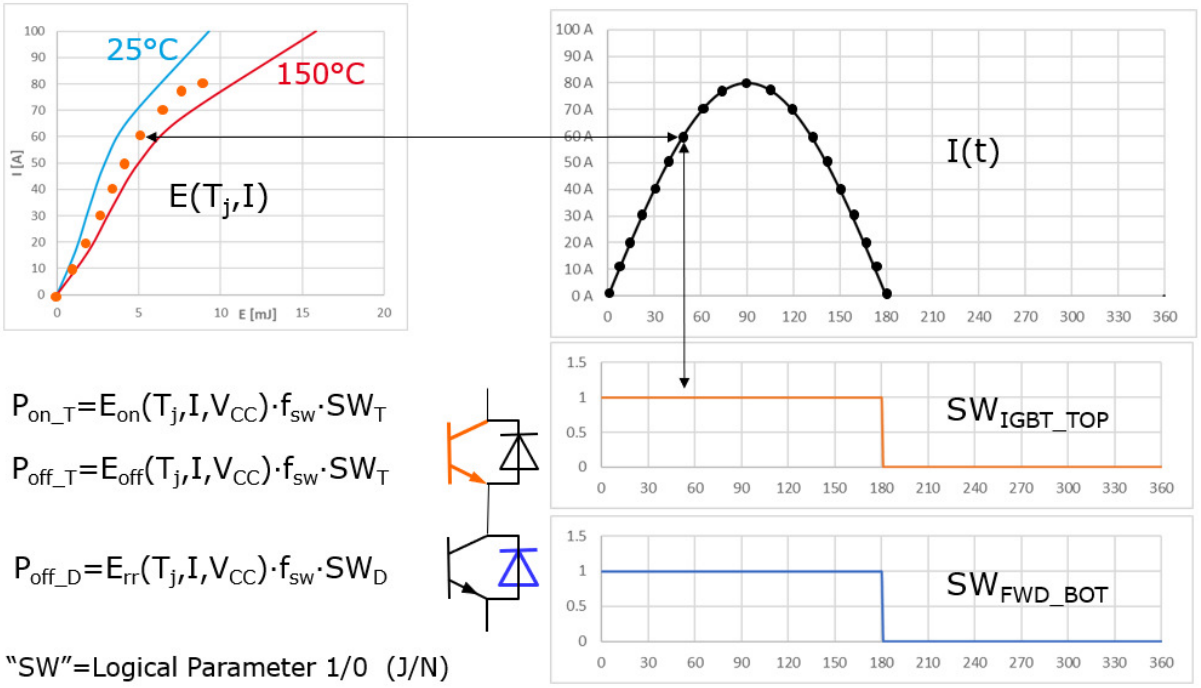


Figure 6.3.4 Calculation of switching losses for periodical functions

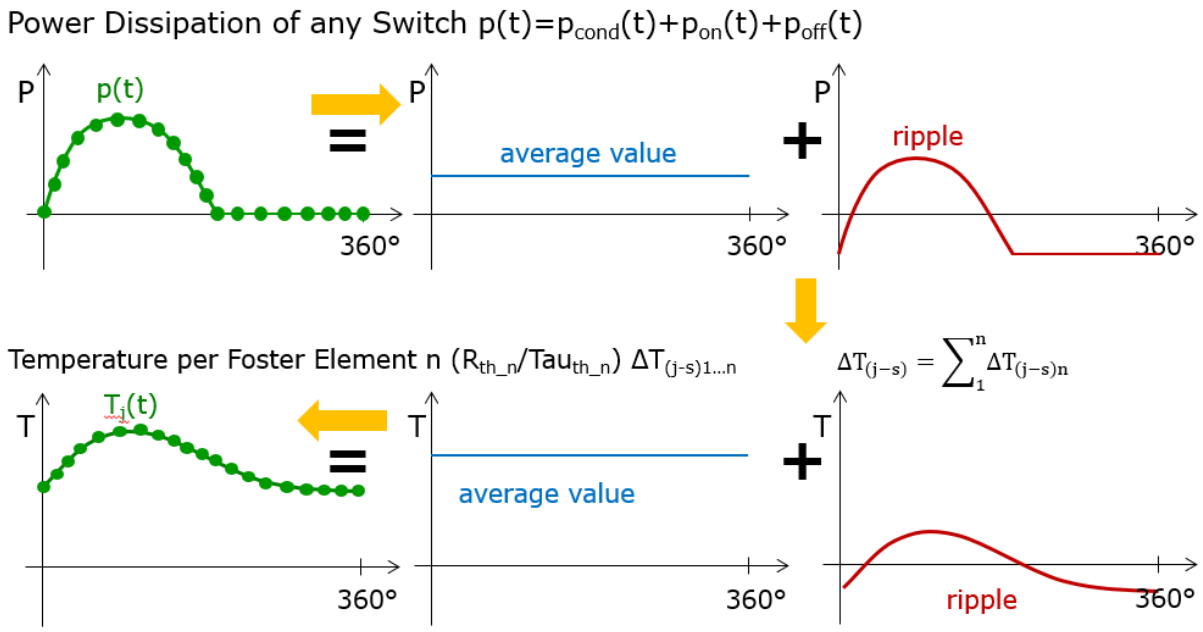


Figure 6.3.5 Separation of average on alternating losses to calculate the temperature ripple for the condition that start and end temperature of a periodic function is equal

6.3.1.2 Losses and temperatures during overload and mission profiles

An ongoing simulation of the temperature for longer sections in real time like it is done in circuit simulators is very time consuming and generates a lot of data. But it is not necessary to calculate the 50 periods in one second of a 50Hz application if the current does not change or only slightly. The first and last are enough to get a complete picture of the necessary information. To solve that problem a patented algorithm is used which switches between two modes depending on the load conditions [6.4]. For conditions with fast changing parameters or low converter frequency a simulation method is used, where losses and temperatures are continuously calculated over time for all switches (like in the circuit simulator) to improve the accuracy. In the remaining time with only small changes the simulator switches to single period calculation with increasing time steps to save simulation time (Figure 6.3.6).

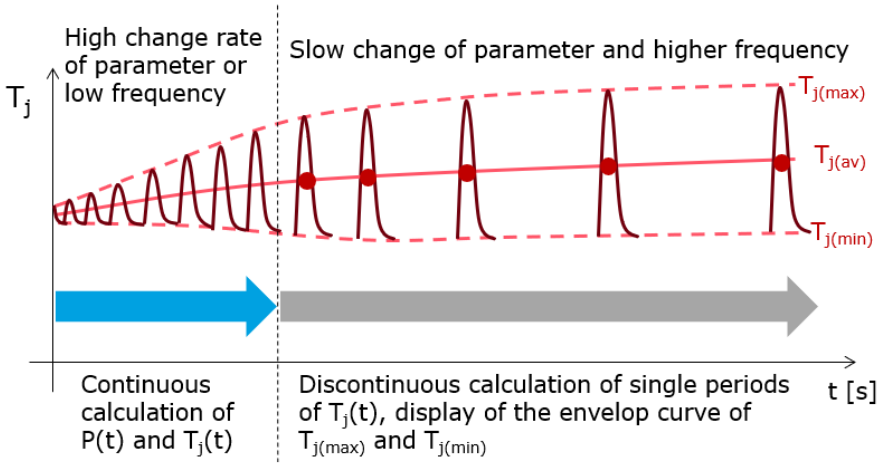


Figure 6.3.6 Switching between two simulation methods depending on operating conditions

6.3.2 Circuit and product selection, specification of operating and cooling conditions

By starting a simulation, the user can choose between in the meanwhile 27 different topologies to find the circuit most suited to his requirements. The topologies are sorted by the way how electrical energy can be transformed. Diagrams showing the circuit topology facilitate selection (see Figure 6.3.2).

In the next steps, the electric parameters for the circuit are entered for nominal conditions and overload conditions. The required input parameters vary depending on the circuit selected. All input fields are filled with default values; white fields with light grey numbers are calculated values for informational purpose. "Additional losses per heatsink" are caused by other components that are not part of the selected circuit (e.g additional rectifier or brake resistor losses) heating the same heatsink.
With the definition of an overload current for a limited period of time and in the case of converters in combination with a low output frequency it should be checked if the maximum allowed junction temperature is not exceeded.

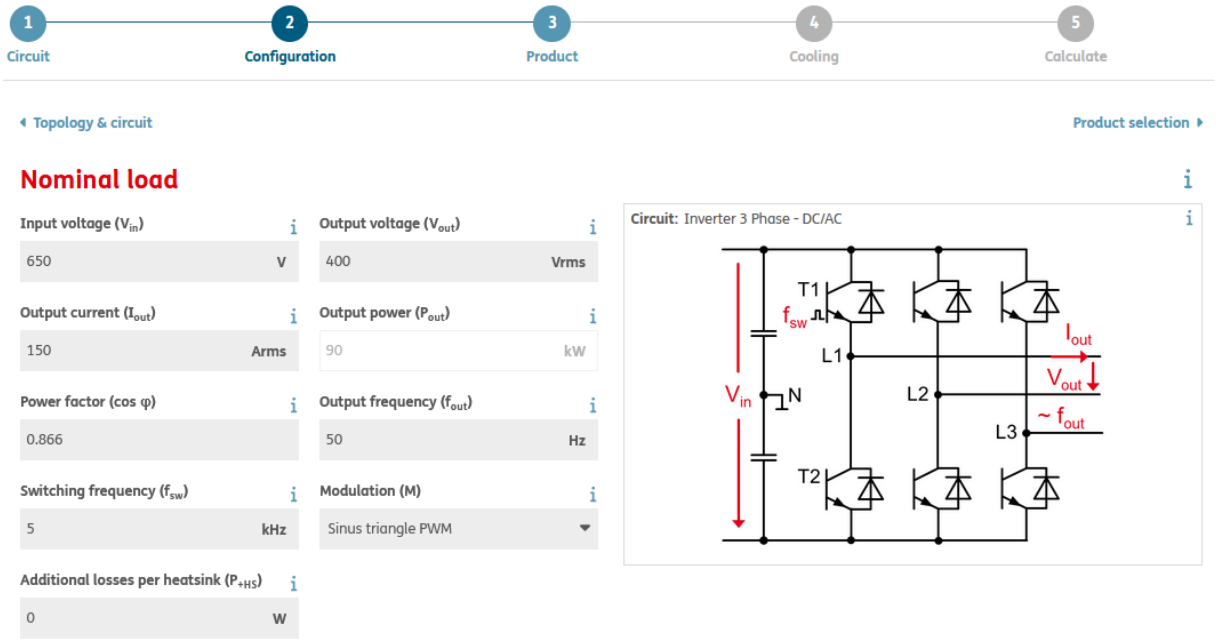
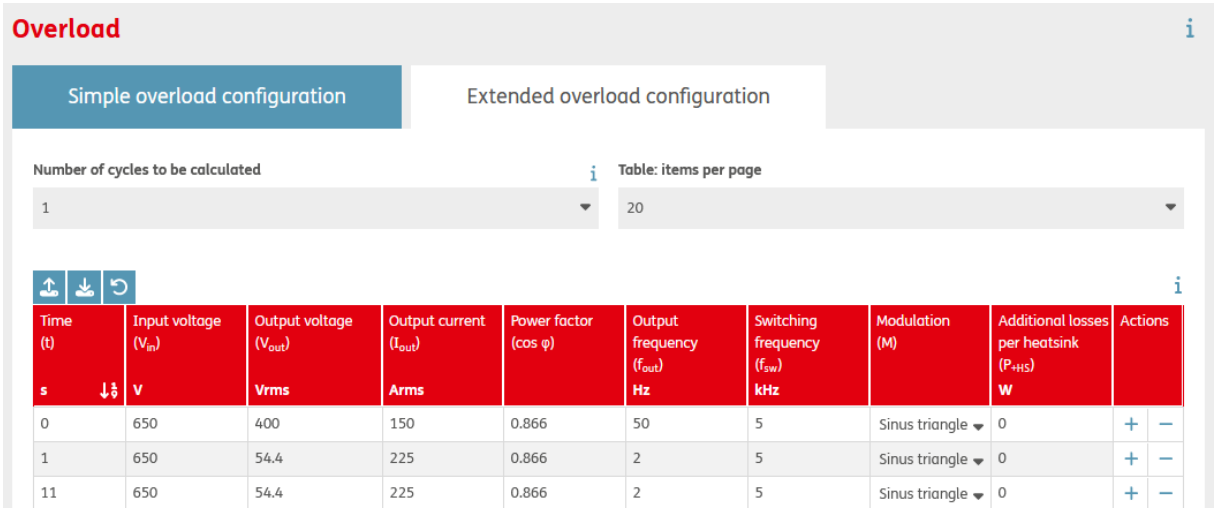


Figure 6.3.7 Input of nominal condition in example for the three phase converter

Load and temperature cycles are another aspect that limits service life. Instead of a simple overload current SemiSel provides for these cases a table for a complete mission profile, which can be specified in the "extended overload condition" or uploaded from a CSV file (correct order of columns must be observed, see Figure 6.3.8). What is relevant for this kind of load is the temperature difference between operation under full load and idling rather than the maximum temperature. This leads to ageing effects in the power module and must therefore be included in the lifetime evaluation of the converter.



Time (t) s	Input voltage (Vin) V	Output voltage (Vout) Vrms	Output current (Iout) Arms	Power factor (cos φ)	Output frequency (fout) Hz	Switching frequency (fsw) kHz	Modulation (M)	Additional losses per heatsink (P+HS) W	Actions
0	650	400	150	0.866	50	5	Sinus triangle	0	+ −
1	650	54.4	225	0.866	2	5	Sinus triangle	0	+ −
11	650	54.4	225	0.866	2	5	Sinus triangle	0	+ −

Figure 6.3.8 The extended overload in tabular form

Figure 6.3.9 shows an example of an operating cycle of an elevator drive including the 4 operating states: start "acceleration", constant speed, braking "deceleration" and standstill. The load cycle

values are entered in a table with reference points. Between these points, the program performs a linear interpolation. During the acceleration and braking phase, an overcurrent flows. A particularity of braking is that the direction of energy flow is changed. The power factor cos(φ) becomes negative – the converter works as a rectifier and feeds back energy into the DC-link capacitor.

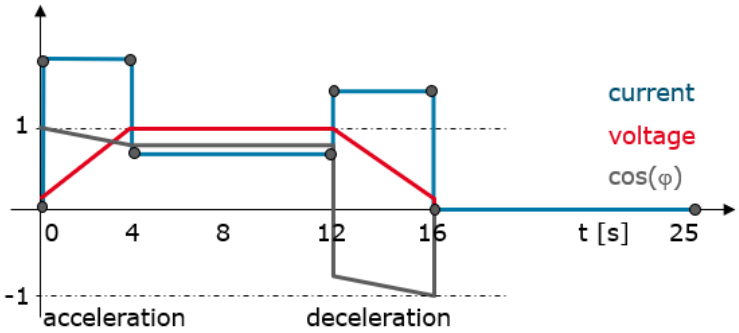


Figure 6.3.9 Typical load cycle of an elevator (voltage and current are shown here as normalized values for a better understanding)

After all electrical circuit conditions are specified, a suitable component need to be selected at the product page. A rough preselection ("Recommended Products") according to current, voltage class and switching frequency shows some products which should typically fit to the application. Switch the recommendation off and use filter setting to reduce the complete list of products to a manageable number (see Figure 6.3.10). Products with voltage classes lower than the required blocking voltage are not visible anyhow. If one product is selected you can get some additional information in a pop-up window by clicking on the "i" or as a registered user you can modify some key parameter by clicking on the gearwheel.

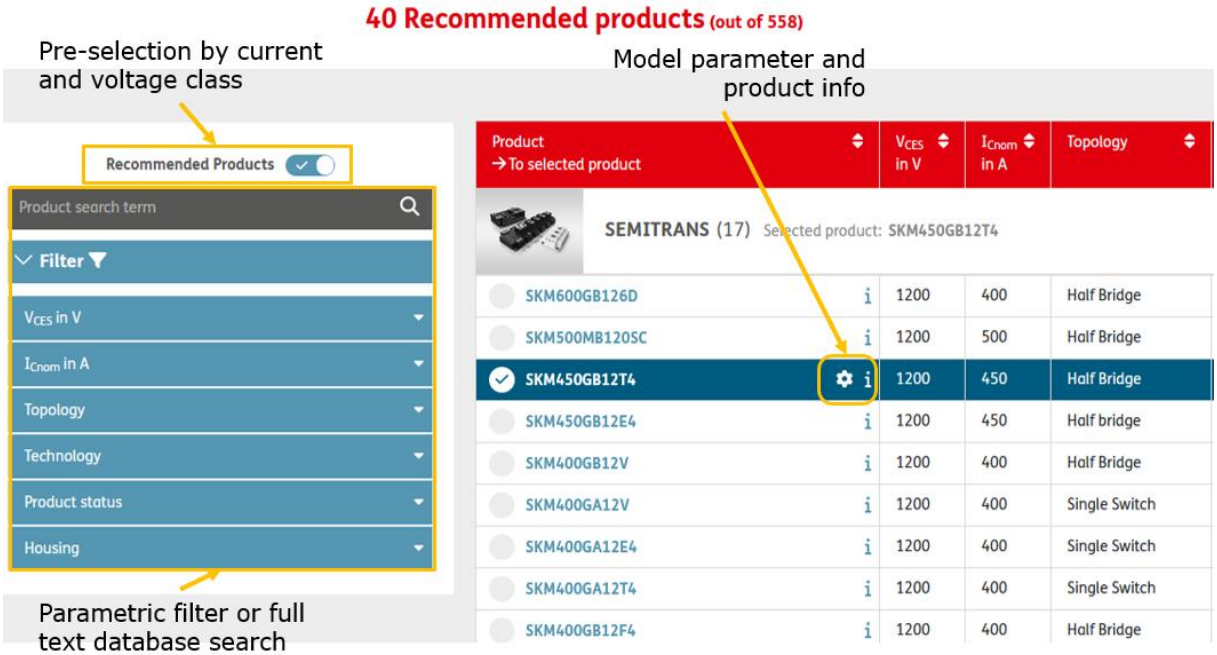


Figure 6.3.10 Product selection

The last step before the simulation can start is the specification of the cooling conditions. In the simplest case, losses and chip temperature can be calculated at a constant heatsink temperature. However, this is not recommended because with an infinite heat sink it is possible to achieve power densities that are not feasible for power modules. Furthermore, contributes the heatsink a high proportion to the ΔT_j which has a major influence on the lifetime calculation. Therefor is a simulation with a typical air cooled or liquid cooled heatsink a better choice as proposed from the software. The heatsink dimensions and therewith its thermal properties are calculated according to the size and number of selected power modules (Figure 6.3.11). Of course, it is possible for the user to specify a thermal impedance by R_{th} and τ values of a Foster model. Ambient temperature is

to be understood in the sense of the coolant temperature (water, air). This needn't necessarily correspond to the temperature inside the converter box. Some products have already included a heatsink, in that case the user interface changes to a predefined heatsink, with the possibility to change the flowrate only.

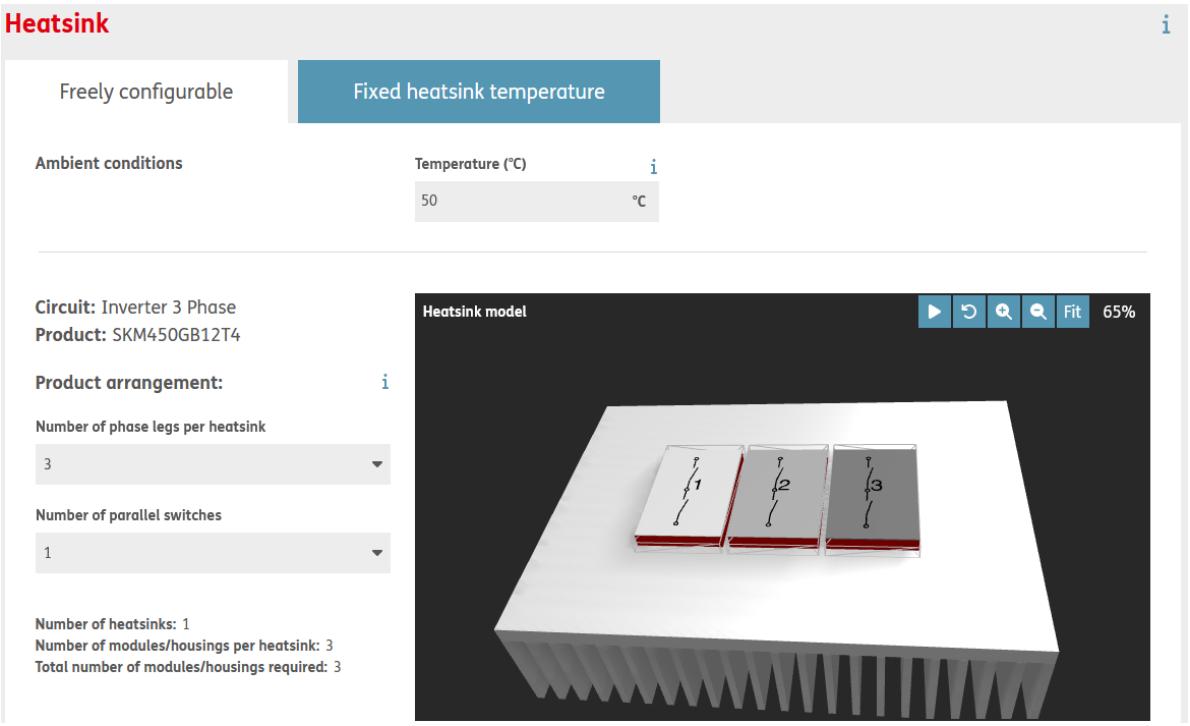


Figure 6.3.11 Specification of cooling conditions with a proposed heatsink

6.3.3 Results

Temperatures and losses at the nominal conditions are displayed after starting the simulation. Bar charts for all types of semiconductors used in the circuit allow easy assessment of numbers compared to critical values (Figure 6.3.12). With symmetrical circuits, the temperature is only displayed for one switch with the same functionality. The legend next to the temperature scale results from the recommended and maximum operating temperatures, blue = recommended area, light red = critical area with restrictions regarding duration or reliability, dark red = not allowed area. Losses and temperatures are also displayed for one period of the output frequency as a function of time (Figure 6.3.13). For losses a distinction is made between conduction losses, losses caused by turn-on energy and turn-off energy. If one of the segments is missing, this type of loss does not occur in the switch.

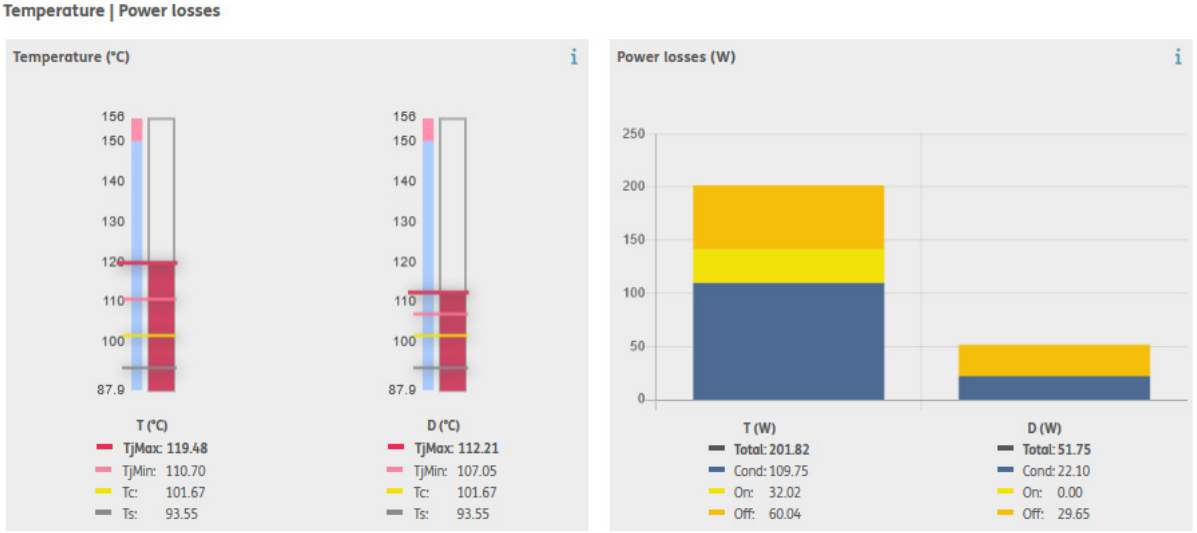


Figure 6.3.12 Temperatures and losses at nominal conditions of a PWM converter as an example calculation (T – IGBT values, D – Freewheeling diode values)



Figure 6.3.13 Time function of temperature and losses for one period (360°) of the PWM converter output frequency

Temperatures and losses during overload or a mission profile are shown in a second folder called "overload". The simulation is carried out as continuous time function at the transitions between nominal load and overload for a higher precision (darker grey background in Figure 6.3.14). At times with small changes of load conditions the temperature represents an envelope curve and the losses are the average values over a period of the output frequency.

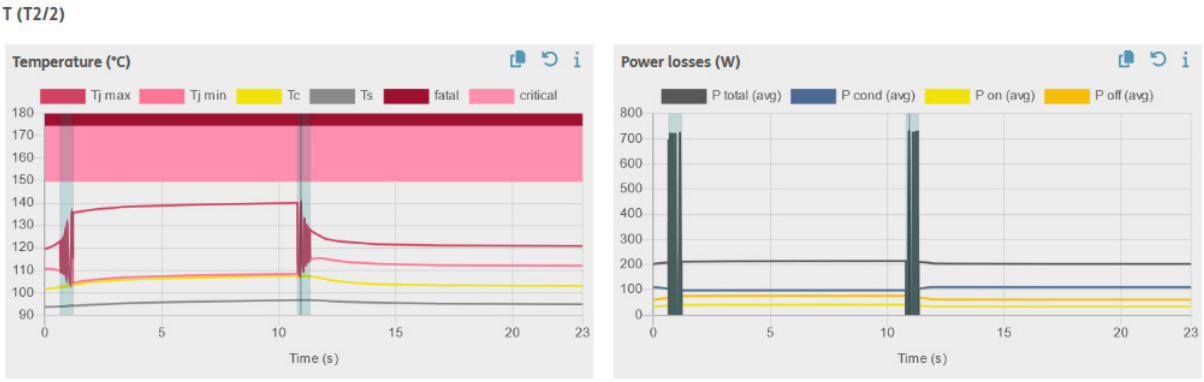


Figure 6.3.14 Temperatures and losses during the overload condition.

A judgment of the results is only done with regards to maximum junction temperature. If a device is suitable for the application might depend also on another parameter.

6.4 Semiconductor models

Before starting to look for suitable models, the following question must always be answered: What properties does my model have to have in order to fulfil the simulation task?

- Analysis of the circuit operating principle: Ideal switch models
- Determination of losses and temperatures: Static models and state models
- Examination of individual switching processes: Physical model of semiconductor and behaviour models

6.4.1 State graph models

The online simulation tool SemiSel can be used to perform power dissipation and temperature calculations for defined circuits. If necessary, e.g to investigate new circuit topologies, state models can simply be generated using the data provided in the datasheets. These models use characteristics in "look-up tables" and/or equations to describe forward voltage, switching losses and switching times. They are suitable for all simulation tools that are compatible with state graphs [6.5] or using it internal as a model description [6.6]. Models in XML format description can be found in the download area at the Semikron Danfoss homepage. Assistance creating the datasets for these models can be provide on request. These models are not suitable for examining switching processes; they have ideal switching edges. Therefore, no parasitic inductances may be taken into account in the simulation circuit.

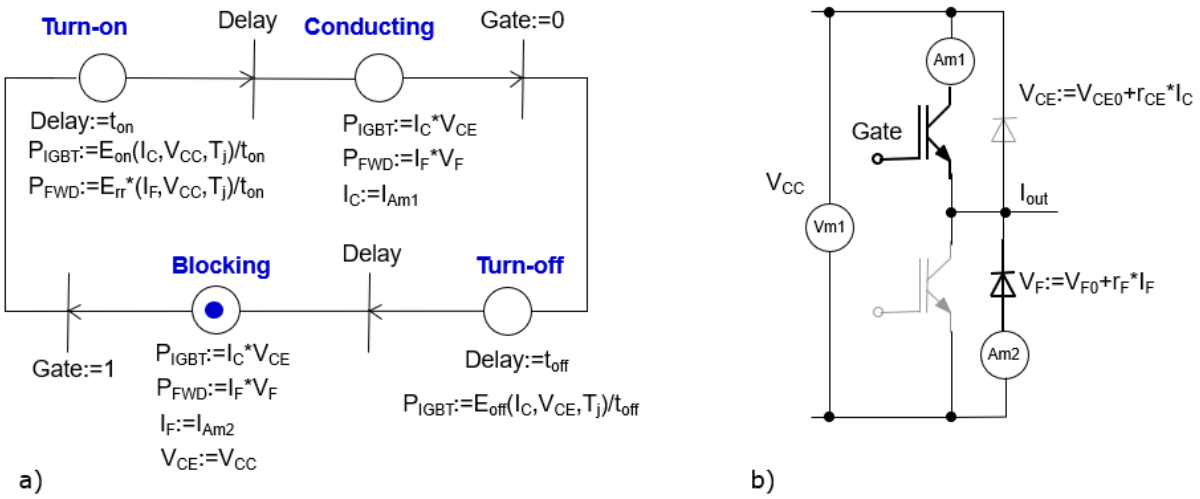


Figure 6.4.1 Semiconductor modelling using state models; a) State description; b) Electric equivalent circuit

A model such as this comprises an "ideal" switch with a logic drive signal ("Gate:=1" or "0" in Figure 6.4.1), for which the power dissipation is calculated in 4 different states. In the example shown, the states (shown as circles) are given as IGBT switching states. If a transition (line) applies, e.g. if the signal "Gate:=1" is set, the marked, active state moves to the next state. In the example here, the marker would move from "Blocking" to "Turn-on". During this state, switching losses are caused; here, turn-on losses for the IGBT and turn-off losses for the diode. After a delay time ton, the marker moves to the next state - "Conducting"- where conducting losses occur. These losses are continuously calculated from the circuit current and the on-state voltage of the IGBT. The on-state voltage can be stored in the form of a characteristic. If the driver signal is set to "0", the component goes over to "Turn-off" state, in which turn-off losses occur. After a delay time toff, the IGBT goes back to the original state - "Blocking" - where the conducting losses of the diode are calculated. This completes the switching cycle. The switching losses can likewise be stored as a characteristic and read out for the current switching parameters. For simple cases, the equations for switching energies given in chapter 6.1.2 are used, since the junction temperature and DC link voltage dependencies are not available in the datasheet as characteristics.

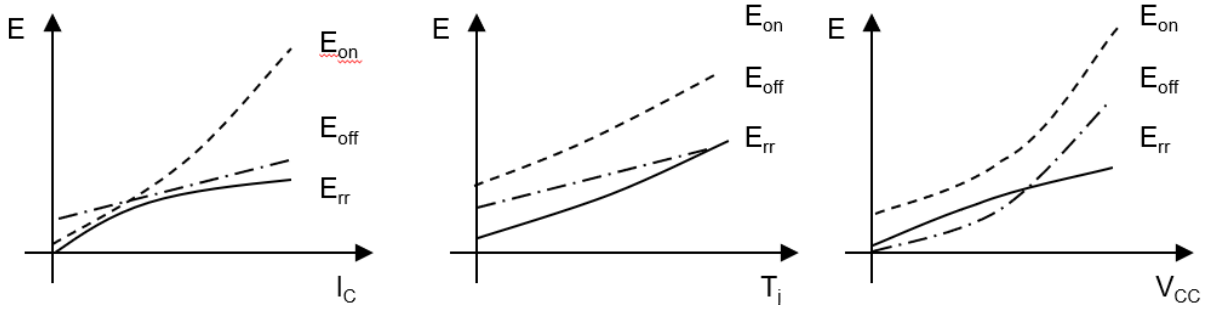


Figure 6.4.2 Example for dependency of switching losses on I_C, T_j and V_{CC}

Current sources in the thermal equivalent circuits can then be fed with the calculated losses (Figure 6.4.3). The resistances correspond with the R_{th} values of the thermal impedances. If time constants τ are given, then the capacitances are calculated by $C_{th} = \tau/R_{th}$. The temperature is then fed back to the switching parameters and affects the switching losses and on-state voltage of the models. For the PWM converter, it suffices to calculate the losses and temperatures for one IGBT and one diode; this is owing to the symmetry here.

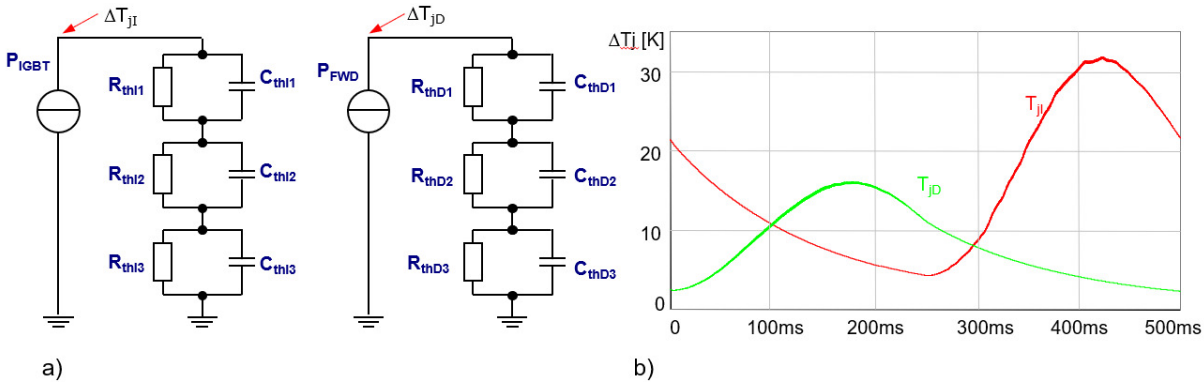


Figure 6.4.3 a) Thermal equivalent circuit and b) example of calculated temperature difference of a PWM converter with 2Hz output frequency

6.4.2 Physical models of semiconductors and behaviour models

Both model types claim to provide a realistic picture of the switching behaviour in dependence of the driver and load conditions. They are highly suitable for investigating individual switching processes. Owing to the differences in time scale (some 10^{-9} s for a single switching process ↔ heating in 100s), these models are not suitable for simulating on system level including heatsink time constants. Even just a few periods of a converter output frequency require substantial calculation time.

While physical models draw upon equations used in semiconductor physics, behaviour models describe the semiconductors more like a black box with characteristics which can be measured from outside. Combined forms are feasible for use in any increments. For the physics-based semiconductor models, the main problem lies in the fact that the parameters are difficult to obtain, meaning that these models are ultimately not very practical for users. They do, however, offer the advantage that they provide valid results across a broad operating range. Behaviour models are more easily parameterised with datasheet values and measured switching curves. One shortcoming here is that they are often applicable to a limited range of operating conditions only. For both models is the switching behaviour essentially determined by parasitic elements (stray inductances, capacitances to ground…) in the circuit environment. The merit of the given model can therefore only be assessed on the basis of how precise elements of the packaging and interconnections are determined and included in the simulated circuit.

An example of a behaviour model is shown in Figure 6.4.4 [6.7]. The static behaviour is simulated using two characteristics: saturation characteristic and the transfer characteristic. The saturation characteristic is assigned to diode D1 and causes the voltage drop $V_{CE} = f(I_C)$. The transfer characteristic controls the current source parallel to D2 in dependence of the applied gate voltage. The current in the IGBT rises and falls in line with the charge and discharge of the gate-emitter capacitance C_{GE} via the gate. The most important element when modelling the dynamic behaviour is the non-linear Miller capacitance which ensures feedback of the collector-emitter voltage to the gate.

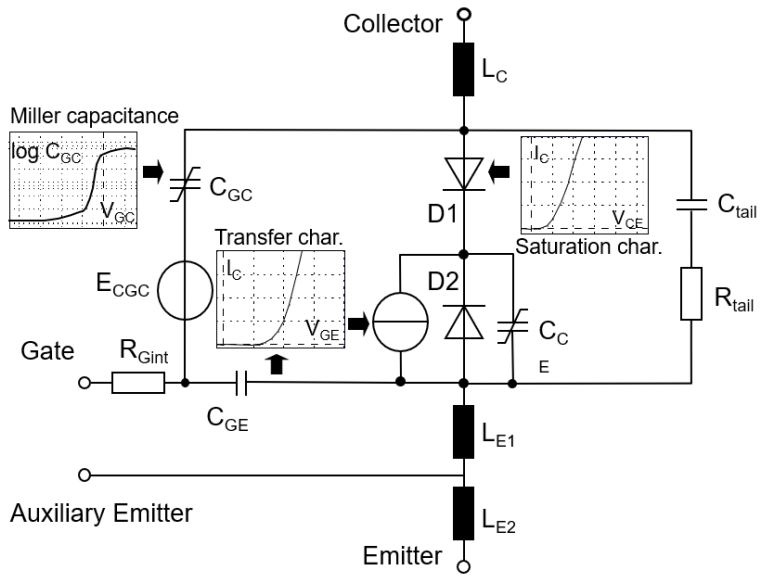


Figure 6.4.4 Example of an IGBT behaviour model with equivalent circuit elements [6.7]

The models can be optimised for certain operating points to ensure that they correctly model switching times and losses. They do not, however, sufficiently describe the switching properties for any given switching condition to malfunction/failure, meaning that the amount of time and work that goes into producing these models is by no means justified. What is more, no adapted models exist for latest-generation IGBT, despite the fact that the switching behaviour of these components differs greatly from that of the predecessor IGBT generation. This is why Semikron Danfoss is not offering semiconductor models.

6.5 References

[6.1] S. Konrad, Dissertation "Ein Beitrag zur Auslegung und Integration spannungsgespeister IGBT-Wechselrichter", ISLE Verlag, ISBN 3-932633-09-1, TU Ilmenau, 1997

[6.2] D. Srajber, W. Lukasch, "The calculation of the power dissipation for the IGBT and the inverse diode in circuits with sinusoidal output voltage", electronica, Conference Proceedings 1992

[6.3] SemiSel software tool https://semisel.semikron-danfoss.com

[6.4] M. Röblitz, A. Wintrich, C. Schmidt, “High Speed Hybrid Simulation Engine for Electrical Mission Profiles”, PCIM Europe, Conference Proceedings 2021

[6.5] PORTUNUS® www.adapted-solutions.com

[6.6] PLECS® www.plexim.com

[6.7] A. Wintrich, Dissertation "Verhaltensmodellierung von Leistungshalbleitern für den rechnergestützten Entwurf leistungselektronischer Schaltungen", TU Chemnitz, 1997

7 Datasheet Statements

7.1 Standards, symbols and common terms

7.1.1 International standards

The practical usage of symbols and terms and their meaning is described in the international standard IEC 60747 "Discrete Semiconductor Devices". Detailed information on the parameters, minimum requirements for datasheet ratings and test methods is provided in the standard's product specific sections.

IEC 60747-1 Letter symbols and terms [7.1]
IEC 60747-2 Diodes [7.2]
IEC 60747-6 Thyristors [7.3]
IEC 60747-8 Field effect transistors [7.4]
IEC 60747-9 IGBT [7.6]
IEC 60747-15 Isolated power semiconductor devices [7.7]

Other important standards applicable to semiconductor devices:
IEC 60191-2 Mechanical standardisation of semiconductor devices, Part 2: Dimensions (Standardised case drawings) [7.8]
DIN EN 50178 Electronic equipment for use in power installations (insulation tests, partial discharge) [7.9]
IEC 60664 Insulation coordination for equipment within low-voltage systems (clearance and creepage distances) [7.10]
IEC 60721 Classification of environmental conditions [7.11]
IEC 60068 Environmental testing (specification of test conditions) [7.12]
IEC 60749 Mechanical and climatic test methods [7.13]

The following specifications and standards do not correspond with international standards in use, but are applicable to particular markets:

UL94 Tests for Flammability of Plastic Materials for Parts in Devices and Appliances" [7.14]
UL508C Power conversion equipment [7.15]
MIL-STD-750E Test methods for semiconductor devices [7.16]

7.1.2 Letter symbols and terms

7.1.2.1 Voltages

Two index letters are used to designate the terminals between which the applied voltage is measured. If the potential of the terminal designated with the first index letter is positive versus the terminal designated with the second index letter (reference potential), the applied voltage is positive, e.g., V_{CE}.

C collector
E emitter
G gate
D drain
S source
K cathode
A anode

For diodes, the forward on-state voltage is indexed with "F" and for thyristors with "T" rather than "AK" ("forward" positive anode potential versus cathode potential); "R" is used to designate the reverse blocking voltage ("reverse" positive cathode potential versus anode potential). In the case of transistors, an additional third index letter may be used to determine the wiring status between the terminal with index 2 and a non-designated third terminal, e.g. V_{CES} indicates that the IGBT is "short circuited between gate and emitter". The following abbreviations are permissible:

S: short circuit
R: resistance to be specified
V: external voltage to be specified
X: resistance and external voltage to be specified

Index letters may be followed or preceded by other indices to specify further parameters; these may (or may not) be in parenthesis and may be in upper or lower case, e.g. $V_{(BR)DS}$ or $V_{GE(th)}$ or V_{CEsat}:

(BR): breakdown voltage
sat: saturation voltage
(th): threshold voltage
clamp: clamping voltage limited by external circuits

Supply voltages are marked with double index letters, e.g. V_{GG} (supply voltage of a gate-emitter circuit), V_{CC}, V_{DD}.

7.1.2.2 Currents

Here, the index letter used designates the terminal at which the current enters the component, for example G: Gate, C: Collector, D: Drain, E: Emitter, S: Source (e.g. I_G stands for gate current). Positive values specify positive currents. For diodes, "F" is used for forward current, for thyristors, "T" for on-state currents (anode-cathode) and "R" for reverse currents (cathode-anode). Exceptions to this rule of thumb are reverse and leakage currents, where a second index letter is used to designate the second terminal at which the reverse voltage is applied. In analogy to the indices used for voltages, an additional third index letter may describe the wiring status between terminal 2 and a non-designated third terminal, e.g., I_{GES}. Index letters may be followed or preceded by other indices; these may (or may not) be in parenthesis and may be in upper or lower case, e.g.:

AV: average value;
RMS: effective value (root mean square);
M: peak value (maximum);
R: periodic (repetitive);
S: non-repetitive (surge);
pulse: pulsed (direct current).

7.1.2.3 Temperatures

Temperatures are always indicated with a capital T. The following index letters are the most commonly used in the context of temperatures:
j junction, formerly also "vj" for virtual junction
c case (here, the heat-dissipating baseplate is meant)
s sink, formerly also "h" for heatsink
r reference point (usually an integrated temperature sensor)
a ambient (usually refers to the coolant temperature)

(Virtual) junction temperature T_j

This refers to temperature assigned to an area inside a semiconductor device where a virtual heat source provides thermal output originating from electrical power losses. The virtual junction temperature T_j is a virtual parameter and cannot be measured directly. For convenience, it is also used for power semiconductors without a pn-junction such as MOSFET. It constitutes a theoretical average value from which the actual temperature at a chip pn-junction can differ significantly. This effect increases with chip size. Figure 7.1.1 shows the temperature spread measured across a live 12mm x 12mm chip with a very good cooling.

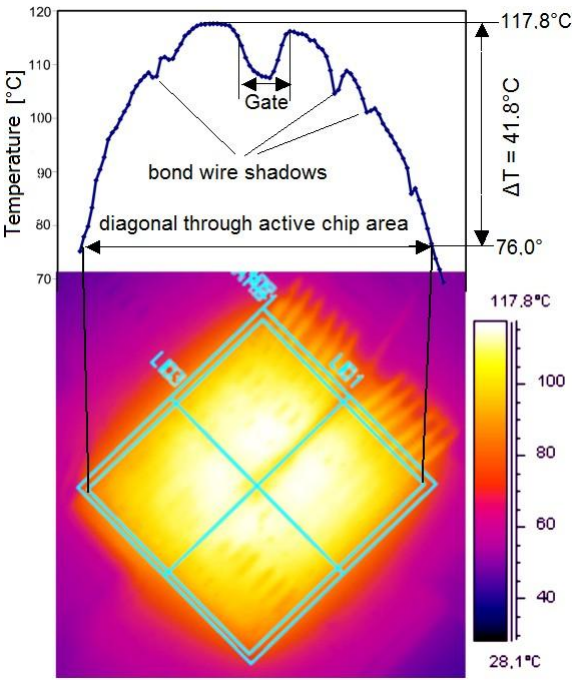


Figure 7.1.1 Example of a temperature spread on a power semiconductor chip

The Figure 7.1.1 reveals the large difference in temperature (ΔT = 41.8°C) between the edges of the chip and the hot spot. The characteristic clearly shows the non-conducting gate area, as well as the heat absorbing activity of the bond wires. The temperature measured with the standard method using the negative temperature coefficient of the forward on-state voltage is equal to the average local chip temperature either measured across the active chip area with an infrared spectrophotometer or calculated by simulation.
The maximum (virtual) junction temperature T_{vj} or T_j is a limit value for power semiconductors and the reference temperature for most characteristics at the same time. The junction temperature T_j can be calculated from the measurable case or heatsink temperature, the power losses and the thermal resistance (given in the datasheet) to check whether it is within the permissible limits.

Case temperature T_c, reference point temperature T_r

Temperature at a fixed reference point of the baseplate. For power modules, it may be necessary to differentiate between the maximum permissible temperature of the baseplate and the plastic housing. For low power devices in plastic housings, generally a difference is made between the case temperature (measured on the surface of the plastic housing) and the reference point temperature T_r (taken at a fixed reference point of a terminal). For metal enclosed devices, both terms are interchangeable. For devices with an integrated temperature sensor, T_r designates the sensor temperature.

Heatsink temperature T_s

Temperature of the heatsink. The temperature T_s is taken at a fixed reference point inside the heatsink or on the heatsink surface next to a power semiconductor.

Ambient temperature T_a

Temperature at which the coolant (e.g., air) flows towards the semiconductor device or its cooling system. The coolant flow may be induced by convection (natural cooling) or effected by a fan (forced cooling). As for liquid cooling, T_a indicates the temperature of the liquid coolant.

Operating temperature range T_{op}

Permissible junction temperature range (or in rare cases also case temperature range) within which the semiconductor device may be subjected to electrical load. The upper limit of the operating temperature is identical to the maximum permissible junction temperature. At this point the permissible electrical load tends to zero, and all of the above-mentioned temperatures will be equal to the maximum permissible virtual junction temperature.

Storage temperature range T_{stg}

Temperature range within which a semiconductor device which is not under electrical load may be stored or transported. Maximum permissible temperature for the (plastic) housing materials of power modules.

7.1.2.4 Temperature differences, thermal resistances (R_{th}) and impedances (Z_{th})

These are designated with two hyphenated index letters describing the reference points between which they apply, e.g., $\Delta T_{(j-a)}$, $R_{th(c-s)}$ or $Z_{th(j-s)}$.

7.1.2.5 Mechanical parameters

These parameters refer predominantly to the assembly of components. Important mechanical parameters are minimum and maximum tightening torques (M) for screw terminals M_t, heatsink connections M_s and the maximum value of permissible acceleration. Further information includes the weight (w or m).
The dimensions are shown in a scale drawing. Also given are the internal and/or standardised housing designations.
The terminology used for other electrical, thermal and mechanical parameters is largely based on the terminology for voltages and currents. Switching states (turn-on, turn-off) may also be specified with index letters (usually in brackets).

7.1.2.6 Other symbols

The terminology used for other electrical, thermal and mechanical parameters is largely based on the terminology for voltages and currents. Switching states (turn-on, turn-off) may also be specified with index letters (usually in brackets).

7.1.3 Datasheet structure and hints for reading

Historically grown, Semikron Danfoss data sheets of different component and module generations, different product families and different module platforms also show differences in structure, data scope and specification conditions. Since standardisation is carried out continuously within the scope of product maintenance, the following explanations are based on the structure of data sheets created after 2016 for rectifier and issued from 2020 onwards for IGBT i.e., the latest 7th chip generation. Deviations in the data sheets of older components are pointed out.
In addition to the designation and a view of the module, the cover sheet contains the limit values and characteristic values of the power semiconductor in tabular form. The characteristic values are subdivided into minimum, typical and maximum characteristic values, if this makes sense. In the grey area to the left of the limit and characteristic values, general information on the special properties and possible applications of the module is listed under "Features" and "Typical Applications". Additional information are listed under "Remarks", e.g. on conditions of use and measurement conditions for the data sheet information. Below this is a schematic diagram of the module topology. The date of publication of the data sheet is listed in the grey footer of all pages.
The data given in the tables are followed by the diagrams, whose numbering is based on the general numbering structure, i.e., the diagrams in a datasheet will not necessarily be numbered consecutively. The final pages of the datasheet contain the outline drawing including dimension data, a basic diagram of the internal circuits showing the terminal layout as well as a disclaimer "IMPORTANT INFORMATION AND WARNINGS".
When comparing data sheets of apparent equal components, it must be considered that the data sheet specifications of different manufacturers are often only comparable to a limited extent due to different specification conditions. In many cases, owing to the complex, application-specific interaction between different module features, additional measurements will be necessary.
Many important limit and characteristic value specifications as well as application hints for Semikron Danfoss semiconductors, which apply uniformly to all types of a product line, are not contained in the type-related data sheets, but in the "Technical Explanations" and "Mounting Instructions" of the product line.

7.1.4 Maximum ratings and characteristics

7.1.4.1 Absolute maximum ratings

The maximum module ratings indicated in the datasheets are extreme electrical, thermal and mechanical load values which are permissible without risk of destruction. Maximum ratings can't be measured. The devices are tested to ensure they meet the rating. Nevertheless, even within these

limits every component is subject to the "usual" aging processes. All maximum ratings are determined under precisely defined conditions. It is mandatory to cite these in the datasheets. Deviating ambient conditions may result in different ratings, whose interdependencies are known to a certain extent only. Maximum ratings are absolute values, i.e. exceeding even one single rating may result in component destruction, even if other ratings have not been stretched to the limit. Apart from the "static" maximum ratings, "dynamic" maximum ratings also exist, i.e. limits for the permissible course of the characteristic (current/ voltage) during switching. Unless otherwise specified, the datasheet ratings apply to a chip or case temperature of 25°C. For reliable operation, it is necessary to keep a safety margin to the maximum ratings. Absolute maximum ratings are not measurable values; the ability to achieve these values is proven through tests.

7.1.4.2 Characteristics

Characteristics are measurable values. The characteristics describe the component properties determined under certain (normally application-specific) measuring conditions. Here, too, the characteristics are based on very precise operating conditions. As operating conditions are not standard in given applications, it is imperative that they be explicitly specified in the datasheets. Characteristics are often given as typical values with a scattering range. The reference temperatures (chip or case temperature) are usually 25°C and a second, high temperature for example 125°C or 150°C. For other temperatures, temperature dependencies have to be taken into account. If no temperature is specified, it applies to 25°C or no temperature dependence at all is assumed.

7.2 Datasheet specifications for thyristors and diodes

7.2.1 General information

The Semikron Danfoss thyristor/diode modules are offered in a variety of single, dual and bridge rectifier topologies. With blocking voltages of up to 2200V, Semikron Danfoss offers a solution for most phase control or rectifier applications. The modules are available in SEMIPACK®, SEMIPONT®, SEMiX® and SEMITOP® housings Various packaging technologies – soldering, wire bonding and pressure contact – are available.
The explanations in the chapters 7.2.2 to 7.2.4 are based on the example of single- and halfbridge-modules with thyristors and diodes as well as AC controller modules. The chapter 7.2.6 contains additional information on the data sheet specifications of power modules with complete rectifier bridges and in chapter 7.2.7 those for discrete thyristors and diodes are explained. However, the CB, CI and CIB modules with additional integrated IGBT as brake choppers and/or inverters are not mentioned here, but the statements made here regarding ratings, characteristics and diagrams for the rectifier also apply to the rectifier part in these modules. Information about module families, type designations and IGBT properties in chapter 7.3.
Most of the following explanations are based on the example of the data sheet of the latest 6th Generation thyristor/diode halfbridge module SKKT107/16E [7.17]. In the following explanations - related to the properties of thyristors and diodes, where the terms in square brackets [ ] exclusively apply to thyristors.

7.2.1.1 Major halfbridge and AC controller module topologies

The Table 7.2.1 shows the most common topologies of thyristor/diode modules and the product lines in which these are being integrated.

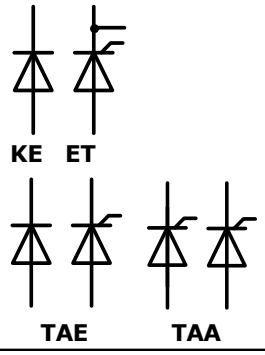
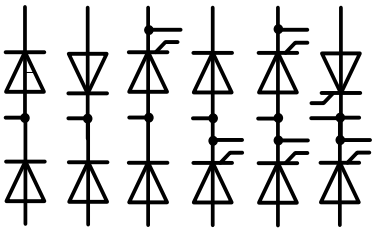
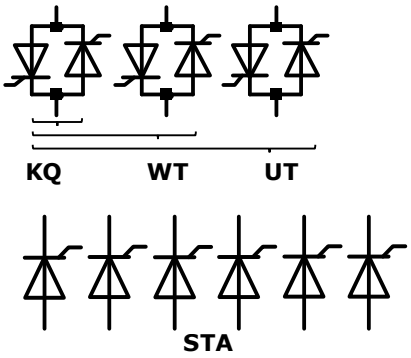
	Single Thyristor/Diode Modules and Thyristor/Diode Pairs	Thyristor/Diodes Halfbridge Modules	AC-Contoller Thyristor Modules
Circurity and designation code			
Product lines	**KE: Single Diode Module** SEMIPACK 1, 2, 3, 4, 6 **ET: Single Thyristor Module** SEMIPACK 4, 6 **TAE: Single Thyristor / Single Diode** SEMITOP 2 **TAA: Two Single Thyristor** SEMITOP 2	**KD: Diode Halfbride Module** SEMIPACK 1, 2, 3, 5 SEMiX 1s, 2s, 3p **KH: Halfbridge Module half-controlled** SEMIPACK 1, 2, 3, 5 SEMiX 2s **KL: Halfbridge Module half-controlled** SEMIPACK 1 **KT: Halfbridge Module full-controlled** SEMIPACK 1, 2, 3, 5 SEMiX 2s **MT / MD: Common Cathode diode or full-controlled halfbr.** SEMIPACK 1	**KQ: Single phase AC-controller** SEMITOP 1, 2 **WT: Two phase AC-controller** SEMITOP 2, 3 **UT: Three phase AC-controller** SEMIPONT 5 SEMITOP 3, 4 **STA: Six single thyristors** SEMITOP 3

Table 7.2.1 Single- and halfbridge thyristor/diode and AC controller modules

7.2.1.2 Type designation codes and module housing images

This chapter provides information on the type designation codes and the housing images of power modules with thyristors and diodes for mains applications from the product lines SEMIPACK, SEMiX and SEMITOP according to Table 7.2.1. Figure 7.2.1 provides an overview of the housing images of thyristor/diode modules from these product lines.

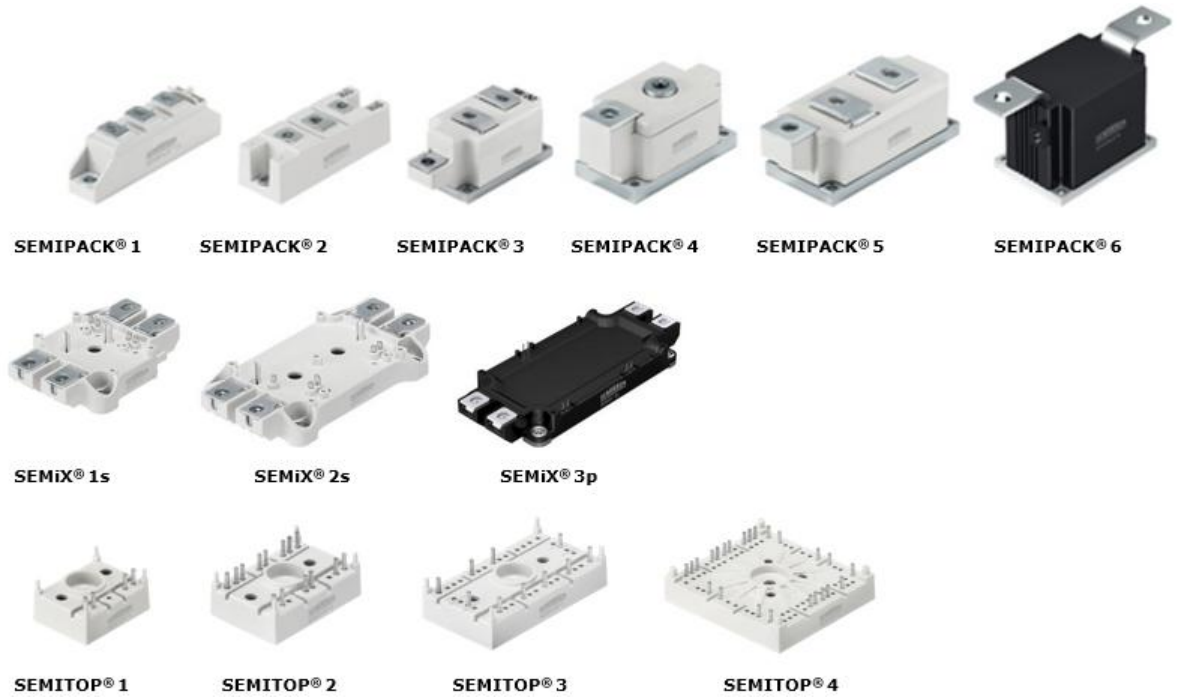


Figure 7.2.1 Housings used for thyristor/diode modules

The product line specific type designation codes for thyristor/diode modules according to table 7.2.1 are shown in Figure 7.2.2 to Figure 7.2.4

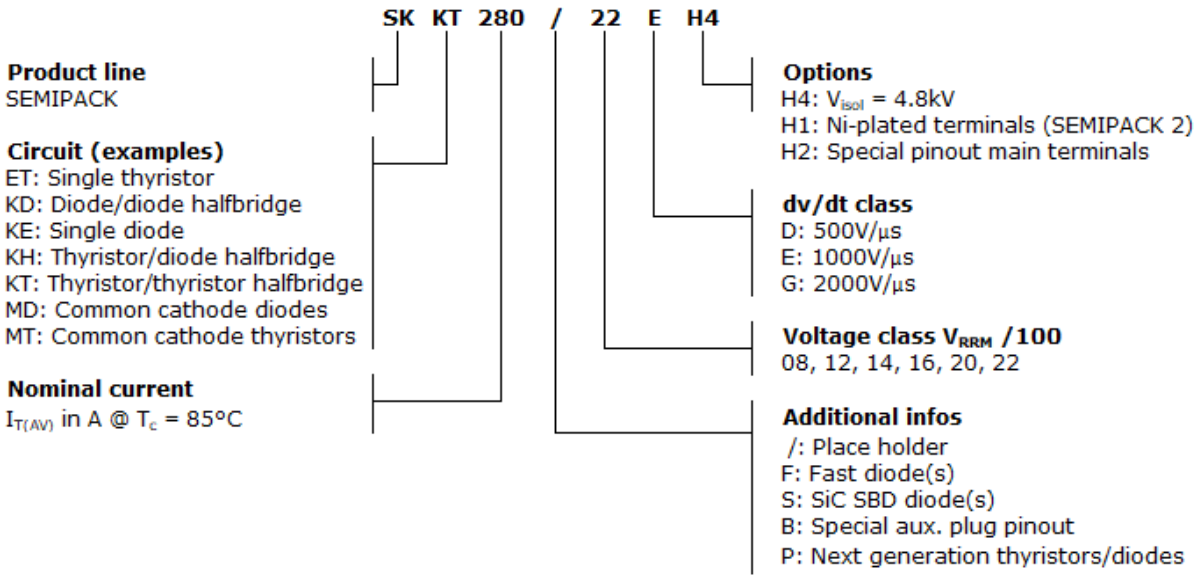


Figure 7.2.2 Type designation code of SEMIPACK thyristor/diode modules

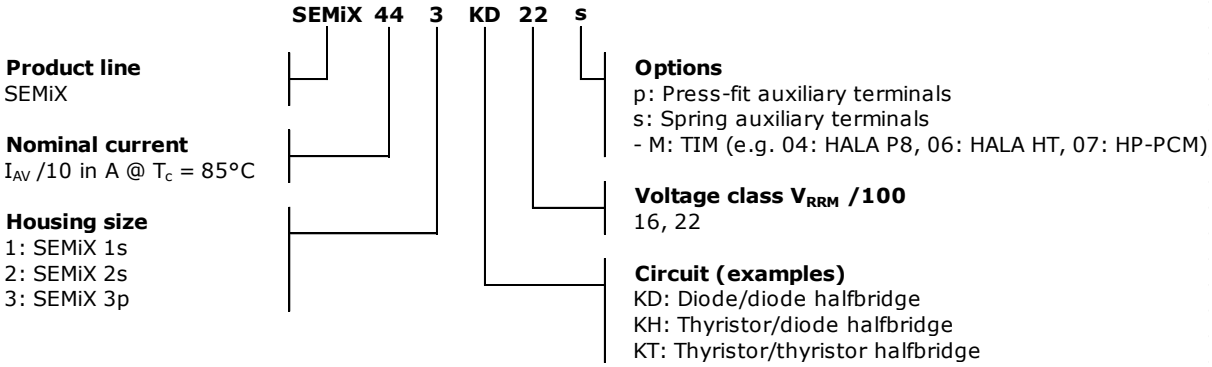


Figure 7.2.3 Type designation code of SEMiX thyristor/diode modules

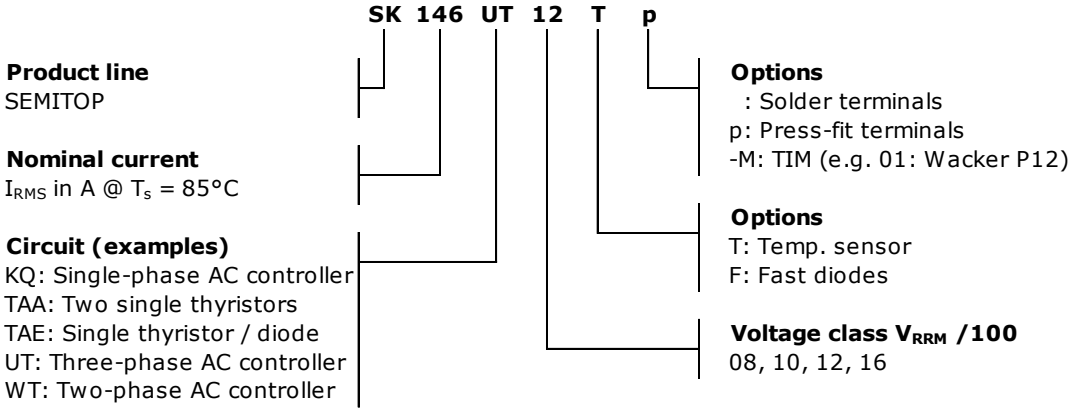


Figure 7.2.4 Type designation code of SEMITOP thyristor/diode modules

7.2.2 Absolute maximum ratings

In the data sheets, the absolute maximum ratings for the separate components of a thyristor/diode module (thyristor, diode, housing, temperature sensor if applicable) are specified separately (Figure 7.2.5). Maximum ratings always refer to one switch (thyristor or diode), hereafter referred to as chip, regardless of whether the switch consists of multiple semiconductor chips connected in parallel.

Absolute Maximum Ratings				
Symbol	**Conditions**		**Values**	**Unit**
Chip				
$I_{T(AV)}$	sin. 180°	T_c = 85 °C	119	A
	T_j = 130 °C	T_c = 100 °C	91	A
I_{TSM}	10 ms	T_j = 25 °C	2250	A
		T_j = 130 °C	1900	A
i^2t	10 ms	T_j = 25 °C	25313	A^2s
		T_j = 130 °C	18050	A^2s
V_{RSM}	T_j = 25 °C		1700	V
V_{RRM}	T_j = 25 °C		1600	V
V_{DRM}	T_j = 25 °C		1600	V
$(di/dt)_{cr}$	T_j = 130 °C		140	A/µs
$(dv/dt)_{cr}$	T_j = 130 °C		1000	V/µs
T_j			-40 ... 130	°C
Module				
T_{stg}			-40 ... 125	°C
V_{isol}	a.c.; 50 Hz; r.m.s.	1 min	3000	V
		1 s	3600	V

Figure 7.2.5 Data sheet section "Absolute Maximum Ratings" of a thyristor module SKKT107/16E

While the specifications of maximum forward [on-state] ratings for most of the SEMIPACK and other modules are usually related to the voltage drop at the terminals. In the data sheets of some newer modules the values refer to chip level, which is clearly marked. A value for the terminal resistance $R_{CC'+EE'}$ is also given in these data sheets.

7.2.2.1 Electrical limit values

Mean forward [on-state] current I_{FAV}, [$I_{T(AV)}$]

The symbols I_{FAV}, [$I_{T(AV)}$] are used to refer to both the mean current values in general and the current limits. The limit values are absolute maximum permissible continuous values for the on-state current load of a diode [thyristor] for sin 180° current shape and given cooling conditions (e.g. case temperature T_c). At this current value, the maximum permissible junction temperature is reached, with no margins for overload or worst-case reserves. The recommended maximum

continuous current is therefore approximately 80% of the current limit for operation at frequencies of between 40Hz and 200Hz.
In general, the usable value depends on the current shape, the current conduction angle and the cooling conditions. This relationship is shown e.g. in Figure 2 of Semikron Danfoss data sheets for discrete thyristors as a set of curves in relation to the case temperature [7.23].
If diodes or thyristors for mains application are operated at frequencies above 50Hz, the switching losses increase by about 2% per 50Hz. For frequencies above 200Hz, the additional losses must be considered in the dimensioning. For frequencies above 500Hz, diodes and thyristors for mains applications are not suitable.
The mean forward current rises proportionate to the decrease in case temperature and breaks off at maximum RMS forward current I_{FRMS} [I_{TRMS}], since this must not be exceeded during continuous operation even at low case temperatures T_c.

RMS forward [on-state] current I_{FRMS}, [I_{TRMS}]

The symbols I_{FRMS}, [I_{TRMS}] are used to refer to both the mean current values and the current limits. The limit values are absolute maximum values of permissible route mean square forward current, averaged over a full operating cycle. The current limit depends on the current carrying capacity of the terminals and connections inside the semiconductor case and is valid for any chosen current waveform, conduction angle and cooling condition. At half sine waves (e.g. AC controller application) the proportion between I_{TRMS} and $I_{T(AV)}$ is

$$I_{TRMS} = \frac{\pi}{2} \cdot I_{T(AV)}$$

Surge forward [on-state] current I_{FSM} [I_{TSM}]

Peak value for a single half sinusoid surge current pulse of 10ms, which the diode [thyristor] is able to withstand without being damaged in the event of a seldom malfunction. The value is specified for T_j = 25°C and T_{jmax}. For 8.3ms (60Hz) the limit will be about 10% higher than the rating for 10ms.
If a diode [thyristor] is exposed to surge forward current load, the junction temperature may temporarily rise to as much as 400°C. Should, however, a reverse voltage occurs immediately after a diode [thyristor] has been exposed to surge current load (self-healing short circuit), the maximum surge forward current is lower than if no subsequent reverse voltage is involved.
In the Figures [8] and 16 in the datasheets of [thyristors] and diodes are shown the current values up to the given surge forward current, the semiconductor chip can withstand at reverse voltage after occasional current surges.

Peak load integral i²t

Reference parameter used to select fuses required for short circuit protection (also see chapter 9.4.5). The peak load integral is calculated from the surge forward current IFSM [I_{TSM}] using the equation:

$$\int_0^{t_{hw}} i_{FS}^2 \, dt = I_{FSM}^2 \cdot \frac{t_{hw}}{2} \quad \text{and} \quad \int_0^{t_{hw}} i_{TSM}^2 \, dt = I_{TSM}^2 \cdot \frac{t_{hw}}{2}$$

t_{hw}: duration of the half sinewave for which I_{FSM} [I_{TSM}] has been specified.

Thus, at 50Hz $t_{hw}/2$ = 5ms; i²t has practically the same value for 60Hz as for 50Hz since the 10% higher I_{FSM} [I_{TSM}] is balanced out by the lower value for t_{hw} ($1.1^2 \cdot 8{,}3ms \approx 10ms$).
The i²t value is given to assist in the selection of suitable fuses to provide protection against damage caused by short circuits and is given for junction temperatures of 25°C and 125°C.
The i²t value of the fuse for the intended input voltage and the prospective short circuit in the device must be lower than the i²t of the diode [thyristor] for t = 10ms.
When the operating temperature increases, the i²t value of a fuse falls more rapidly than the i²t value of the diode [thyristor], a comparison between the i²t of the diode [thyristor] for 25°C and the i²t value of the fuse is generally sufficient.

Non-repetitive peak reverse voltage V_{RSM}

Maximum permissible value for non-repetitive, occasional transient peak voltages in the reverse blocking state of diodes and thyristors at T_j = 25°C…T_{jmax}

Repetitive peak reverse voltage V_{RRM}, [Repetitive peak off-state voltage V_{DRM}]

Maximum permissible values for repetitive transient peak voltages in the reverse [forward] blocking state of diodes and thyristors at T_j = 25°C…T_{jmax}

Figure 7.2.6 illustrates the meaning of the voltage limits for V_R and [V_D]. In addition, "recommended" crest (peak) working off-state and reverse voltage limits V_{RWM} and [V_{DWM}] are marked here, but these are not listed in current Semikron Danfoss data sheets.

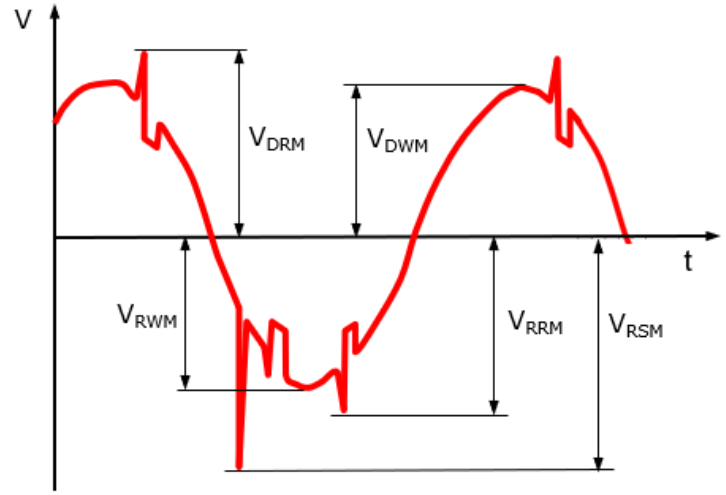


Figure 7.2.6 Example of voltage characteristic

The properties of diodes and thyristors in their blocking states - and thus the above-described permissible voltages - are determined by the avalanche breakdown voltages $V_{(BR)}$ and reverse currents (I_{RD}, [I_{DD}]). Both values increase with the temperature T_j. Therefore, $V_{(BR)}$ degreases with T_j by ~ 0.11%/K (≈ 7% from 25 to -40°C) but I_{RD} and [I_{DD}] drop with temperature degrease by ~ $0.96^{(Tjmax-Tj)}$ (see description of characteristics I_{RD} and [I_{DD}] below). Please refer to chapter 8.1.2 for more detailed information on application-related blocking voltage selection.

Critical rate of rise for thyristor on-state current [$(di/dt)_{cr}$]

Immediately after the thyristor has been triggered, only part of the chips conducts the current flow, meaning that the rate rise of the on-state current has to be limited. The critical rate of rise of on-state current $(di/dt)_{cr}$ represents the highest permissible increase of forward current without damaging the thyristor. Figure 7.2.7 shows the definition of the $(di/dt)_{cr}$ rating according [7.3]. Thyristors with different gate structures (perimeter gate, central gate and amplifying gate) have different permissible values of $(di/dt)_{cr}$.
The Semikron Danfoss data sheet values for $(di/dt)_{cr}$ regarding the IEC standard [7.3] apply for the maximum permissible junction temperature T_{jmax}, a frequency f of 50/60Hz, a current amplitude I_T of three times the mean forward current $I_{T(AV)}$ of the thyristor at sinusoidal half wave and gate current pulses $I_G = 5 \cdot I_{GT}$ with $di_G/dt \geq 1A/\mu s$ and gate trigger pulse duration $t_p \geq 10\mu s$ (see Figure 7.2.7).

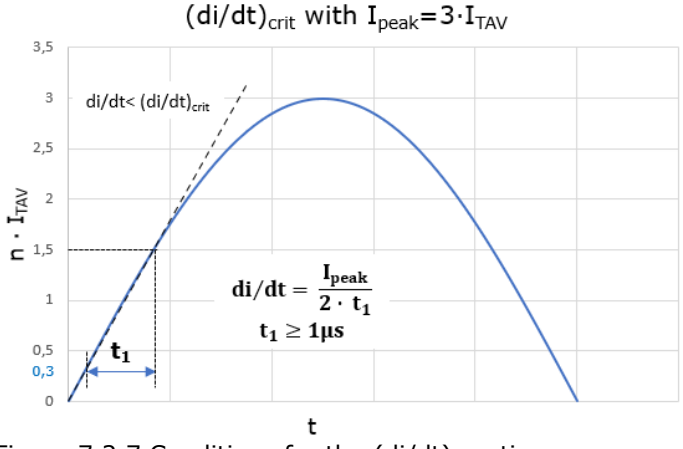


Figure 7.2.7 Conditions for the $(di/dt)_{cr}$ rating

The real di/dt-capability is dependent on various circuit parameters and operating conditions, see also [7.18]. For example, the (di/dt)–capability decreases as T_j, V_D, I_{TM} or f increase. On the other hand, the (di/dt)–capability increases with increasing I_G, di_G/dt, or trigger pulse duration t_p.
For this reason, for frequencies > 60 Hz and pulses with a high rate of rise of current, the peak on-state current must be reduced to values below those given in the datasheets.

Critical rate of rise for thyristor off-state voltage [$(dv/dt)_{cr}$]

Figure 7.2.8 illustrates the conditions for the $(dv/dt)_{cr}$ rating. The values specified apply to an exponential increase in off-state voltage to $0.63 \cdot V_{DRM}$ using method 2 from the IEC standard [7.3]. If these values are exceeded, the thyristor can break over and self-trigger.

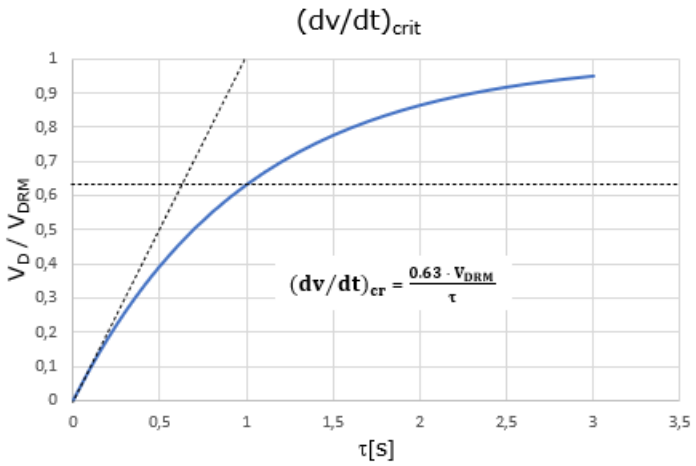


Figure 7.2.8 Conditions for the $(dv/dt)_{cr}$ rating

The Semikron Danfoss data sheet values for $(dv/dt)_{cr}$ were determined with open gate terminal and at the maximum permissible junction temperature T_{jmax}. The (dv/dt)–capability increases with decreasing T_j or decreasing forward supply voltage V_D.

Junction temperature range T_j (min...max)

The most important referential value for calculating limit values is the maximum permissible junction temperature T_j. At most in the event of a circuit fault (e.g. at fuse breaking) this value may be exceeded briefly (cf. "Surge on-state current"). In applications where very low junction temperatures may occur, the blocking voltages that decrease with temperature may have to be taken into account. The lowest permissible T_j value is identical to minimum permissible value of storage temperature T_{stg}.

Storage temperature range T_{stg} (min...max)

The permissible ambient conditions without current or voltage stress are described, among other things, by the permissible temperature range for storage and transport conditions, but also as a limit for operating conditions. The maximum value of T_{stg} is also the maximum permissible case temperature and must not be exceeded by internal or external temperature rise. For thyristor/diode modules, the minimum permissible value of storage temperature T_{stg} of -40°C is limited among others by the properties of the silicon soft-mould and the fatigue of module-internal layers and connections by thermo-mechanical stress.

Insulation (test) voltage V_{isol}

The insulation voltage of a thyristor/diode module is a guaranteed value for the insulation between the terminals and the baseplate. In the data sheets, the RMS values are specified for test durations of 1s and 1min with 50Hz AC. The limit value of V_{isol} for 1s is subject to 100% production testing. During the insulation test, all terminals - including the gate terminals - must be connected to each other. Please refer to [7.19] for more precise information on the testing methods and the relevant standards.

7.2.2.2 Mechanical limit values

Some limits for the mechanical strength of discrete component or module are usually specified in the last lines of the data sheet tables. In some cases, these limits are specified in the characteristics even if they belong to the maximum ratings.

Range for tightening torque to heatsink M_s and to terminals M_t

Undercutting leads to increased thermal contact resistance (and electrical contact resistance at non-isolated components). Exceeding increases the risk of housing cracks or damages of terminal connections.

Maximum amplitude of vibration or shock acceleration a

The maximum permissible value of vibration or shock acceleration in x, y and z direction is limited by the mechanical resilience of all module-internal connections and terminals. Also, for all soft moulded modules at use in rotating applications, the soft mould mass may come away and leak.

Soldering temperature T_{sold} for the terminals of modules with solderable terminals

Maximum temperature to which the output terminals may be exposed when soldered onto a PCB (parameter: exposure time). For some modules, T_{sold} is not listed in the data sheet, but only in the Mounting Instructions.

7.2.3 Characteristics

In the data sheets, the characteristics are likewise specified for one or all switches of the module, hereafter referred to as chip, regardless of whether the switch consists of multiple semiconductor chips connected in parallel. Figure 7.2.9 shows the relevant section of the data sheet using the example of the SEMIPACK 1.6 thyristor module.

Characteristics						
Symbol	Conditions		min.	typ.	max.	Unit
Chip						
V_T	T_j = 25 °C, I_T = 300 A			1.6	1.75	V
$V_{T(TO)}$	T_j = 130 °C			0.8	0.90	V
r_T	T_j = 130 °C			2.80	3.35	mΩ
I_{DD};I_{RD}	T_j = 130 °C, V_{DD} = V_{DRM}; V_{RD} = V_{RRM}				20	mA
t_{gd}	T_j = 25 °C, I_G = 1 A, di_G/dt = 1 A/µs			1		µs
t_{gr}	V_D = 0.67 * V_{DRM}			2		µs
t_q	T_j = 130 °C			200		µs
I_H	T_j = 25 °C			150	250	mA
I_L	T_j = 25 °C, R_G = 33 Ω			300	600	mA
V_{GT}	T_j = 25 °C, d.c.		2.5			V
I_{GT}	T_j = 25 °C, d.c.		100			mA
V_{GD}	T_j = 130 °C, d.c.				0.25	V
I_{GD}	T_j = 130 °C, d.c.				4	mA
$R_{th(j-c)}$	continuous DC	per chip			0.15	K/W
		per module			0.075	K/W
$R_{th(j-c)}$	sin. 180°	per chip			0.2	K/W
		per module			0.1	K/W
$R_{th(j-c)}$	rec. 120°	per chip			0.21	K/W
		per module			0.105	K/W
Module						
$R_{th(c-s)}$	chip			0.09		K/W
	module			0.05		K/W
M_s	to heatsink M5		4.25		5.75	Nm
M_t	to terminals M5		2.55		3.45	Nm
a					5 * 9.81	m/s^2
w				75		g

Figure 7.2.9 Data sheet section "Characteristic Ratings" of a thyristor module SKKT107/16E

Direct forward [on-state] voltage V_F [V_T]

Maximum forward voltage across the main terminals or at chip level at T_j = 25°C for a given current. In addition, the diagramFigure 7.2.10 below, shows on-state characteristics at the typical and maximum forward [on-state] voltage values and at the maximum permissible junction temperature.

Terminal resistance $R_{CC'+EE'}$ (selected module families)

Ohmic Resistance of all internal connections across anode and cathode terminal, measured per switch at T_j = 25°C and $T_j \leq T_{jmax}$

Threshold voltage $V_{(TO)}$ [$V_{T(TO)}$] and forward [on-state] slope resistance r_T

These two values define the forward characteristics (upper value limit) and are auxiliary values for a linear approximation of the forward characteristic to calculate the instantaneous value of the forward [on-state] power dissipation P_F [P_T] or the mean forward [on-state] power dissipation P_{FAV} [P_{TAV}]. As marked in Figure 7.2.10, the forward [on-state] slope resistance r_T is the slope of a I = f(V) curve (Figure 7 of datasheet), interpolated between the T_c = 85°C mean forward [on-state] current datasheet values I_{FAV} [$I_{T(AV)}$] and the value 3 · I_{FAV} [3 · $I_{T(AV)}$].
The threshold voltage V_{T0} [$V_{T(T0)}$] is the voltage at the point of crossover between this approximated line and the voltage axis, see Figure 7.2.10, using the example of thyristor characteristic.

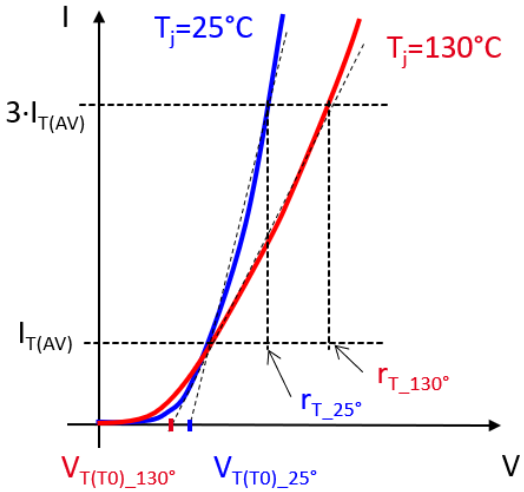


Figure 7.2.10 Definition of the on-state slope resistance r_T

Direct reverse [off-state] current I_{RD} [I_{DD}] (leakage currents)

Maximum reverse [off-state] current at maximum permissible junction temperature T_j and maximum repetitive peak reverse voltage V_{RRM} [peak off-state voltage V_{DRM}].
As illustrated in Figure 7.2.11, the reverse current increases with rising temperature. Approximately, for each 10K increase in temperature, its value increases by a factor of 2 to 2.5:

$$I_{DD}(T_j) = I_{DD}(25°C) \cdot 2 \ldots 2{,}5^{\left(\frac{T_j - 25°C}{10K}\right)}$$

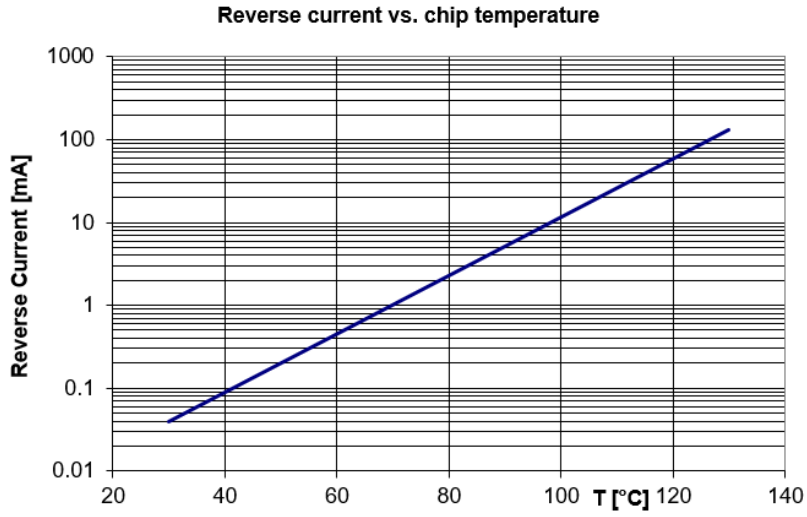


Figure 7.2.11 Thyristor direct reverse current I_{DD} as a function of junction temperature T_j

The direct reverse current rises almost linear to the chip area.

Gate-controlled delay time [t_{gd}] and gate-controlled rise time [t_{gr}]

Time intervals from applying the trigger current until the beginning of the anode-cathode voltage decay to 90% of forward voltage V_D across the thyristor (t_{gd}) and from 90% to 10% of V_D (t_{gr}), see Figure 7.2.12.
The total gate trigger time $t_{gt} = t_{gd} + t_{gr}$ depends on the internal structure of the thyristor and is typically between 3µs and 6µs.

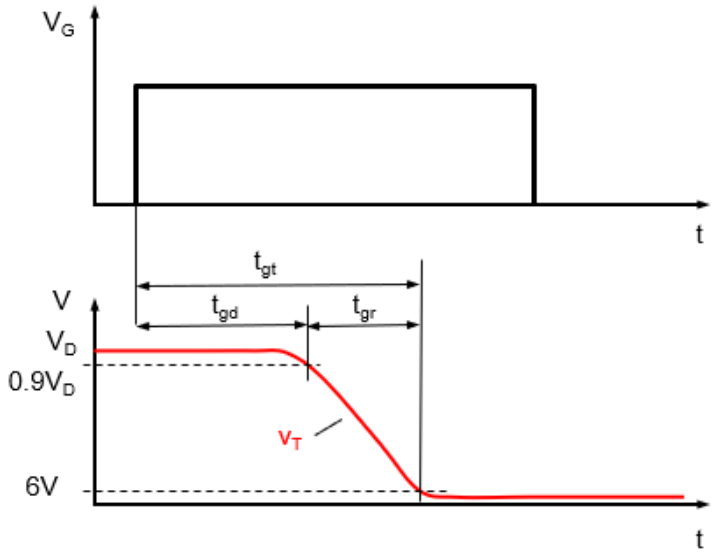


Figure 7.2.12 Time definitions for thyristor triggering

The datasheet specifies a typical value which is applicable, provided the following conditions are fulfilled:

- A square-wave gate pulse, duration 100µs and steepness 1A/µs
- Forward voltage 0.67 · V_{DRM}
- On-state current after trigger approx. 0.1 · $I_{T(AV)}$ @ 85°C
- Junction temperature during trigger process approx. 25°C

Circuit commutated turn-off time [t_q]

The circuit commutated turn-off time is the required time between zero crossing of thyristor current i_T and the earliest re-application of forward off-state voltage, without parasitic turn-on of the thyristor Figure 7.2.13.

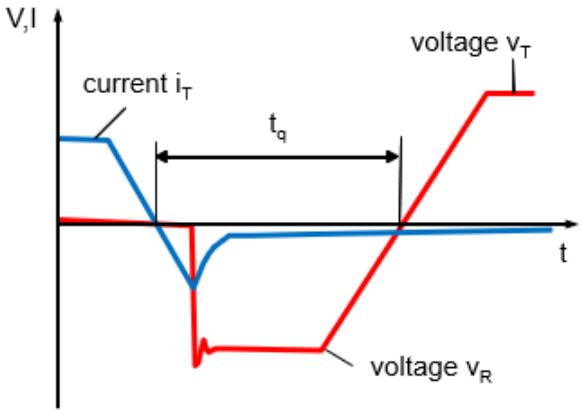


Figure 7.2.13 Characteristic of current i_T and voltage v_T of a thyristor when switched off and definition of commutated turn-off time t_q

The circuit commutated turn-off time t_q of a thyristor rises with increasing junction temperature T_j, increasing peak on-state current I_{TM} before commutation, increasing amplitude and rising steepness of the off-state voltage V_D. On the other hand, t_q degreases in proportion to the steepness $-di_T/dt$ and with increasing reverse blocking voltage V_R. In circuits with an inverse diode connected in parallel to the thyristor, the reverse voltage V_R is only a few volts only and t_q increases by factor about 1.8.

In the case of thyristors for mains applications (e.g. line-commutated converters, AC controllers), the circuit commutated turn-off time is usually of no significance. For this reason, the datasheets contain typical values of several hundred microseconds only, valid up to the maximum permissible junction temperature. There no guarantee is given for these values.

Holding current [I_H]

The holding current I_H is the minimum anode current, which will hold the thyristor in its on-state. Turn-off occurs when the anode current falls below I_H. I_H is given in the data sheet for T_j = 25°C as 98% values of the typical distribution and measured at resistive load with 6V voltage in the main circuit. If the thyristor is triggered at temperatures below 25°C, the values specified may be exceeded.

Latching current [I_L]

The latching current I_L is the lowest anode current at which the thyristor remains in the on state at the end of the trigger pulse lasting 10µs. I_L is also given in the data sheet for T_j = 25°C as 98% values of the typical distribution and measured at resistive load with 6V voltage in the main circuit. The values specified apply to rectangular trigger current pulses with 10µs duration, 1A amplitude, 1A/µs rise slope. I_L increases at lower trigger current and decreases at higher temperature.

Gate trigger current [I_{GT}] and Gate trigger voltage [V_{GT}]

Gate trigger voltage V_{GT} and Gate trigger current I_{GT} are the minimum values of control current and control voltage, which are required at 100µs pulse width for a guaranteed trigger. Shorter control pulses increase I_{GT} between 1.4- and 2-fold; see the example in Figure 7.2.14. In the data sheets, V_{GT} and I_{GT} are specified as minimum values at T_j = 25°C, qualified with DC trigger pulses and DC load.

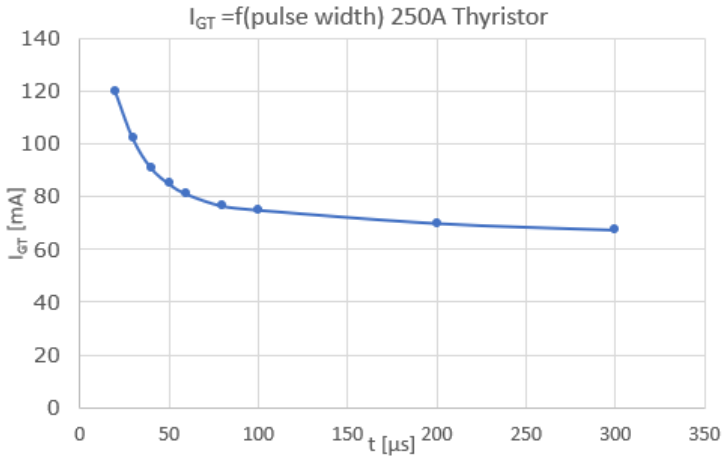


Figure 7.2.14 Measured dependency of the trigger current I_{GT} on the trigger pulse width t_p at a 250A SEMIPACK thyristor module

[Gate Non-trigger current I_{GD} and non-trigger gate voltage V_{GD}]

Below the highest gate non-trigger current I_{GD} or the highest gate non-trigger voltage V_{GD} at the gate, the thyristor will not trigger. Above $V_D \approx 100V$, I_{GD} decreases by up to 30% with increasing voltage. In the data sheets, V_{GD} and I_{GD} as maximum values at the highest permissible T_j, qualified with DC trigger pulses and DC load. Table 2.2.2 in chapter2.2.4.1 illustrates the dependency of trigger characteristics on circuit parameters and operating conditions. For example, I_H, I_L and I_{GD} decrease as T_j or V_D increases and I_{GT} decreases with increasing T_j, I_G and di_G/dt, [7.18].

Thermal resistances of thyristor/diode modules

Thermal resistances may be used to calculate true constant quantities, as well as average temperatures of periodic functions. Normally, however, the current conducted through a semiconductor device and, consequently, the power losses, are time-dependent parameters.
In mains applications, the losses and temperatures vary within the bounds of the line frequency around a mean value. The junction temperature T_j is higher under peak load than under direct current load or if calculated with a mean power loss P_{FAV} [P_{TAV}] and $R_{th(j-c)}$. $T_{j(max)}$ depends on the current waveform and the current flow time within a cycle and can be calculated by using p(t) and the thermal impedance $Z_{th(j-c)}$.

Historically grown, owing to the formerly more restricted methods of calculation, the datasheets of previous thyristor/diode modules and discrete mains diodes and thyristors contained auxiliary values. These values should enable the user to factor in the load dependent power loss and temperature fluctuation based on the current waveform and the lead angle. Although not correct from a physics point of view, for this the static resistance $R_{th(j-c)}$ is used as a mathematical aid and is multiplied by a corrective factor in order to project the mean temperature to the maximum temperature value. The resulting value $R_{th(j-c)}$, which is given either as a pure operand or in the form of a diagram, applies to the given current waveform and the lead angle for a frequency range of 40…60 Hz. In other words, rec 120° stands for "rectangular current with a current flow time of 120°".

Thermal resistance $R_{th(j-c)}$ per chip and per module (halfbridge modules with baseplate)

In the data sheets of thyristor/diode modules, each switch is usually referred to as a thyristor or diode chip. The thermal resistances are likewise specified for one or all switches of a module in parallel.

Thermal resistance $R_{th(c-s)}$ per chip and per module (halfbridge modules with baseplate)

Contact thermal resistance for the heat flow from the module baseplate to the heatsink $R_{th(c-s)}$ per chip applies provided the assembly instructions are followed. The $R_{th(c-s)}$ per module represents the thermal resistance at thermal paralleling the $R_{th(c-s)}$ of diode [thyristor] chips to module baseplate. Since halfbridge modules normally have the same chip areas in both switches, $R_{th(c-s)}$ per module is $½ \cdot R_{th(c-s)}$ per chip here applies.
In new or updated data sheets from 2020 onwards for SEMIPACK halfbridge modules, the previously used reference point T_{s1} to measure heatsink temperature is replaced by the reference point T_{s2}, as it is already used for other module families, see [7.21], [7.22]. Figure 7.2.15 illustrates this change. The changed reference point T_{s2} is used already in the datasheets for SEMiX 3p, SEMiX 5 and SEMiX 6p baseplate thyristor/diode and bridge rectifier modules.

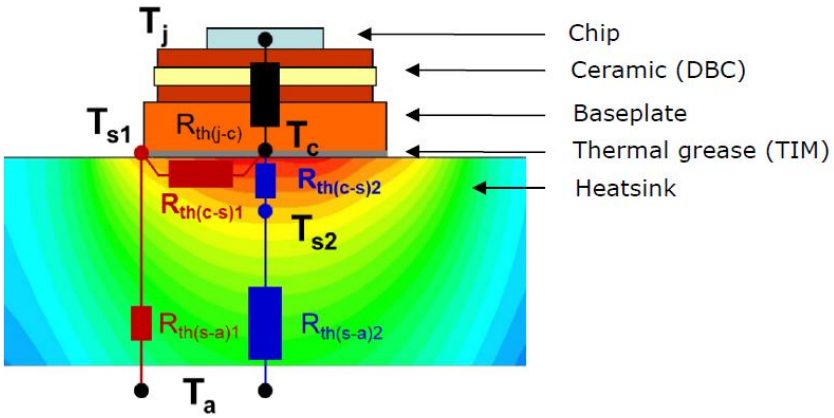


Figure 7.2.15 Different reference points for calculations of thermal resistances in a module with baseplate

Some recent data sheets of such thyristor/diode modules contain even additional information on $R_{th(c-s)}$ according to different specifications, e.g.:

- $R_{th(c-s)}$ per chip for two different thermal interface materials (Wacker P12 with λ = 0.81W/(m·K) and Semikron Danfoss pre-applied phase changer material)
- $R_{th(c-s)1}$ per module, calculated without thermal coupling of switches
- $R_{th(c-s)2}$ per module with thermal coupling (reference point underneath module, thermal interface material with λ = 0.81W/(m·K) respective Semikron Danfoss pre-applied phase changer material

For a more detailed explanation of the physical correlations of R_{th}, please refer to chapter 3.2.3 and for TIM see chapter 5.3.

Thermal resistance $R_{th(j-s)}$ per switch for heatsink rated baseplate-less modules

Since an individual determination of $R_{th(j-c)}$ is not possible for thyristor/diode baseplate-less modules (e.g. SEMITOP, MiniSKiiP), the thermal resistances $R_{th(j-s)}$ per switch are given for such modules instead. Because here is only a very limited thermal coupling between the chips inside the DBC, the values are specified for a heatsink temperature measured underneath the chips.

7.2.4 Diagrams

The diagram part for datasheets of Semikron Danfoss thyristor/diode modules begin with a sequence of diagram pairs to support an initial rough dimensioning based on typical device data:

- Current – Power Dissipation – required Cooling
- RMS-Current – Power Dissipation – required Cooling (AC Controller Application)
- Direct Current – Power Dissipation – required Cooling (B2 Rectifier Bridge Application)
- RMS or Direct Current – Power Dissipation – required Cooling (3-Halfbridge AC Controller and B6 Rectifier Bridge Application)

The usage of these diagrams is described below using the example of the diagrams from datasheet figure 1 for estimating power dissipation and required cooling conditions as a function of a thyristor's current I_{TAV} and the current waveform.

Power dissipation and maximum permissible values

These diagrams demonstrate the usable current per switch or per module for different circuit configurations, depending on the current shape, the current conduction angle and the cooling conditions. A set of curves is given representing the required $R_{th(j-a)}$ in relation to the ambient temperature or of required $R_{th(c-a)}$ for a resulting case temperature (Figure 7.2.16).
Left diagram (L): Typical mean on-state power dissipation P_{TAV} per chip (switch) as a function of the mean on-state current I_{TAV} for DC (cont.), sinusoidal half waves (sin. 180) and square-wave pulses (rec. 15...180).
Right diagram (R): Maximum permissible power dissipation P_{TAV} per chip (switch) as a function of ambient temperature T_a and thermal resistance $R_{th(j-a)} = R_{th(s-a)} + [(R_{th(j-c)} + R_{th(c-s)})$ per chip]

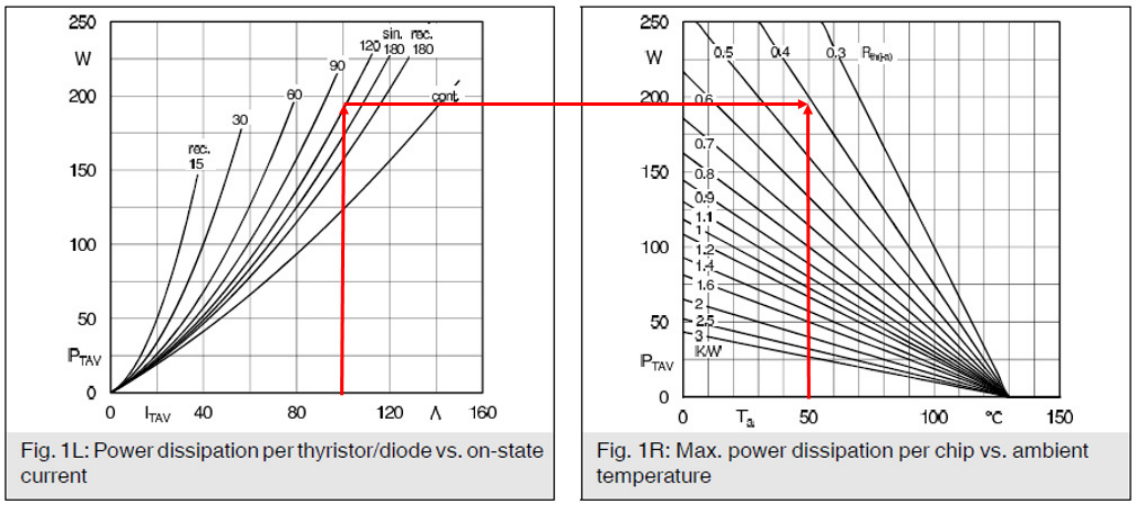


Fig. 1L: Power dissipation per thyristor/diode vs. on-state current

Fig. 1R: Max. power dissipation per chip vs. ambient temperature

Figure 7.2.16 Use of datasheet figures 1L and 1R of a SEMIPACK module SKKT107/16E

The example marked in red in the figure can be read as follows:
For 100A I_{TAV} per chip in a B6 rectifier application (rec. 120°) can be read from Figure 1L a power dissipation P_{TAV} per chip of approx. 195W. Regarding fig. 1R, at 195W P_{TAV} and a maximum ambient temperature T_a of 50°C the thermal resistance $R_{th(j-a)}$ per chip to ambient must be about 0.42K/W at most. At $R_{th(j-a)}$ = 0.42K/W, the chips are heated to the maximum permissible junction temperature of 130°C. Since the diagrams are based on typical component values, it is recommended to undercut the maximum temperature by 10% to 20%. For this, a heatsink with lower $R_{th(s-a)}$ is required.

Reverse recovery charge Q_{rr}

Q_{rr} is the total recovered charge that flows through the main circuit (current-time area) at commutation during the reverse recovery time t_{rr}. The corresponding characteristic in the datasheet (see Figure 7.2.17) shows this value's dependence on the forward current falling rate di_T/dt as well as the peak on-state current I_{TM} before commutation at a junction temperature $T_j = T_{jmax}$ (typical values).

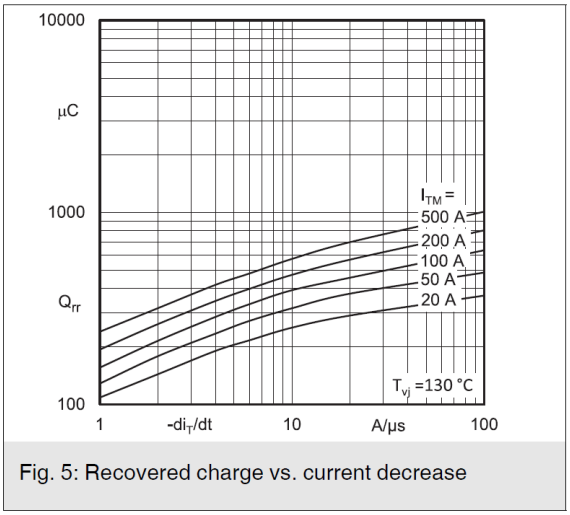


Fig. 5: Recovered charge vs. current decrease

Figure 7.2.17 Thyristor's recovered charge versus current degrease of SKKT107/16E

Figure 7.2.18 shows the schematic current curve during commutation and illustrates the integration limits defined according to IEC60747-6 [7.3]

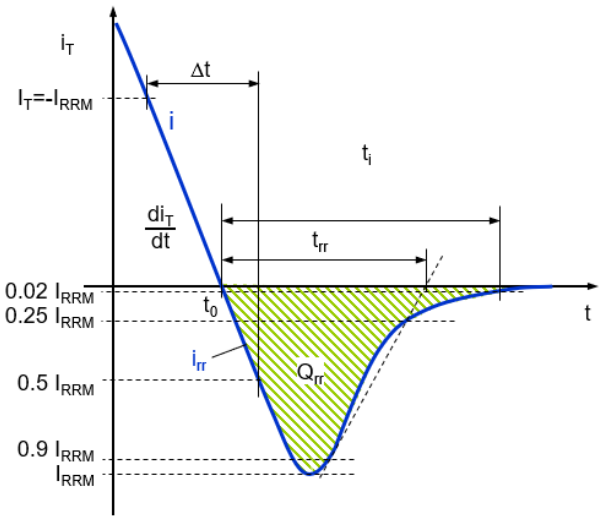


Figure 7.2.18 Schematic current curve during commutation and integration limits

According to the definition in Figure 7.2.18 is:

$$-\frac{di_T}{dt} = \frac{1.5 \cdot I_{RRM}}{\Delta t}$$

For simple estimations, often are used the following approximation equations:

$$I_{RRM} = 2 \cdot \frac{Q_{rr}}{t_{rr}}$$

$$t_{rr} = \sqrt{2 \cdot \frac{Q_{rr}}{\frac{-di_T}{dt}}}$$

Transient thermal impedances $Z_{th(j-c)}$ and $Z_{th(j-s)}$

The transient thermal impedances $Z_{th(j-c)}$ (junction to case) and $Z_{th(j-s)}$ (junction to heatsink) are given for a single chip (switch) as a function of the time t elapsed after a step change in power dissipation. For modules with baseplate, a diagram according to Figure 7.2.19 a) is shown in the data sheets. For baseplate-less modules only a $Z_{th(j-s)}$ (junction to heatsink) can be specified, a diagram according to Figure 7.2.19 b) is shown in the data sheets.

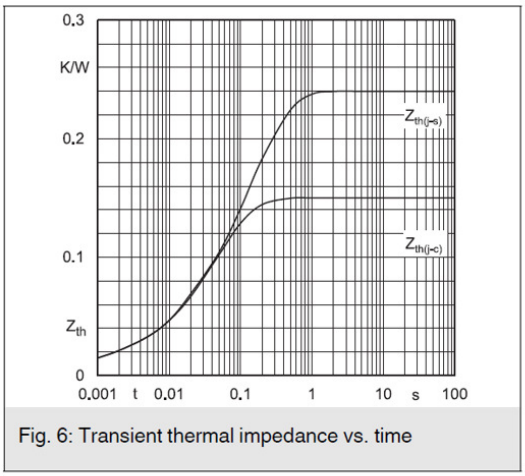


Fig. 6: Transient thermal impedance vs. time

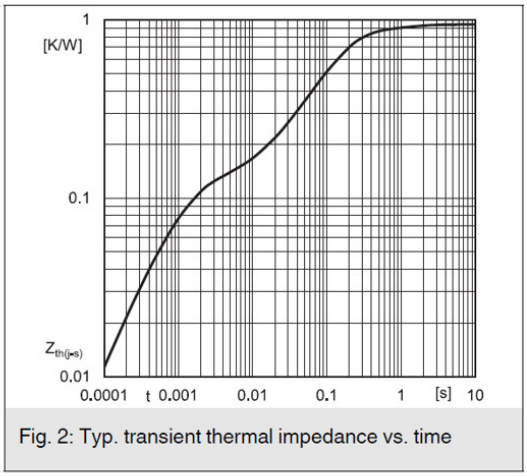


Fig. 2: Typ. transient thermal impedance vs. time

a) b)

Figure 7.2.19 Courses of transient thermal impedances vs. time: a) SEMIPACK module SKKT107/16E (with baseplate); b) SEMITOP module SK55TAA12p (without baseplate) [7.20]

The transient thermal impedances are defined as a quotient of the time function of a temperature difference divided by the impressed power dissipation:

$$Z_{th}(t) = \frac{T_1(t) - T_2(t)}{P}$$

The static upper range value is the actual thermal resistance. The thermal impedance is used to calculate the temperature change at a specified point in time after power dissipation has been effective. Thus, it is possible to calculate the effective junction temperature $T_j(t)$ for any given duration of power dissipation.
In Semikron Danfoss's simulation program, SemiSel the Foster model is used for simulation:

$$Z_{th}(t) = R_1(1 - e^{\frac{-t}{\tau_1}}) + R_2(1 - e^{\frac{-t}{\tau_2}}) + \ldots + R_n(1 - e^{\frac{-t}{\tau_n}})$$

As already mentioned with the thermal resistances, in new or updated data sheets for SEMIPACK modules from 2022 onwards, the previously used reference point T_{s1} will be replaced by the reference point T_{s2}, as it is already used for other module families, [7.21], [7.22].

Forward [On-state] characteristics V_F, [V_T]

The diagrams contain curves for the forward voltage V_F [on-state voltage V_T], depending on diode forward DC current I_F or thyristor on-state DC current I_T for typical and maximum component values (Figure 7.2.20).

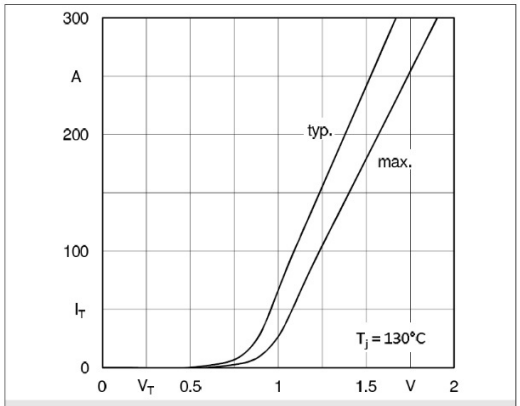


Fig. 7: On-state characteristics

Figure 7.2.20 On-state characteristics of SKKT107/16E

The example of an actual SEMIPACK datasheet shows the curves at T_{jmax} (130°C), but some older datasheets show the curves at lower temperatures too. Because of its negative temperature coefficients, V_T and V_F are higher at lower reference temperatures than used in the diagrams.

Surge overload current $I_{F(ov)}$ [$I_{T(ov)}$] vs. time

In case of a permissible overload the surge current determined by the grid impedance and mains voltage has to be survived. For this reason, data sheets contain a diagram, shown in Figure 7.2.21 a). The surge on-state (forward) characteristic contains curves of the overload current $I_{F(ov)}$ or $I_{T(ov)}$, permitted in the event of malfunction as function of pulse duration t, related to surge current I_{FSM} [I_{TSM}] under different reverse voltage conditions (ratio between applied reverse voltage V_R and peak reverse blocking voltage V_{RRM}) directly after the last half-sine wave (Figure 7.2.21 a)).
Up to 10ms pulse duration, the time t means the overload pulse duration. For t > 10ms, t refers to an overload sequence duration with sinusoidal half wave currents in intervals of 20ms/50Hz (Figure 7.2.21 b)).

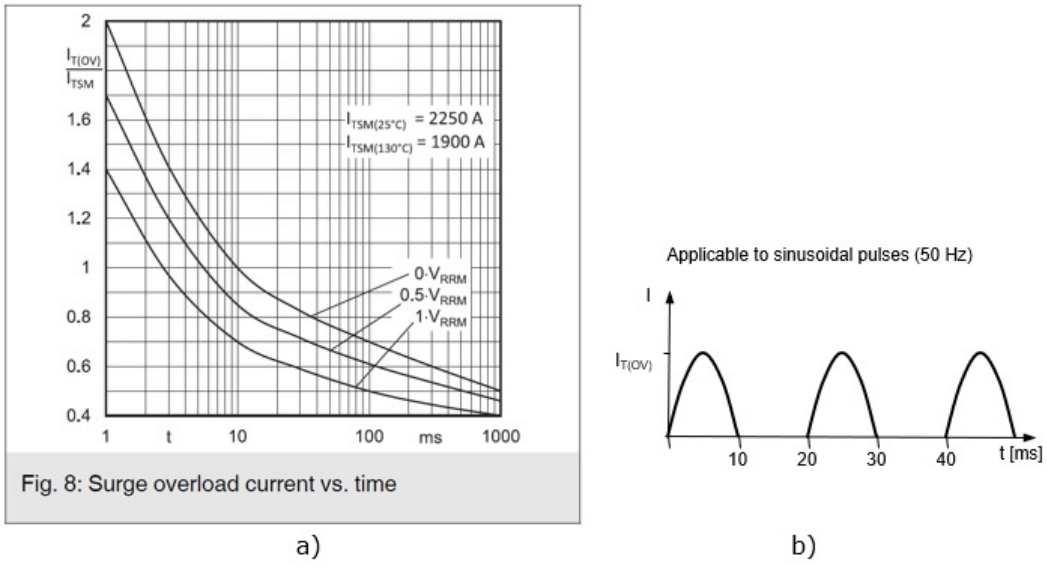


Figure 7.2.21 a) Surge overcurrent characteristics of SKKT107/16E; b) Permissible overload pulse sequence

The parameter of the three depicted curves is the applied reverse voltage V_R of a single thyristor or diode. Depending on the fault case (topology, position and number of failed thyristors or diodes), the curves for $V_R = 0 \cdot V_{RRM}$ to $V_R = 1 \cdot V_{RRM}$ applies. If the current is only limited by external measures, the current decreases analogously according to remaining voltage (current reduction between the curves for $V_R = 0.5 \cdot V_{RRM}$ and $V_R = 1 \cdot V_{RRM}$). The selection of overload protective devices depends on the expected overload conditions, see also chapter 8.4.6 below.

Gate trigger characteristics [$V_G=f(I_G)$]

The gate trigger characteristics shown in the datasheet figure 9 of SEMIPACK 1.6 thyristor/diode modules datasheets describe the possible deviation ranges of the gate-cathode voltage V_{GC} as a function of the gate current I_G at trigger pulses with 100µs minimum duration. Trigger current I_{GT} and trigger voltage V_{GT} at T_j = 25°C as well as highest non-triggering gate current I_{GD} and highest non-triggering gate voltage V_{GD} are marked in the diagram at T_j = 25°C and at the minimum and maximum permissible junction temperature (Figure 7.2.22).
Gate pulses under 100µs will affect an increase in the minimum gate trigger current and voltage values by a factor of 1.4 to 2. The driver unit should ensure that the trigger current value given in the datasheet is exceeded by a factor of four or even five. The relatively wide spread between the two extreme curves takes several physical effects into account:

- The temperature dependence of the gate cathode voltage over the entire operating temperature (lower limit: minimum expected DC voltage at T_{jmin}; upper limit: the highest expected dynamic voltage at T_{jmax}).
- The dynamic gate-cathode voltage as a function of the charge carrier concentration in the gate region, the internal impedances and the di/dt of the anode current. Especially in an amplifying gate structure, a high di/dt results in a high voltage drop in the internal main gate resistance. This result in a higher gate-cathode voltage required for triggering, than the steady-state value given in the datasheets.

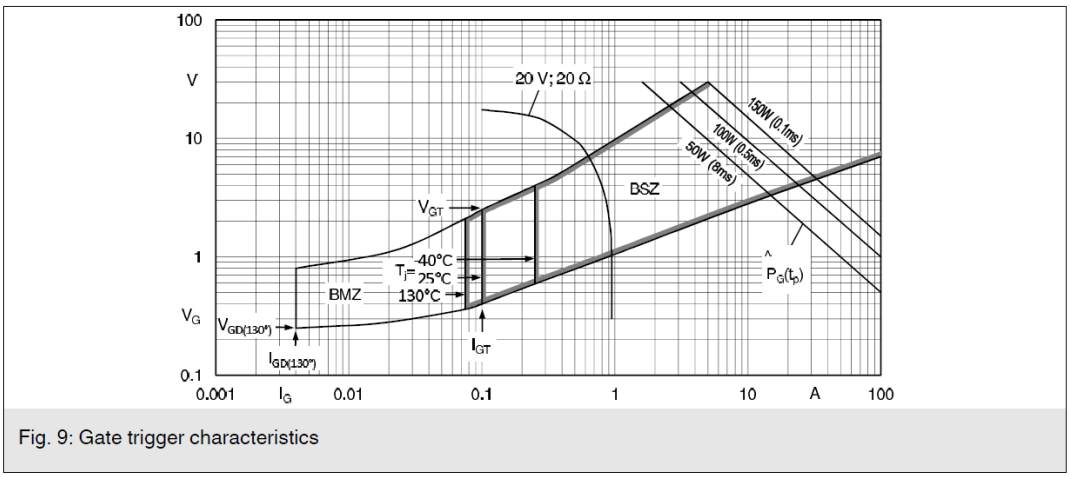


Fig. 9: Gate trigger characteristics

Figure 7.2.22 Gate trigger characteristics of SKKT107/16E

The diagram includes the temperature-dependent trigger ranges of possible trigger (BMZ German for: "**B**EREICH **M**ÖGLICHER **Z**ÜNDUNG") and safe trigger (BSZ German for "**B**EREICH **S**ICHERER **Z**ÜNDUNG") at T_j = 25°C and at the minimum and maximum permissible junction temperature. The I_{GT} sinking with rising temperature causes the BSZ to expand to smaller gate currents as the temperature increases. An operating point in the BMZ must be avoided for intentional trigger currents as well as residual currents or coupled interference currents that could inadvertently lead to triggering. The current-voltage characteristic of a trigger circuit output stage has to ensure that the current and voltage of the trigger pulses are within the BSZ over the full operating temperature range.
The diagram also contains limiting curves of the permissible peak trigger power loss $\hat{P}_G(t_p)$ for trigger pulse durations t_p of 100µs, 500µs and 8ms is not exceeded. Note that Semikron Danfoss and most other manufacturers data sheets do not contain a value for the maximum continuous gate power losses for DC gate current operation. Here, P_G should be less than 10W. Also shown in the diagram is an exemplary characteristic of a trigger circuit with 20V no load voltage, 20Ω internal resistance and – respectively – 1A short circuit current of the trigger circuit output stage.

7.2.5 Deviating structure of data sheets for older thyristor/diode modules

The data sheet structure of older thyristor/diode halfbridge modules differ slightly from the examples given before. The limit value specifications are preceded by another table that gives an initial overview of the voltage and current limit values and the tabular data sheet information does not explicitly distinguish between limit and characteristic values. In addition, the data sheets contain information on the possible output current in B2, B6, W1C and W3C circuit under selected cooling conditions.

7.2.6 Bridge rectifier modules - additional datasheet specifications

The explanations in the previous chapters were based on the example of single- and halfbridge-modules with diodes and thyristors as well as AC controller modules. This chapter contains additional information on the data sheet specifications of power modules that contain complete rectifier bridges.

7.2.6.1 Bridge rectifier modules and type designation

Bridge Rectifier Power Modules are available for a wide power range, in different topologies and housings. The Table 7.2.2 shows the most common topologies of the bridge rectifier modules and the product lines in which these are being integrated.

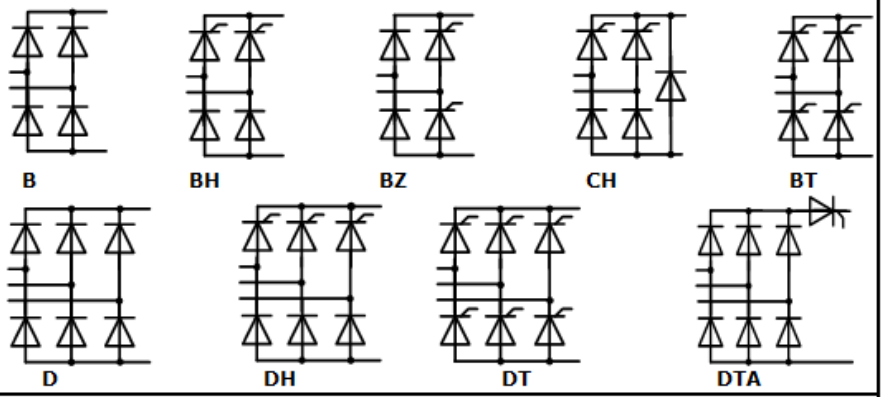
	Bridge Rectifier Modules (without Brake choper)
Circurity and designation code	
Product lines	**B: Single Phase Diode Bridge** SEMIPONT 1, 2, 3 SEMITOP 2 **BH, BZ: Single Phase Bridge, half-controlled** SEMIPONT 1 SEMITOP 2 (BZ) **BH, BZ: Single Phase Bridge, half-controlled + freewheeling diode** SEMIPONT 1, 2 **BT: Single Phase Bridge, full-controlled** SEMIPONT 1, 2, **D: 3-Phase Diode Bridge** SEMIPONT 1, 2, 3, 4, 5 SEMITOP 2 MiniSKiiP 3 (AN) SEMiX 6p SEMiX 13s **DH: 3-Phase Bridge, half-controlled** SEMiX 5 SEMITOP 3 **DT: 3-Phase Bridge, full-controlled** SEMIPONT 2, 5 SEMITOP 3 **DTA: 3-Phase Bridge + thyristor** SEMITOP 3

Table 7.2.2 Bridge rectifier circuits with corresponding modules

Figure 7.2.23 provides an overview of the housing images offering bridge rectifier topologies.

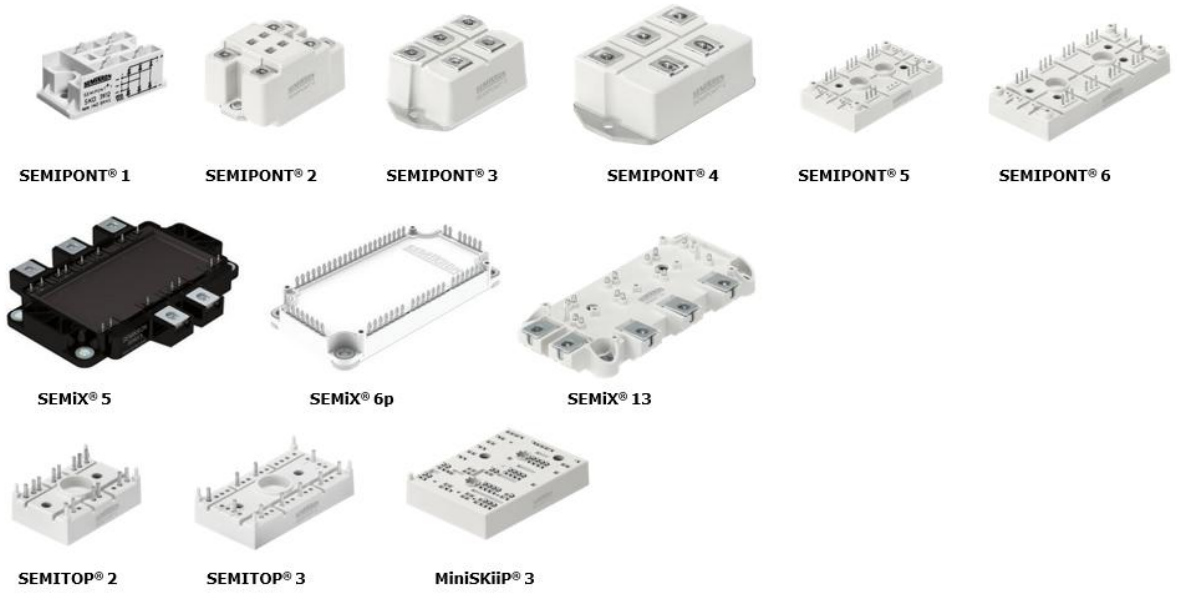


Figure 7.2.23 Housings used for bridge rectifiers

The product line specific type designation codes for bridge rectifier and some AC controller modules are shown in Figure 7.2.24 to Figure 7.2.27:

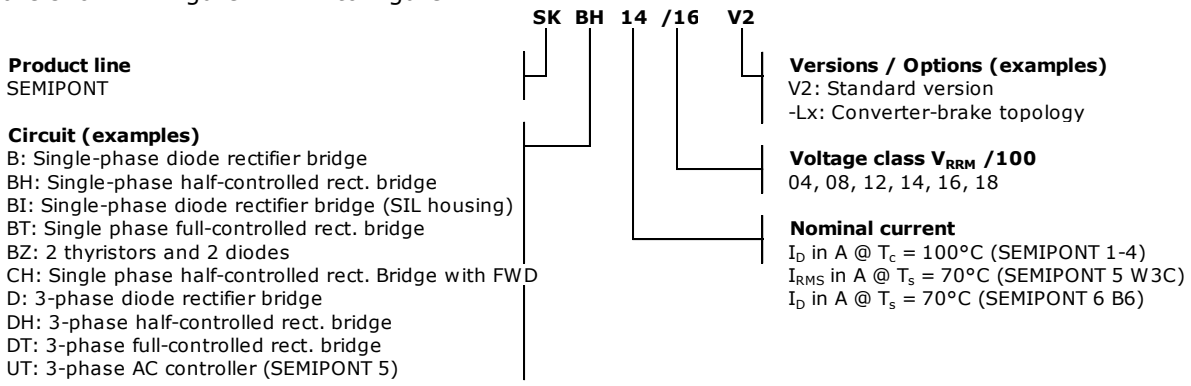


Figure 7.2.24 Type designation code of SEMIPONT bridge rectifier and AC controller modules

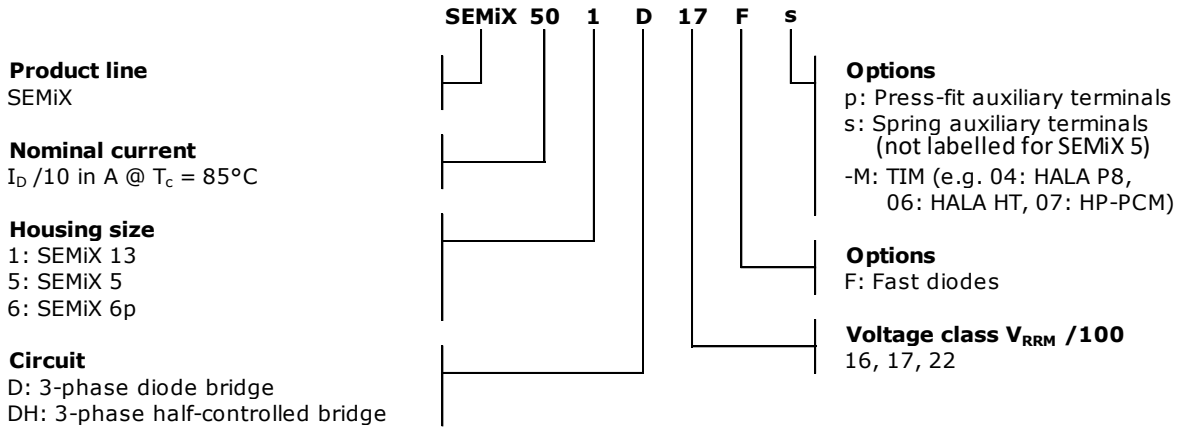


Figure 7.2.25 Type designation code of SEMiX bridge rectifier modules

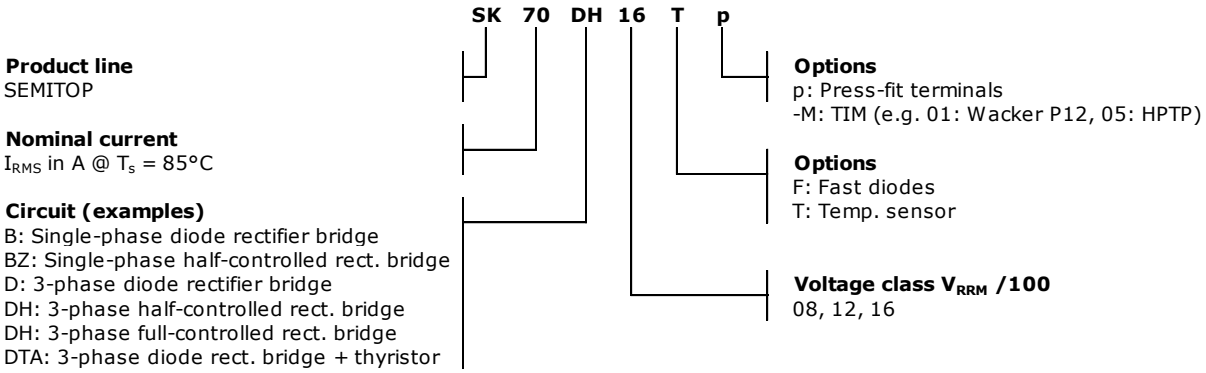


Figure 7.2.26 Type designation code of SEMITOP bridge rectifier modules

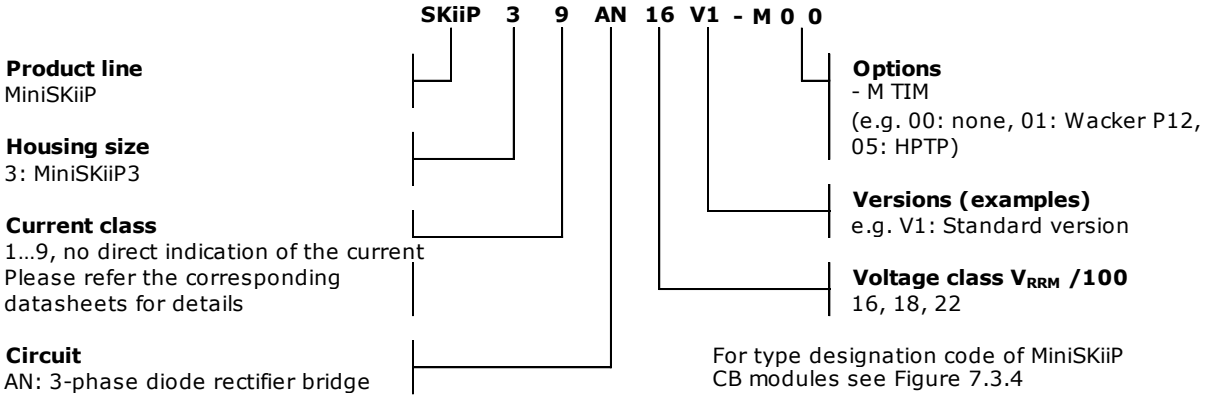


Figure 7.2.27 Type designation code of MiniSKiiP bridge rectifier modules

7.2.6.2 Device parameters

At the head of a bridge rectifier data sheet, a small table is added listing the blocking voltages V_{RSM}, V_{RRM} and V_{DRM} (if applicable) as well as the highest possible output direct current at full conduction and a specified heatsink temperature. The data sheet table contains for two different case temperatures T_c the maximum output direct current I_D at full conduction, and – per diode or thyristor - the limit values for I_{FSM} [I_{TSM}] and i²t, the forward characteristics V_F, [V_T], $V_{(T0)}$ [$V_{T(T0)}$], r_T and the reverse current I_{RD} and I_{DD} per diode [thyristor] switch. As with the other power semiconductors, the maximum permissible temperature ranges for operation (T_j) and storage (T_{stg}) as well as insulation test voltage V_{isol}, tightening torques for housing and terminals, module weight and case description are included in the table.
Also indicated are the thermal resistances $R_{th(j-c)}$, $R_{th(j-s)}$ or $R_{th(j-a)}$ per diode or thyristor switch as well as $R_{th(c-s)}$ per bridge rectifier module with baseplate. The specification of thermal resistances indicates to which class the module belongs, e.g. for mounting on heatsink baseplate modules ($R_{th(j-c)}$, $R_{th(c-s)}$), or baseplate-less modules ($R_{th(j-s)}$), cooling surface or free-standing resp. mounting on insulator or PCB.
For bridge rectifiers with integrated brake chopper, the data sets correspond to those of the IGBT and fast freewheeling diodes used.

7.2.7 Discrete thyristors and diodes – particular datasheet specifications

7.2.7.1 Type designation codes and housing images

The Figure 7.2.28 provides an overview of exemplary housings used for discrete diodes and thyristors.



Figure 7.2.28 Housings used for discrete diodes and thyristors

The type designation codes of discrete thyristors and diodes is shown in Figure 7.2.29. The Figure 7.2.30 shows the type designation code for high voltage axial screw diodes.

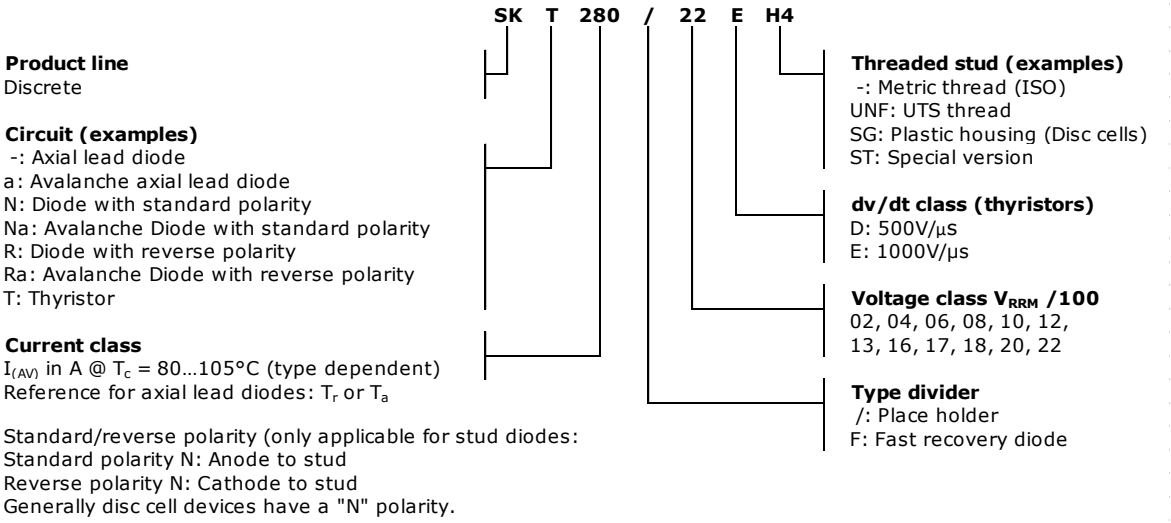


Figure 7.2.29 Type designation code of discrete thyristors and diodes

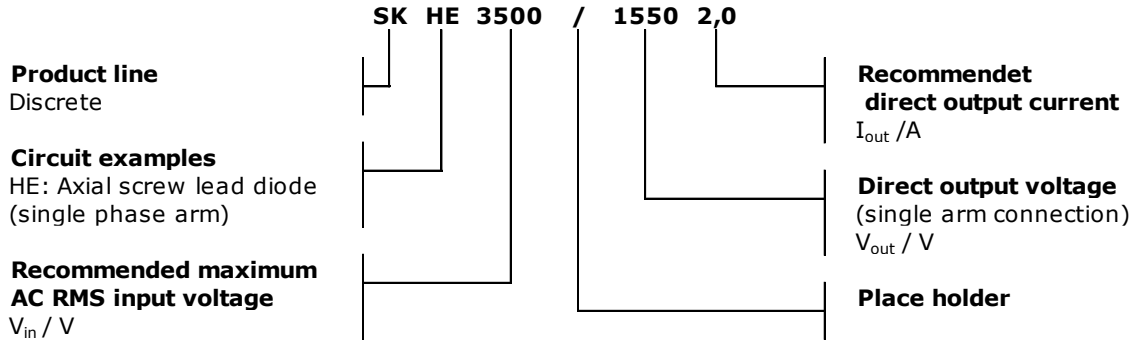


Figure 7.2.30 Type designation code of high voltage axial screw diodes

7.2.7.2 Particular datasheet specifications

Thermal resistance $R_{th(j-c)}$ and $R_{th(c-s)}$ for discrete diodes and thyristors

For discrete diodes and thyristors with metal cases, the information for $R_{th(j-c)}$ and $R_{th(c-s)}$ applies accordingly. The measuring point for T_c here is as follows:

- in metal cases with threaded studs: the centre of one of the flats on the hexagonal base,
- in disc type devices: any point on the outer edge of the round copper base

For disc type thyristors and diodes, these thermal resistances for single-sided and double-sided cooling are specified separately (Figure 7.2.31).

Characteristics						
Symbol	Conditions		min.	typ.	max.	Unit
Chip						
$R_{th(j-c)}$	continuous DC	SSC				K/W
		DSC			0.021	K/W
$R_{th(j-c)}$	sin. 180°	SSC			0.054	K/W
		DSC			0.0225	K/W
$R_{th(j-c)}$	rec. 120°	SSC			0.06	K/W
		DSC			0.027	K/W
Module						
$R_{th(c-s)}$	SSC			0.01		K/W
	DSC			0.005		K/W

Figure 7.2.31 Data sheet excerpt thermal characteristic ratings for a disc type thyristor SKT1200/18E [7.23]

For discrete diodes with plastic housings and axial leads, integrated in the circuit via solder connections, often values for $R_{th(j-r)}$ and $R_{th(j-a)}$ are specified, because heat transfer via the terminals plays a very important role:

- $R_{th(j-r)}$: Thermal resistance between diode chip and PCB surface at a defined length of the connection wires,
- $R_{th(j-a)}$: Thermal resistance between diode chip and ambient at a defined copper-plated PCB mounting area.

Mean on-state or forward current I_{FAV} [I_{TAV}] vs. case temperature T_c for direct current (cont.), half sine waves (sin.) and rectangular pulses (rec.) for different current conduction angles θ

Maximum permissible forward current, averaged over a full operating cycle. This value depends on the current shape, the current conduction angle and the cooling conditions. A relationship is shown as a set of curves in relation to the case temperature (Figure 7.2.32).
The mean on state (forward) current is assigned particular importance as an orientation value for one half sine wave of half a load cycle (current conduction angle 180°) at a case temperature of approx. 85°C. Because the selected figure 2 is part of disc thyristors datasheet, there are different diagrams for single side and double side cooling.

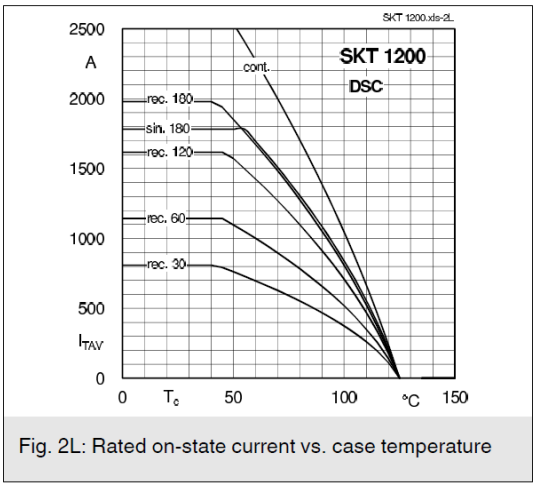


Fig. 2L: Rated on-state current vs. case temperature

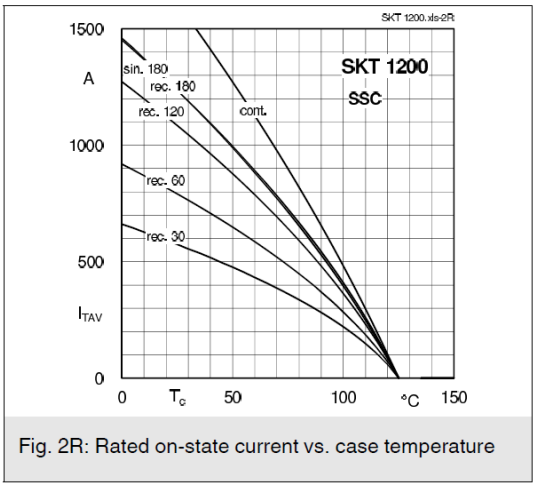


Fig. 2R: Rated on-state current vs. case temperature

Figure 7.2.32 Rated on-state current of a disc type thyristor SKT1200/18E versus case temperature at double side cooling (DSC) and single side cooling

Supplementary thermal impedance [$Z_{th(z)}$]

Although not correct from a physics point of view, in these datasheets the thermal impedance is indicated with a supplementary value in order to infer the maximum temperature from the average dissipated power. The Figure 7.2.33 gives such thermal supplementary impedances $Z_{(th)z}$ for different current conduction angles of sine and rectangular waves to calculate a thermal pulse impedance $Z_{th(p)}$ using the formula $Z_{th(p)} = Z_{th(t)} + Z_{th(z)}$.

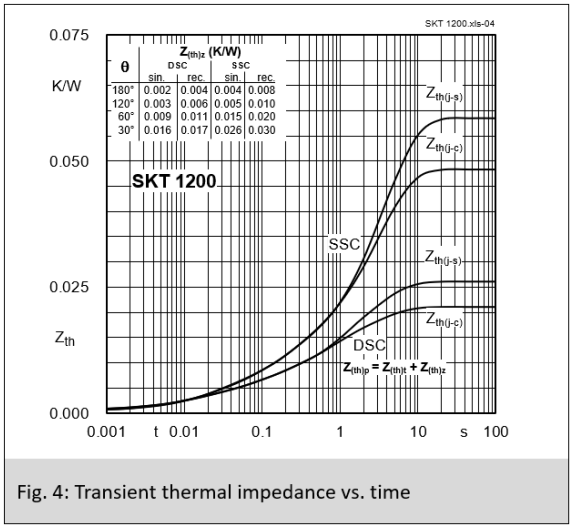


Fig. 4: Transient thermal impedance vs. time

Figure 7.2.33 Transient thermal impedances versus time of a disc type thyristor SKT1200/18E

In order to calculate the total thermal impedance $Z_{th(j-a)}$, the transient thermal impedance $Z_{th(s-a)}$ of the heatsink must be added to $Z_{th(j-s)}$. Datasheets of heatsinks often contain a diagram illustrating the given thermal impedance $Z_{th(s-a)}$ or $Z_{th(c-a)}$ as a function of the time t.

Mean power loss [P_{TAV}] as a function of the mean on-state current [I_{TAV}]

By analogy with figure 1L of thyristor/diode datasheets, but for the overload case, Figure 7.2.34 shows the typical power dissipation P_{TAV} as a function of the mean on-state current I_{TAV} for DC (cont.), sinusoidal half waves (sin. 180) and square-wave pulses (rec. 60...180).

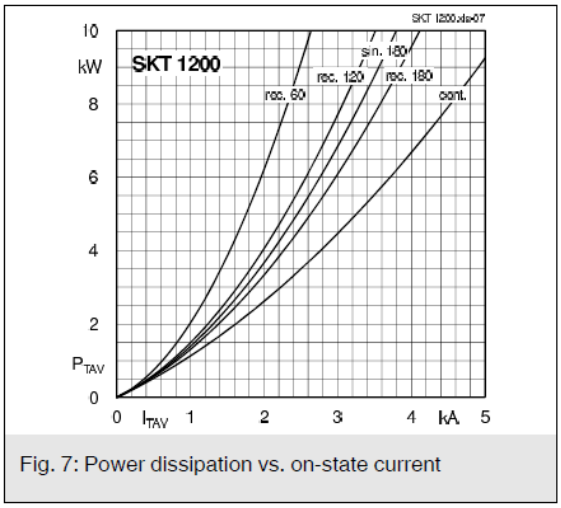


Fig. 7: Power dissipation vs. on-state current

Figure 7.2.34 Power dissipation versus on-state current angle of a disc type thyristor SKT1200

7.2.8 Fast diodes – additional datasheet specifications

7.2.8.1 Current platforms with fast diodes

Semikron Danfoss product range includes three module families of fast switching diodes:

- Fast (medium-speed) switching diode chips made of gold-doped silicon, packed in SEMIPACK housings and as discrete screw fit diodes,
- Fast speed switching, soft recovery silicon diode chips in CAL technology, packed in SEMIPACK or SEMITRANS housings
- Ultra-fast speed switching diode chips made of silicon carbide, packed in SEMIPACK or SEMITOP housings.

The data sheets of the fast (switching) diode modules and discrete diodes have some differences to the data sheets of the modules with mains diodes and the discrete diodes for mains applications.

7.2.8.2 Additional characteristics

For fast Silicon diodes and diode modules, the table "Characteristics" contains additional information on their dynamic behaviour (Figure 7.2.35).

Characteristics						
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Unit**
Diode						
Q_{rr}	I_F = 600 A di/dt_{off} = 4000 A/µs V_R = 600 V	T_j = 150 °C		80		µC
I_{RRM}		T_j = 150 °C		280		A
t_{rr}		T_j = 150 °C		0.78		µs
E_{rr}		T_j = 150 °C		21		mJ

Figure 7.2.35 Additional dynamic values in the datasheet for a 1200V/170A fast silicon diode module SKKE600F12 [7.24]

The information contains typical values of reverse recovery charge Q_{rr}, peak reverse recovery current I_{RM}, reverse recovery time t_{rr} and the energy E_{rr} during reverse recovery. The values listed refer to identical parameters:

- Chip temperature $T_j = T_{jmax}$
- Defined Forward current I_F before switch-off: For Si diode modules according to the max permissible mean current I_{FAV} (sin 180°, T_c = 85°C).
- Defined falling rate of forward current $-di_F/dt$
- Defined reverse voltage V_R (for Si diode modules according the typical DC working voltage).

Explanations on definitions of dynamic values are given in the chapter 2.3.4 above.

For silicon carbide diode modules, the corresponding datasheet table is modified, as there is no storage charge here (Figure 7.2.36).

Characteristics					
Symbol	**Conditions**	**min.**	**typ.**	**max.**	**Unit**
Diode					
C_j	f = 1 MHz, V_R = 800 V, T_j = 25 °C		0.340		nF
Q_c	V_R = 800 V, di/dt = 500 A/µs, T_j = 25 °C		0.26		µC

Figure 7.2.36 Additional dynamic values in the datasheet for a 1200V/60A silicon carbide diode module SKKE60S12 [7.25]

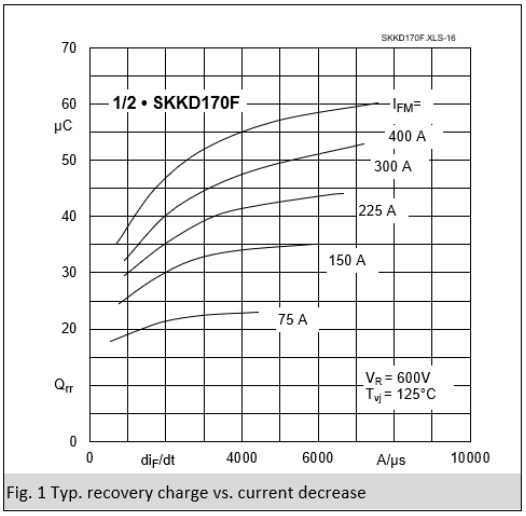
Here, the information contains typical values of junction capacitance C_j and capacitive charge Q_c at T_j = 25°C and a defined reverse voltage V_R. C_j is a small signal value at a measuring frequency of 1MHz.
The datasheet value of the capacitive charge Q_c:

$$Q_c = \int_0^{V_R} C_j\,(v)\mathrm{d}v$$

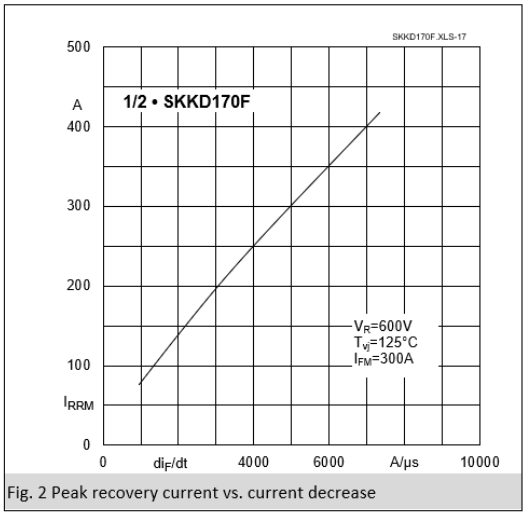
was measured at defined forward current falling steepness $-di_F/dt$.

7.2.8.3 Diagrams for fast silicon diodes

When turning off a diode, most of the charge carriers transported with the forward current into the middle layer of the PIN junction must be depleted in order to be able to pick up a voltage in the reverse direction when the anode/cathode voltage is reversed.
Residual positive charge carriers (holes) still present in the I-layer cause the anode current to not stop at the zero crossing but to continue to flow for the reverse recovery time t_{rr} in the reverse direction as a reverse recovery current with the peak value I_{RRM}, cf. chapters 2.1.3 and 2.3.4. In the most datasheets of fast silicon diodes or diode modules are two diagrams added to the figures in the data sheets for mains diodes and diode modules (Figure 7.2.37).



a)



b)

Figure 7.2.37 Dynamical characteristics of a 1200V/170A fast silicon diode halfbridge module SKKD170F12 [7.26] a) Typ. recovered charge vs. current decrease; b) Peak recovery current vs. current decrease

The characteristic diagrams show the dependences of recovered charge Q_{rr} and peak recovery current I_{RM} on the forward current falling rate $-di_F/dt$ as well as the peak forward current I_{FM} before commutation (typical values at $T_j = T_{jmax}$).
The diagram "Transient thermal impedance vs. time" essentially corresponds to figure 14 (4) in the data sheets of the mains diode modules or discrete diodes. In some data sheets, however, several curves are given for different duty cycles (Figure 7.2.38).

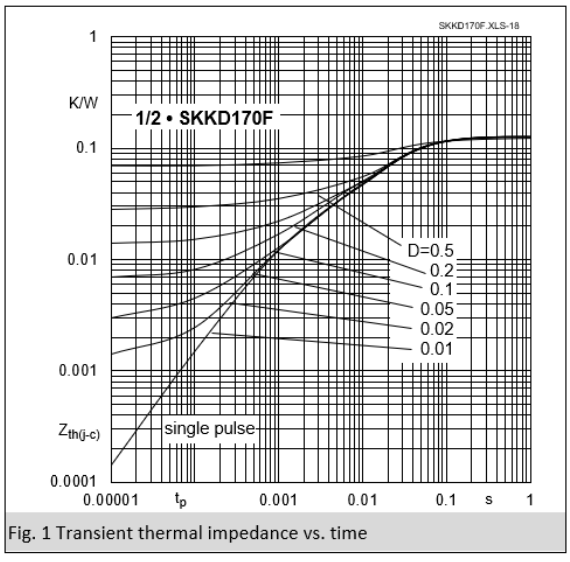


Figure 7.2.38 Diagram for transient thermal impedance $Z_{th(j-c)}$ vs. time at various duty cycles for the fast silicon diode halfbridge module SKKD170F12

The transient thermal impedance $Z_{th(j-c)}$ is given for single pulses and square wave current as a function of the time t elapsed after a step change in power dissipation. In the short-time range, the duty cycle has a clear influence on $Z_{(thj-c)}$: As the duty cycle increases, the initial value of $Z_{th(j-c)}$ rises from over the value for single pulses. Regardless of the current form, however, the final value $R_{th(j-c)}$ is reached at about the same time.

7.2.8.4 Diagrams for SiC diode modules

The data sheets for Semikron Danfoss SiC diode modules have not the complexity of data sheets for older products. The historical ballast has been removed. The diagrams showing the main feature of the Schottky diodes:

The datasheet figure 1 "Transient thermal impedance vs. time" essentially corresponds to figure 3 in the data sheets of the fast silicon diode modules.
The datasheet figure 2 “Typ. Forward characteristics” corresponds to figure 4 in the data sheets of the fast silicon diode modules.
The added Figure 7.2.39 “Typ. Capacitance-voltage characteristics” (small signal values at 1MHz measuring frequency) illustrates the dependence of the capacitance on the anode-cathode voltage at the diode is shown here. The capacitance has its maximum at 0V and decreases as the reverse voltage increases.

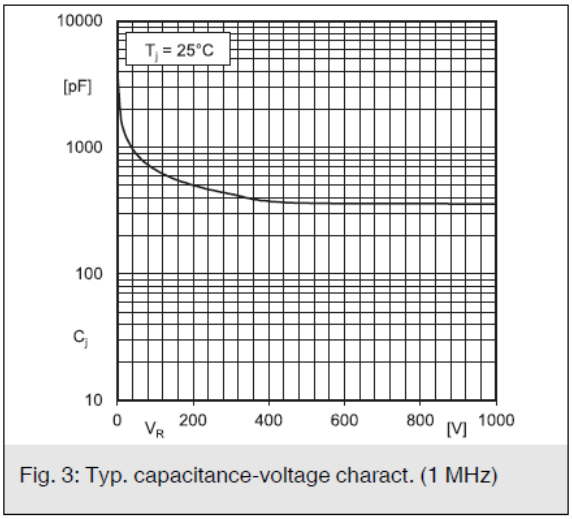


Figure 7.2.39 Small signal capacitance vs. voltage characteristics of a 1200V/60A silicon carbide diode module SKKE60S12

7.3 Datasheet specifications for IGBT modules

7.3.1 Preface

Semikron Danfoss offers IGBT modules in various topologies within the product lines SEMITOP®, MiniSKiiP®, SEMiX®, SEMITRANS® and SKiM®, as well as the intelligent power modules SKiiP®. The IGBT modules are available from 4A up to 3600A, with voltage classes from 600V up to 1700V, featuring also key technologies such as sintering and spring or Press-fit contacts for quick and easy assembly.
Available topologies include halfbridge, H-bridge, sixpack, CB, CI and CIB (converter inverter brake), 3-level and many more topologies, covering every application field. In these topologies, the latest IGBT chips usually are combined with freewheeling diodes in CAL diode technology.

As an introduction, Table 7.3.1 provides an overview of the IGBT and SiC MOSFET chips used in the Semikron-Danfoss power modules.

Voltage class	Shortcut	IGBT / SiC MOSFET Chip series designation	SEMITOP	MiniSKiiP	SEMiX	SEMITRANS	SKiM 4/5	SKiM 63/93	SKiiP
IGBT									
600/650V	066	Infineon IGBT3 Standard type 600V	✓	✓	✓	✓			
	07E3	Infineon IGBT3 Standard 650V (E-Type)	✓	✓	✓	✓	✓		
	07F3	Infineon IGBT3 High Speed Q-Type 650V (Q-Type)	✓		✓		✓		
	07E4	Infineon IGBT3 Medium Power 650V (M-Type)		✓	✓				
	07S5	Infineon Trenchstop5 650V Medium Speed (S-Type)	✓						
	07L5	Infineon Trenchstop5 650V Low V_{CEsat} (V-Type)	✓			✓			
	125	Infineon IGBT2 Ultra Fast	✓			✓			
	126	Infineon IGBT3 Standard Type	✓	✓	✓	✓	✓		✓
	12T4	Infineon IGBT4 Low Power (L-Type)	✓	✓	✓	✓	✓		
	12E4	Infineon IGBT4 Medium Power (M-Type)	✓	✓	✓	✓	✓	✓	✓
	12P4	Infineon IGBT4 High Power (H-Type)				✓			
	12F4	Infineon IGBT4 High Speed (Q-Type)	✓	✓		✓			
	12RA	Rohm RGA IGBT	✓	✓					
	12T7	Infineon IGBT7 Low Power (L-Type)	✓	✓					
	12M7	Mitsubishi Gen. 7 IGBT	✓	✓	✓	✓			✓
	12V	Fuji V-IGBT			✓	✓			
1700V	176	Infineon IGBT3 Standard Type		✓	✓	✓	✓		✓
	17E4	Infineon IGBT3 (shrink) Medium Power (M-Type)	✓	✓	✓	✓		✓	✓
	17P4	Infineon IGBT3 (shrink) High Power (H-Type)				✓			
	17T7	Infineon IGBT7 Low Power (L-Type)							✓
SiC MOSFET									
650/1200/2000V	65CR03	Cree (Wolfspeed) 650V SiC MOSFET Gen. 3	✓						
	12RM2	Rohm SIC MOSFET Gen. 2				✓			
	12RM4	Rohm SIC MOSFET Gen. 4	✓						
	12CR03	CREE (Wolfspeed) SiC MOSFET Gen. 3	✓						
	20RM4	Rohm SIC MOSFET Gen. 4	✓			✓			✓
	20IE1	Infineon CoolSiC™							✓

Table 7.3.1 IGBT and SiC MOSFET chip assemblies per product line of Semikron Danfoss power transistor modules. (A red tick means that some types are also available with SiC Schottky Barrier freewheeling diodes.)

The explanations in chapter 7.3 mainly refer to transistor modules with IGBTs and freewheeling diodes in CAL technology. Chapter 7.4 contains explanations of the datasheets for the Semikron Danfoss' Power IPM SKiiP series. Explanations on SiC MOSFET module designations and housing images are contained in chapter 7.5.

Due to the developments over the past few decades, Semikron Danfoss datasheets also have differences with regard to datasheet layout, data content and specifications for the different generations of IGBT modules and different module platforms. Since this data is to be standardised as part our product maintenance measures, the following information essentially refers to the latest datasheets issued in from 2020 onwards, and i.e., the latest 7th chip generation is referred to in the context of IGBT modules.
The datasheet content is explained by the example of widely used IGBT halfbridge modules with screw power terminals and Press-fit control terminals from the SEMiX3p product family. Where applicable, different datasheet structures for the datasheets of older modules which are still being produced will be pointed out expressly.

7.3.1.1 Major IGBT module topologies

Table 7.3.2 shows the most common topologies of IGBT modules for the primary use in 2-level converters and the product lines into which these are currently being integrated.

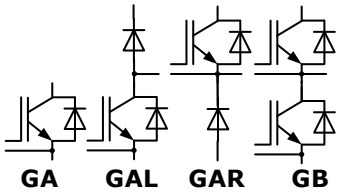
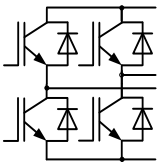
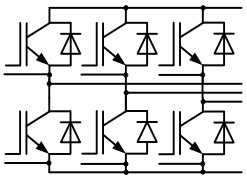
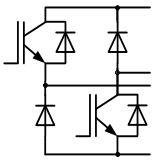
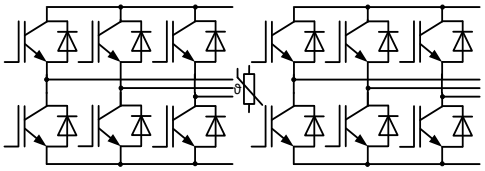
Single switch, Buck/Boost Chopper and halfbridge IGBT modules	H-Bridge IGBT modules	Sixpack and Twelvepack IGBT modules
		
GA: Single switch SEMITRANS **GAL/GAR: Buck/Boost Chopper** SEMITRANS SEMITOP MiniSKiiP SEMiX SKiM **GB: Halfbridge** SEMITRANS SEMITOP MiniSKiiP SEMiX SKiiP	**GH: Symmetrical H-Bridge** SEMITOP MiniSKiiP SEMiX SKiM	**GD or AC: Sixpack (3-Phase Bridge)** SEMITOP (GD) MiniSKiP (AC) SEMiX (GD) SKiM (GD) SKiiP (GD)
		
	GAH: Asymmetrical H-Bridge SEMITOP	**ACC: Twelvepack** MiniSKiiP

Table 7.3.2 Most common topologies of IGBT modules for major applications

Due to their connection flexibility, SEMITOP and MiniSKiiP modules allow the integration of a large number of other topologies. Please refer www.semikron-danfoss.com for more detailed information on the broad possible spectrum.

7.3.1.2 3-level power modules

The Semikron Danfoss 3-level power modules use a wide variety of IGBT or SiC MOSFET chips and various diode chips in different topologies.
3-level circuit with IGBT are available in SEMITOP®, MiniSKiiP®, SEMiX® 5, SKiM® 4 or SEMITRANS® 10 housings, see Table 7.3.3.

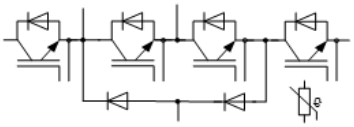
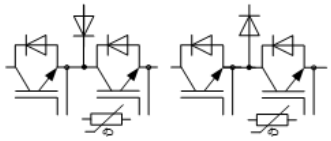
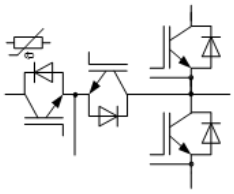
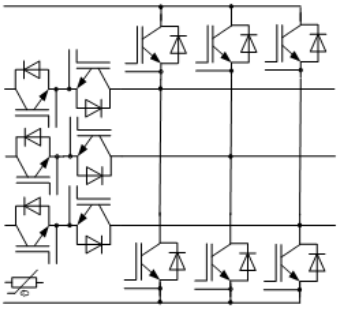
Topology	SEMITOP	MiniSKiiP	SEMiX 5	SKiM 4	SEMITRANS 10	Circuit
NPC	✔	✔	✔	✔	✔	
Split-NPC		✔			✔	
T-NPC	✔	✔	✔	✔	✔	
3-phase TNPC	✔					

Table 7.3.3 3-level IGBT modules

3-level modules in hybrid SiC and full SiC technology are available exclusively in SEMITOP housings, see Table 7.3.4.

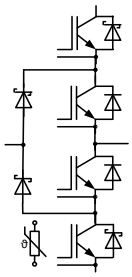
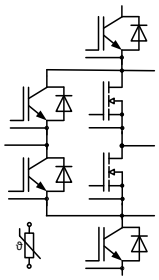
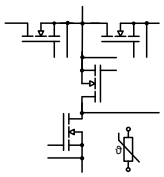
	Hybrid-SiC NPC	Hybrid-SiC ANPC	Full SiC T-NPC
Circuit			

Table 7.3.4 3-level hybrid SiC and full SiC modules

7.3.1.3 CI, CB and CIB power modules

CI (Converter Inverter), CB (Converter Brake) and CIB (Converter Inverter Brake) structures are high-integration-level, user-friendly topologies that can be found in the MiniSKiiP®, SEMITOP® and SEMIPONT® 6 product lines. Such modules feature a single-phase or three-phase diode, half- or full-controlled bridge rectifier (C), a three-phase inverter (I) and - in the CB and CIB topologies - an IGBT with freewheeling diode which serves as a brake chopper (B). The Table 7.3.5 shows examples of these topologies.

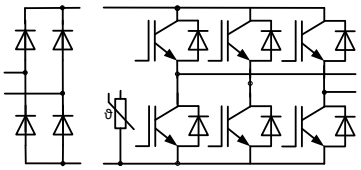
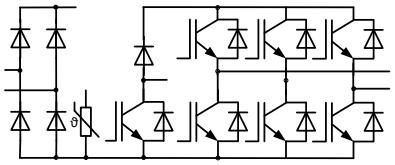
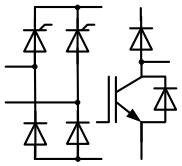
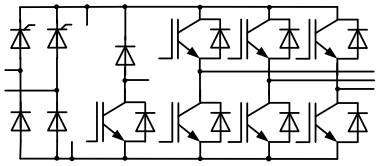
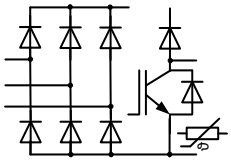
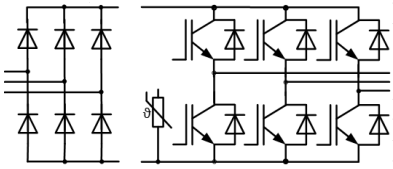
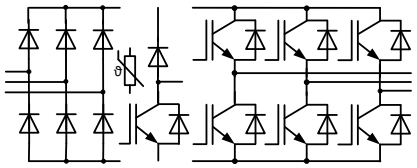
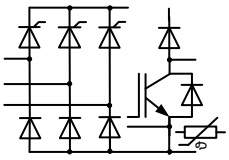
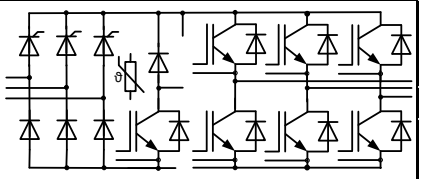
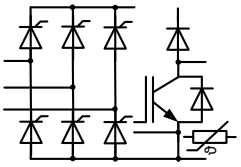
Converter **B**rake **IGBT modules**	Converter **I**nverter **IGBT modules**	**C**onverter **I**nverter **B**rake **IGBT modules**
	 **Single-phase diode rectifier bridge + IGBT inverter** MiniSKiiP (NEC) SEMITOP (BGD)	 **Single-phase diode rectifier bridge +brake IGBT + IGBT inverter** MiniSKiiP (NEB)
 **Single-phase half - controlled rectifier bridge + brake IGBT** SEMITOP (BHL)		 **HEB: Single-phase half-controlled rectifier bridge + brake IGBT + IGBT inverter** MiniSKiiP (HEB)
 **3-phase diode rectifier bridge + brake IGBT** MiniSKiiP (ANB) SEMITOP (DGL) SEMIPONT (L)	 **3-phase diode rectifier bridge + IGBT inverter** MiniSKiiP (NAC) SEMITOP (DGD)	 **3-phase diode rectifier bridge + brake IGBT + IGBT inverter** MiniSKiiP (NAB) SEMITOP (DGDL)
 **3-phase half-controlled rectifier bridge + brake IGBT** MiniSKiiP (AHB) SEMIPONT (DH)		 **3-phase half-controlled rectifier bridge + brake IGBT + IGBT inverter** MiniSKiiP (HAB)
 **3-phase full-controlled rectifier bridge + brake IGBT** MiniSKiiP (ATB)		

Table 7.3.5 Examples of power modules including CB, CI, or CIB topologies

Within each topology, the modules differ with respect to the circuit layout and the integration of temperature sensors. The datasheet ratings for inverter and brake chopper IGBT and diodes, the temperature sensor and the properties of CI, CIB and CB power modules correspond to those for IGBT modules provided in the chapter 7.3.2 to 7.3.4 below.
The same freewheeling diodes are used for inverters and brake choppers, whereas the chopper IGBT may have a smaller rating than the inverter IGBT. In such cases, the datasheet of another module type may be referred to in the relevant datasheet.
The properties of rectifier diodes or thyristors are also given in the datasheet tables and diagrams. Explanations on the respective maximum ratings, characteristics and diagrams are included in the chapter 7.2 for the line rectifier diodes or thyristors.

7.3.1.4 Type designation codes and housing images

The following information on the type designation codes and the housing images of the Semikron Danfoss product lines also apply to 3-level IGBT modules and power modules with SiC MOSFET.

SEMITOP®

The SEMITOP product line that extend furthest into the low-power range consist exclusively of 12-mm-high modules for PCB mounting, covering the low and medium power range, with one or two mounting screws and no baseplate. The PCB interface can be made via solder or Press-fit pins. The low commutation inductance design and the choice of the latest Si and SiC chip technologies make this product suitable for UPS, solar, energy storage, motor drives, power supplies, welding and EV charger markets. A large variety of configurations are possible within the SEMITOP product line, including 3-level (NPC/TNPC) and CIB (converter-inverter-brake) topologies.
Figure 7.3.1 provides an overview of the six SEMITOP housing images used for IGBT and SiC MOSFET power modules. The SEMITOP 1...4 sizes listed in the top row belong to the "SEMITOP classic" series, while the SEMITOP E types in the bottom row are mechanically compatible with many competitor products.

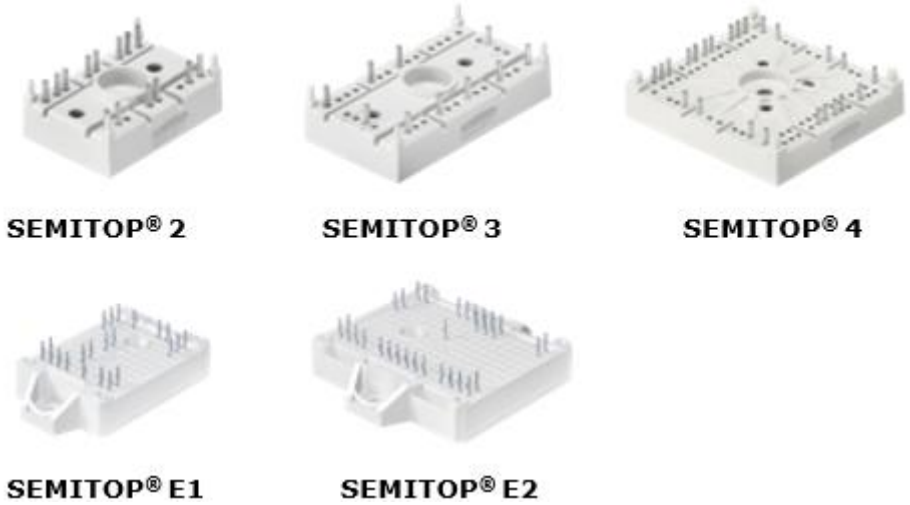


Figure 7.3.1 SEMITOP housings used for IGBT and SiC MOSFET power modules

The type designation code for SEMITOP IGBT modules is shown in Figure 7.3.2.

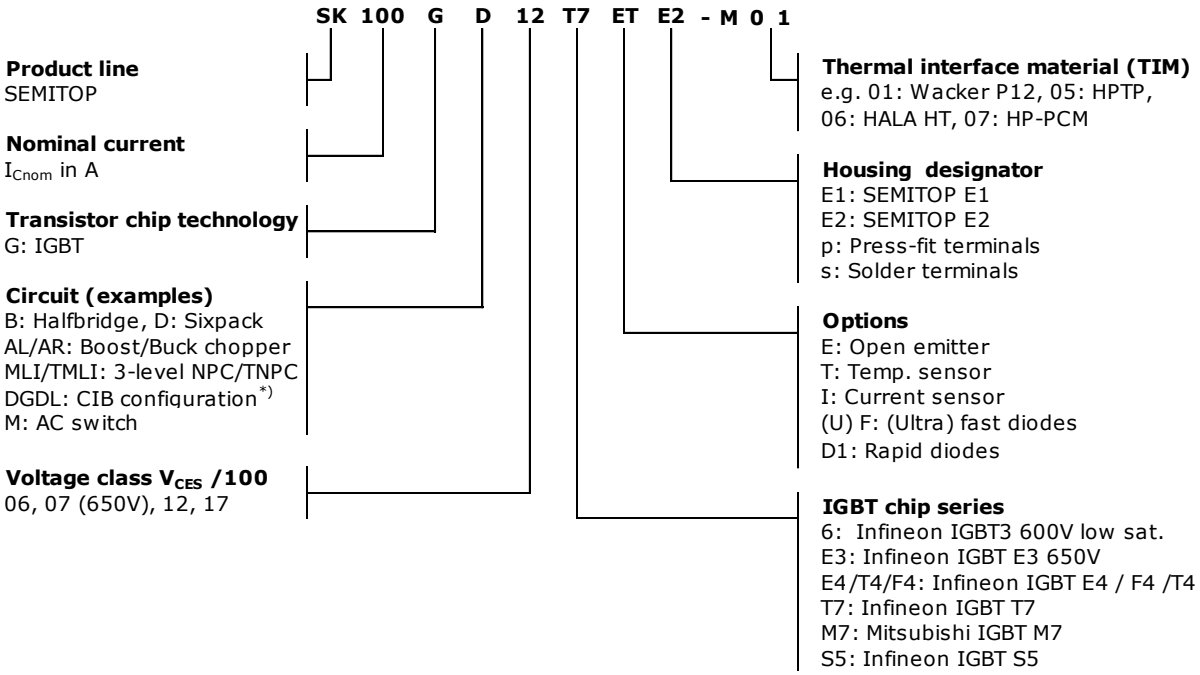


Figure 7.3.2 SEMITOP IGBT module type designation code; *) see chapter 7.3.1.3 for additional statements about CIB modules)

MiniSKiiP®

The unique mechanical design of these power modules offers outstandingly easy assembly and service friendly spring contact technology. Opposed to conventional solder or Press-fit modules with specific equipment required (automated presses, wave-soldering machine), no dedicated tools are needed for MiniSKiiP assembly. Instead, one or two screws connect everything from driver to heatsink.
Assemble the printed circuit board (PCB), power module and heatsink in one mounting step. For higher flexibility, the PCB does not need holes for solder pins or Press-fit connections. The springs connecting the PCB and power circuitry are far superior to soldered joints, increasing lifetime under thermal or mechanical stress. Thanks to the high mechanical pressure provided by the springs, achieve an airtight, reliable electrical connection.
Figure 7.3.3 provides an overview of the MiniSKiiP housing images. The mechanical dimensions of the "MiniSKiiP Dual" types with halfbridge or chopper topologies correspond to those of the other types with the same numbers.

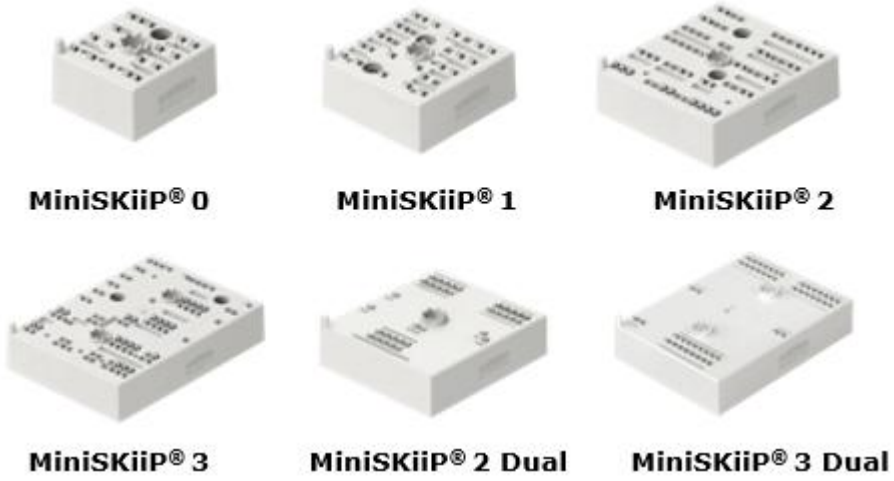


Figure 7.3.3 MiniSKiiP housings

The type designation code for MiniSKiiP IGBT modules is shown in Figure 7.3.4.

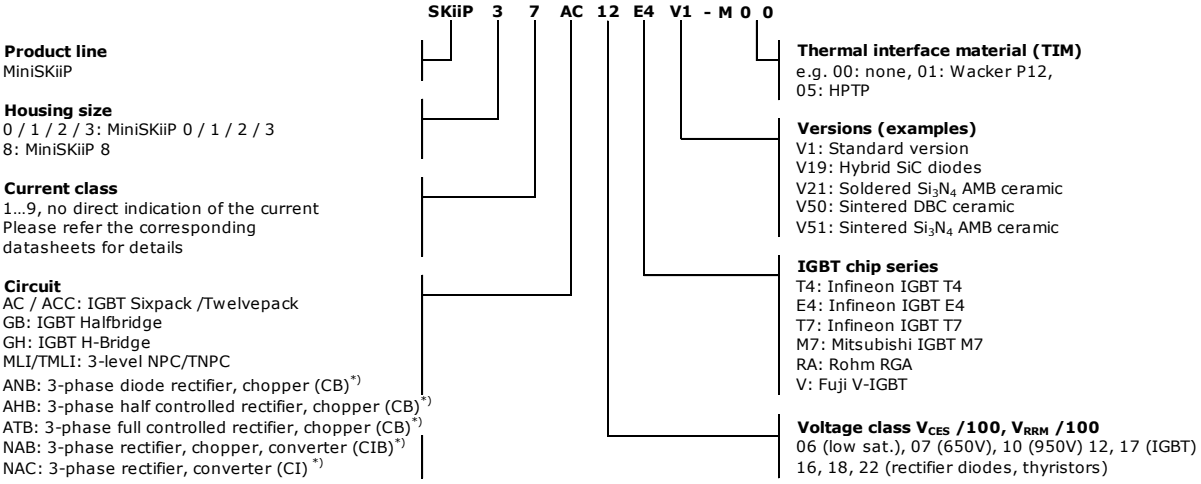


Figure 7.3.4 MiniSKiiP IGBT module type designation code; *) see chapter 7.3.1.3 for additional statements about CIB modules)

SEMiX®

The SEMiX product line comprises three module platforms with a standardised module height of 17mm, allowing a flat and compact inverter design. Some SEMiX modules are also available in diode and thyristor configurations, e.g. in the form of bridge rectifiers, see chapter 7.2.
The SEMiX spring platform covers SEMiX 1s to SEMiX 4s and SEMiX 13 packages with spring contacts for auxiliary connections and power terminals with screw connectors.
The SEMiX 1c, SEMiX 2c, and SEMiX 33c modules are provided with solder terminals for auxiliary connections and power terminals with screw connectors. The control connections of SEMiX 33c modules are adapted from a spring contact to solder terminals with a PCB on top of the module.
The PCB-mountable SEMiX 6c modules have solder terminals for both power and auxiliary connections.
The SEMiX Press-fit platform combine the proven SEMiX designs with the fast and easy assembly using Press-fit technology for mounting a gate driver directly on top of the module.
SEMiX 3p and SEMiX 5p modules use Press-fit terminals for auxiliary connections and screw connectors for power terminals, SEMiX 6p modules have Press-fit terminals for both power and auxiliary connections.
Selected SEMiX 3p IGBT modules are also available with integrated shunt resistors for AC current measurement or SiC freewheeling diodes. The SEMiX 5p IGBT modules belong to a compact, baseplate power module platform with optimized AC and DC screw connections. The platform also includes IGBT modules with NPC and T-NPC 3-level topologies. Figure 7.3.5 shows the various SEMiX housing images. The type designation code for SEMiX IGBT modules is shown in Figure 7.3.6.



Figure 7.3.5 SEMiX housings

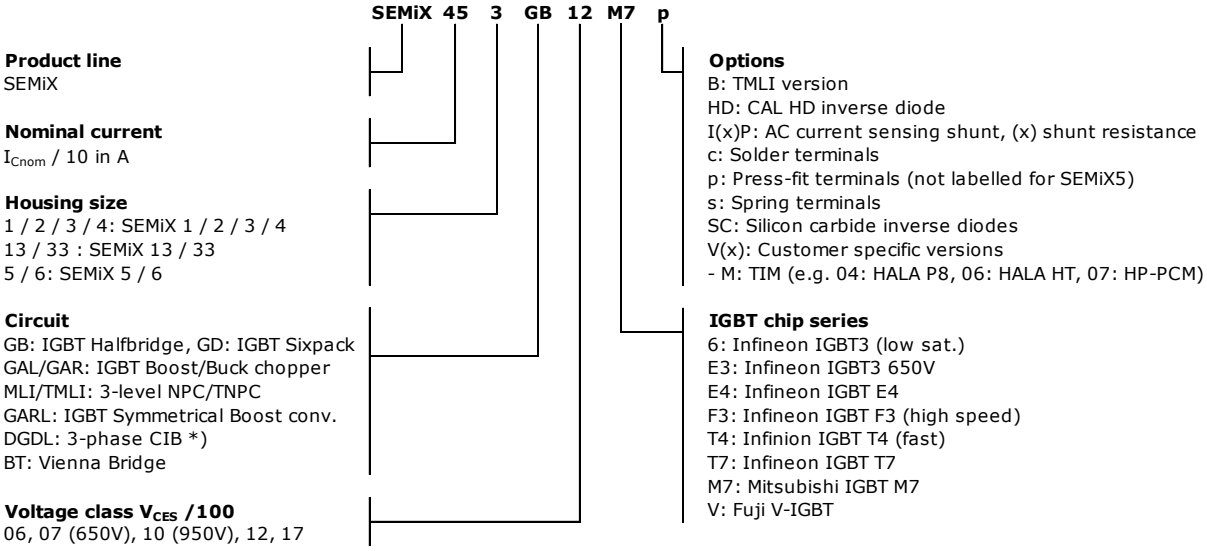


Figure 7.3.6 SEMiX IGBT module type designation code; *) see chapter 7.3.1.3 for additional statements about CIB modules)

SEMITRANS®

The SEMITRANS product line covers the platforms SEMITRANS Classic (SEMITRANS 2 to 5), SEMITRANS 10 and SEMITRANS 20 whose housing images are shown in Figure 7.3.7.



Figure 7.3.7 SEMITRANS housings

The SEMITRANS Classic platform feature well-proven designs that come from over 30 years of market experience. It covers the SEMITRANS 2 to SEMITRANS 5 packages with screw terminals for power terminals and plug, solder or screw contacts for auxiliary connections.
These packages are still suitable for the latest chips generations, including Silicon Carbide, thanks to its low-inductance design.
The platform SEMITRANS 10 takes the power range into the realm of megawatt applications, not only with halfbridges, but also in complete and split 3-level halfbridge topologies for wind and solar applications. It covers the SEMITRANS 10 P2, SEMITRANS 10 and SEMITRANS 10+ packages with screw terminals for power and auxiliary connections.
The SEMITRANS 20 power modules serve high power applications with a low inductance and easy-to-parallel power module design. With its available advanced technologies (options see Figure 7.3.8) such as sintered chips and AlCu bond wires, it boasts up to 5 times more lifetime than standard modules. All packages use screw terminals for power and auxiliary connections. The type designation code for SEMITRANS IGBT modules is shown in Figure 7.3.8.

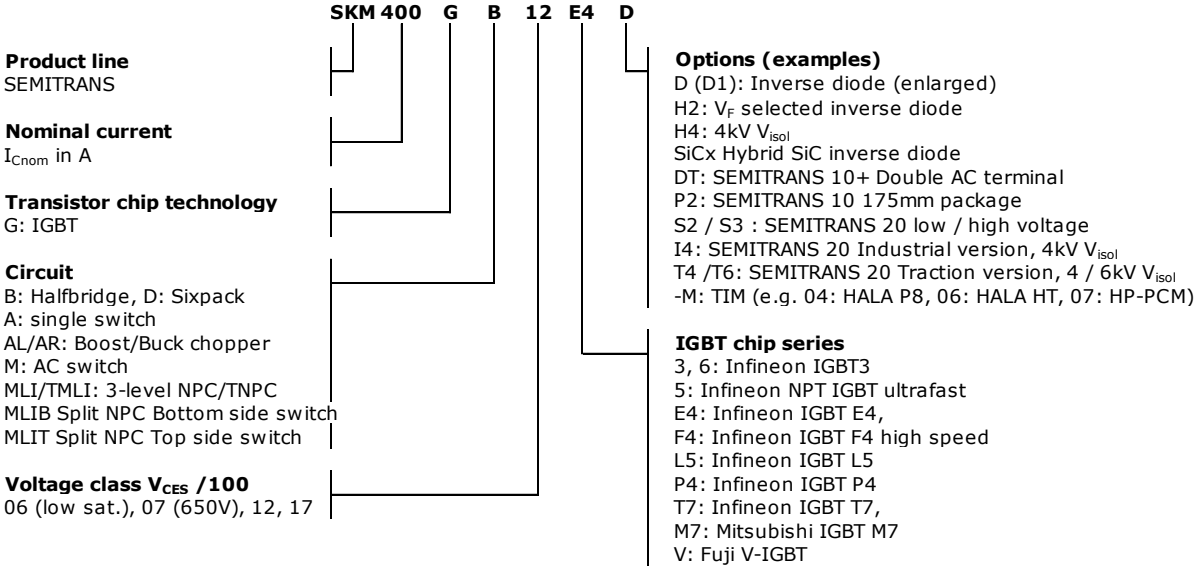


Figure 7.3.8 SEMITRANS IGBT module type designation code

SKiM®

The SKiM IGBT module product line covers the platforms SKiM 4/5 and SKiM 93, whose housing images are shown in Figure 7.3.9.



Figure 7.3.9 SKiM housings

All SKiM power modules are designed as a high-reliability modules without baseplate and with screw terminals for power terminals and spring contacts for auxiliary connections. SKiM modules meet the high demands of shock and vibration stability, as well as high temperature capability and service life. Modules of the SKiM 4/5 platform offer a wide variety of sixpack and 3-level topologies. Due to sintered chips, pressure chip-to-terminal contacts and spring technology the SKiM 93 sixpack modules are completely solder-free modules. Optional features are AlCu-bonded diodes and high-performance thermal grease. The type designation code for SKiM 4/5 IGBT modules is shown in Figure 7.3.10 a), for SKiM 93 in Figure 7.3.10 b).

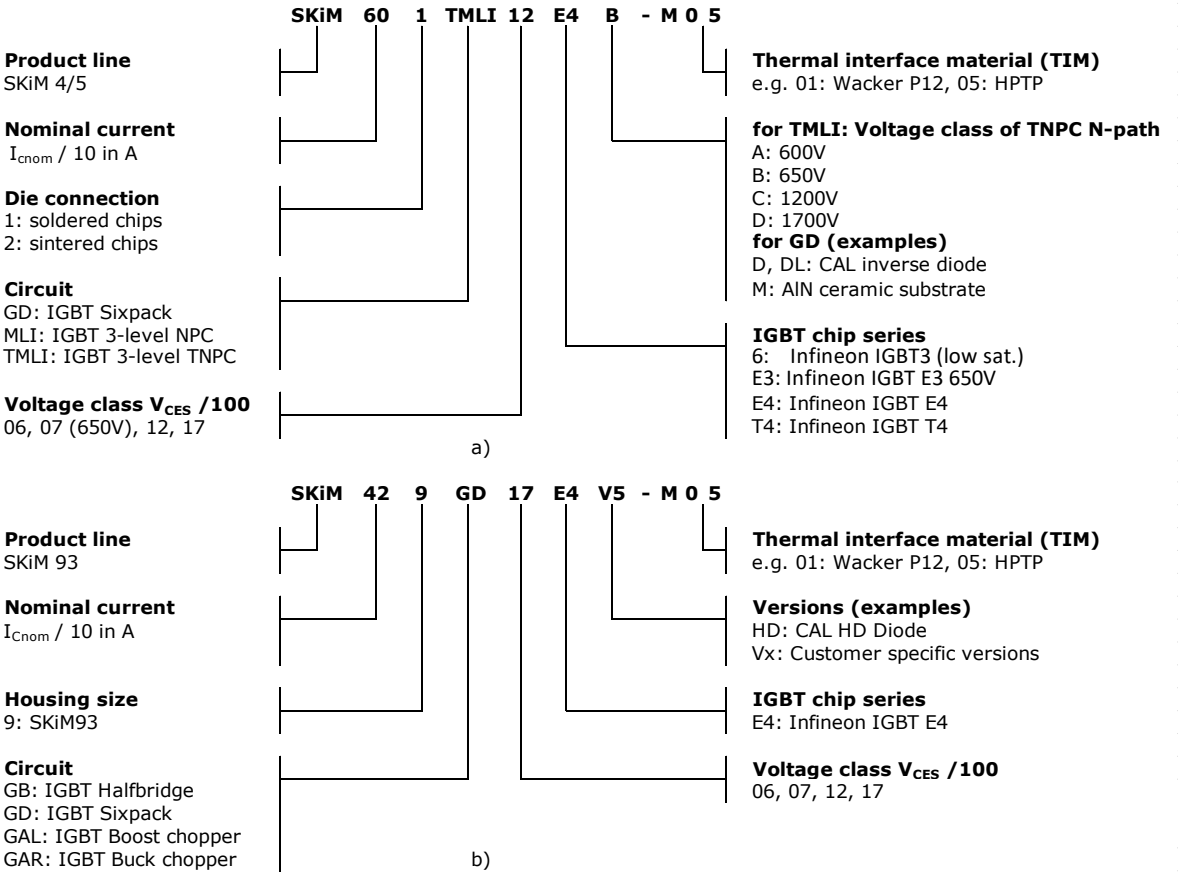


Figure 7.3.10 SKiM IGBT module type designation codes: a) SKiM 4/5; b) SKiM 93

7.3.2 Absolute maximum ratings

In the datasheets, the maximum ratings are specified separately for each individual component of an IGBT module (IGBT, diode, case, temperature sensor, if available). All ratings for IGBT and diodes refer to one switch (arm), irrespective of the number of IGBT or diode chips actually connected in parallel per switch (arm).

Absolute Maximum Ratings				
Symbol	**Conditions**		**Values**	**Unit**
IGBT				
V_{CES}	T_j = 25 °C		1200	V
I_C	T_j = 175 °C	T_c = 25 °C	601	A
		T_c = 80 °C	457	A
I_{Cnom}			450	A
I_{CRM}			900	A
V_{GES}			-20 ... 20	V
t_{psc}	V_{CC} = 800 V $V_{GE} \leq$ 15 V $V_{CES} \leq$ 1200 V	T_j = 150 °C	8	µs
T_j			-40 ... 175	°C
Inverse diode				
V_{RRM}	T_j = 25 °C		1200	V
I_F	T_j = 175 °C	T_c = 25 °C	554	A
		T_c = 80 °C	415	A
I_{FRM}			900	A
I_{FSM}	t_p = 10 ms, sin 180°, T_j = 25 °C		2430	A
T_j			-40 ... 175	°C
Module				
$I_{t(RMS)}$			600	A
T_{stg}	module without TIM		-40 ... 125	°C
V_{isol}	AC sinus 50Hz, t = 1 min		4000	V

Figure 7.3.11 Maximum ratings of IGBT module SEMiX453GB12M7p [7.27]

7.3.2.1 IGBT maximum ratings

Collector-emitter voltage V_{CES}

Maximum permissible voltage between the collector and emitter terminals of the IGBT chips with gate-emitter short circuited at junction temperature T_j = 25°C. The temperature coefficient is about $\frac{V_{CES}}{1000} \cdot \frac{1}{K}$, means for a 1200V IGBT 1.2V/K as a rule of thumb. The maximum collector-emitter voltage increases in proportion to the temperature owing to the temperature dependency of the breakdown voltage. Irrespective of the load conditions, the sum of the collector-emitter supply voltage V_{CC} and the switching overvoltage $\Delta V_{CE} = L_\sigma \cdot di_C/dt$ must not exceed voltage V_{CES} (L_σ: sum of the parasitic inductances in the commutation circuit).

Continuous collector current I_C

Maximum permissible continuous direct current over the collector output at which the permissible maximum junction temperature is reached; parameters: for two different case temperatures for IGBT modules with baseplate or two different heatsink temperature or baseplate-less modules; junction temperature $T_j = T_{jmax}$.
The maximum permissible I_C for IGBT modules is determined with

$$I_C = \frac{P_{totmax}}{V_{CE(sat)}} = \frac{(T_{jmax} - T_c)}{V_{CE(sat)} \cdot R_{th(j-c)}} \quad \text{for baseplate modules}$$

$$I_C = \frac{P_{totmax}}{V_{CE(sat)}} = \frac{(T_{jmax} - T_s)}{V_{CE(sat)} \cdot R_{th(j-s)}} \quad \text{for baseplate-less modules}$$

T_{jmax} and P_{totmax} are the maximum permissible values of junction temperature and power dissipation. Since I_C designates a static maximum value, it is not relevant to switching operation.

Nominal collector current I_{Cnom}

Rated current of IGBT chips indicated in the chip manufacturer's datasheet multiplied by the number of IGBT chips per switch connected in parallel in the module.
For current IGBT modules, I_{Cnom} is the naming current, i.e., the current encoded in the module's type designation (e.g. SEMiX453GB12M7p: I_{Cnom} = 450A).

Repetitive peak collector current I_{CRM}

The permissible repetitive peak forward current depends on the feasible power dissipation and the thermal impedance Z_{th}, but also takes into account damaging of chip metallisation and premature chip ageing or bonding wire failure mechanisms and limiting the IGBT-chip forward and reverse bias safe operating areas.
Therefore, the datasheet value is lower than a theoretically calculated value of Z_{th} and the chip output characteristics. Thus, up to current I_{CRM}, safe switching operation is possible, taking into account all practical limitations of the power module. The specified value must not be exceeded although the maximum permissible junction temperature is not reached.
In most of the datasheets I_{CRM} is indicated as $2 \cdot I_{Cnom}$; For some IGBT modules using IGBT4 chips, I_{CRM} is specified as $3 \cdot I_{Cnom}$ in accordance with the specifications by the chip manufacturer. With the nominal gate resistance and high DC link voltage, it is not always possible to turn these currents off without exceeding V_{CES} Therefore, Semikron Danfoss recommends for turning off currents above $2 \cdot I_{Cnom}$ countermeasures like DC link voltage reduction, active clamping, very slow turn-off or turn-off snubber circuits. Such action is likely to increase power losses which must be taken into account.

Gate-emitter voltage V_{GES}

Maximum permissible voltage between the gate and emitter terminals of the IGBT module at case temperature T_c = 25°C with both polarities.

Turn-on time during non-repetitive short circuit t_{psc}

The amount of energy that the IGBT chips of a switch can absorb in the event of a short circuit, depending on volume and structure of the chips, is decisive for the ability to actively switch off a short circuit current. However, the short circuit characteristics in a real application depend significantly on application specific parameters like operation voltage, temperature, stray inductances, gate driving conditions and the impedance of the short circuit path. The level of the short circuit current determined by the gate-emitter voltage $V_{GE(on)}$ and the IGBT chip technology. The datasheet value of maximum time t_{psc} is based on the IGBT arm short circuit as shown in the test circuit according Figure 7.3.12 a). Here both IGBT are switched-on simultaneously. In that case it has to be guaranteed that the DUT limits the current and take over the full V_{CC} e.g. by a higher Gate voltage of the BOT switch in the example. The same effect is reached if the BOT IGBT is short circuited by a short piece of cable and the TOP IGBT is driven with single pulses. This kind of short circuit is called SC1.

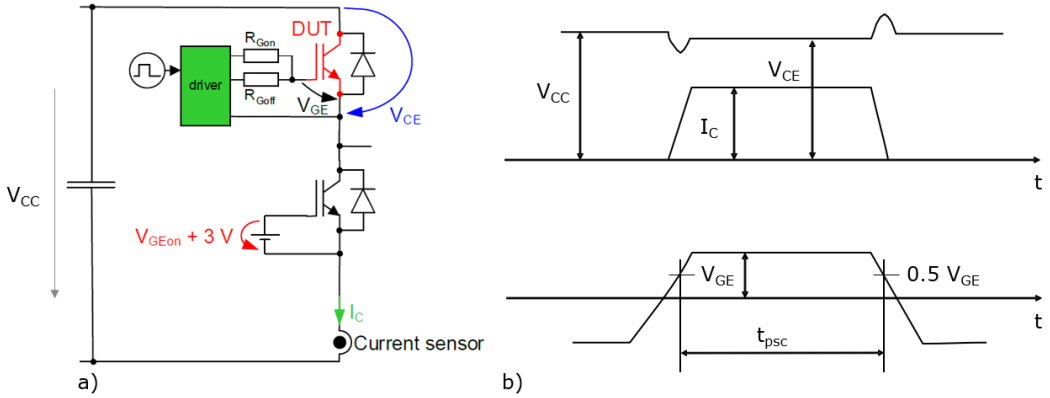


Figure 7.3.12 a) Single-pulse short circuit test setup for the determination of t_{psc}; b) Basic voltage and current waveforms and specification of t_{psc} according IEC 60747-9

Because of the low loop impedance, the short circuit current in the conducting IGBT increases rapidly with a current slope depending on parasitic inductances and the operation voltage V_{CC}. Due to desaturation of the IGBT, the collector current is limited to a technology-dependent value, see Table 7.3.6. The collector-emitter voltage remains on the high level, the chip temperature increases rapidly due to high losses. The increase of IGBT chip temperature causes a slightly current decrease during operating in short circuit condition (Figure 7.3.12 b).

Within the time t_{psc} the IGBT has to be switched off to avoid a device failure. When switching off the short circuit current, the overvoltage at the parasitic inductances must not lead to the V_{CES} being exceeded.
Table 7.3.6 shows the permitted short circuit data and measured values of short circuit currents at maximum operational junction temperature $T_{j(op)}$ of chipsets used in current Semikron Danfoss IGBT modules.

IGBT chip series	$T_{j(op)}$ [°C]	V_{CC} [V]	V_{GE} [V]	t_{psc} [µs]	I_{sc}/I_{cnom}
650V IGBT E3	150	360	15	6	4…5
650V IGBT E4				10	3.8…5.4
1200V IGBT 3	125	600	15 (20)*	10	≈ 4
1200V V-IGBT	125	720	15	10	≈ 4.3
1200V IGBT T4/E4	150	800		10	≈ 4
1200V IGBT T7	150	800		8	3.2…4.5
	175			7 (6)*	3.2…4.3
1200V IGBT M7	150	800		8	≈ 3
1200V IGBT RA	150	800		8	≈ 5.3
1700V IGBT E4/P4	150	1000	15	10	≈ 4
1700V IGBT T7	150			8	≈ 3.5
	175			6	≈ 3.3
1700V IGBT R8	150	1200		10	≈ 4

Table 7.3.6 Permitted short circuit data of current Semikron Danfoss IGBT chipsets at $V_{CE} \leq V_{CES}$ (at chip level) and measured values of short circuit currents at maximum $T_{j(op)}$ in a test setup according Figure 7.3.12 a); * - dependent from product line

At V_{GE} values, specified in the IGBT module datasheet the short circuit current I_{sc} is self-limiting to the values, stated in Table 7.3.6. A higher supply voltage, a higher starting temperature or a higher gate-emitter voltage cause a reduction in short current withstand time t_{psc}.
In principle, the short circuit parameters can be varied at common energy level, e.g. for deviating DC link supply voltage:

$$t_{psc}(600V) = t_{psc}(800V) \cdot \frac{800V}{600V} = 10\mu s \cdot \frac{800V}{600V} = 13.6\mu s$$

or (by approximation of the diagram "Typical transfer characteristic") for deviating gate-emitter voltage:

$$t_{psc}(17V) = t_{psc}(15V) \cdot \frac{4 \cdot I_{Cnom}}{5 \cdot I_{Cnom}} = 6.4\mu s$$

Changed conditions resulting from short circuits with higher impedances (e.g, motor phase-to-phase short circuit) are described in more detail in chapter 9.5.4. Because the real gate-emitter-voltage on chip-level is influenced by the voltage gradient dV_{CE}/dt (Miller-effect), the gate-emitter voltage may also rise above the value specified as a reference for the time t_{psc}, which causes an increased collector current.
Please note that the active turn-off of short circuits is only permissible as single-pulse events - that means only applicate for a limited number of occurrences in the service life of the IGBT module. A number of 1000 possible short circuit events for IGBT is a common accepted value, but not a guaranteed or tested parameter.

Junction temperature range T_j; $T_{j(min)}$...$T_{j(max)}$

Permissible junction temperature range $T_{j(min)}$ to $T_{j(max)}$. For continuous and reliable operation, the maximum junction temperature $T_{j(op)}$ should be kept at least 25K below $T_{j(max)}$, see also "Remarks" in the shaded area to the left of the maximum ratings and characteristics. Where $T_{j(max)}$ is a physical limit for the semiconductor, for example can increased leakage current cause thermal runaway, is $T_{j(min)}$ more package related.
IGBT modules with 7th generation chip sets allow operation at $T_{j(op)} = T_{jmax}$ under certain overload conditions [7.28]. Figure 7.3.13 shows details of the maximum temperature definition and the allowed load profile. The nominal continuous operation is limited to a maximum junction temperature of $T_{j(op)}$ = 150°C. However, to match typical motor drive overload profiles it is allowed

to operate at 175°C for an absolute maximum time of t_1=60s. In addition, the overload duration is limited to a maximum duty cycle of 20%.

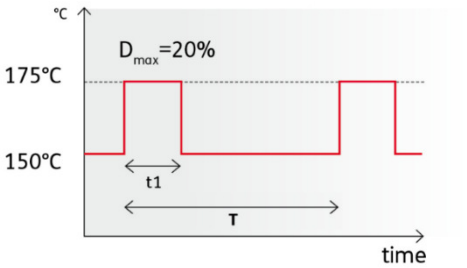
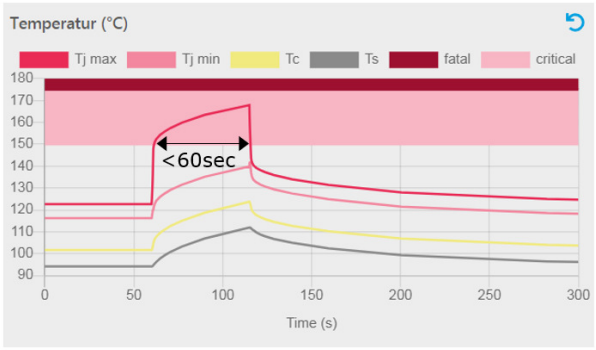


Figure 7.3.13 Definition of maximum operational junction temperature at 7th generation IGBT

Example: The overload time t_1 is limited to an absolute maximum duration of 60s, so the minimum permissible cycle time T is 300s or larger. If the load cycle time T is 25s the permissible overload with 150°C < $T_{j(op)-ol}$ ≤ 175°C is limited to t_1 ≤ 5s.

It is important to notice that the maximum junction temperature should never exceed 175°C including the temperature ripple originating from the fundamental output frequency. The lower the fundamental output frequency of an inverter the higher the temperature ripple in the junction becomes. The effect can be seen in Figure 7.3.14 for a converter application on an aircooled heatsink. At nominal load the fundamental output frequency is set to 50Hz which results in a moderate junction temperature swing of 7K. During overload condition, the current is increased and at the same time also the fundamental output frequency is reduced to 10Hz. This leads to a temperature swing of more than 25K.
The example on the left fulfils the defined overload conditions: The junction temperature never exceeds 175°C, exceeds 150°C for less than 60s and the duty cycle is lower than 20%.
The example on the right does NOT fulfil the defined overload conditions: The junction temperature is even lower than in the previous example, but the junction temperature exceeds 150°C for about 90s. Additionally the duty cycle is 30%.

Acceptable Overload Condition



Not Acceptable Overload Condition

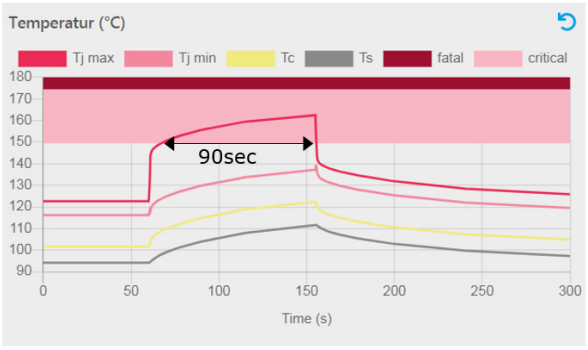


Figure 7.3.14 Example of acceptable and not acceptable overload condition

This overload definition is in particular beneficial for drives with well-defined load cycle conditions. Also fault situations e.g. low voltage ride-through can be covered without limiting the nominal operation.

Please note, that higher junction temperatures will lead to higher heatsink temperatures, which could imply additional limitations for the power module as well as other system components: Solder and wire bond connections in power modules are aging over time. The dominating factor is the junction temperature swing during load cycles.
An additional limitation is the maximum permissible power module case or housing temperature, which can be found in the module datasheet (see chapter below). This can be in particular critical for long overload durations of aircooled systems where the heatsink is subject to an additional temperature rise.

The maximum heatsink temperature underneath the power module will also affect the Thermal Interface Material (TIM). Please check the maximum permitted operation condition in the relevant TIM datasheet resp. Technical Explanation [7.29].

7.3.2.2 Maximum ratings of integrated inverse diodes (freewheeling diodes)

Repetitive peak reverse voltage V_{RRM}

Maximum permissible values for repetitive transient peak voltages in the reverse blocking state of the inverse diode at T_j = 25°C…T_{jmax}. Please note that VRRM is lower at very low temperatures.

Diode forward current I_F

Maximum permissible direct current at maximum permissible junction temperature T_{jmax}; parameters: for two different case temperatures for IGBT modules with baseplate or two different heatsink temperatures for baseplate-less modules.

Nominal diode current I_{Fnom} (in older datasheets only)

Rated current of the diode chips used as indicated in the chip manufacturer's datasheet, e.g. for CAL diodes "Nominal diode I_F rating, verified by design and characterisation", multiplied by the number of diode chips connected in parallel in the module per switch.

Repetitive peak forward current of the inverse diode I_{FRM}

The periodically permissible peak forward current in switching operation depends on the feasible power dissipation and the thermal impedance in the module, but also takes into account module-internal failure mechanisms at chip and bonding wires or due to overvoltage at the parasitic inductances.

Surge forward current I_{FSM}

If the inverse diodes are used as line rectifiers, their non-repetitive short-time overload capability is definitive for the choice of protective circuits. The non-repetitive peak forward current I_{FSM} in the form of a half-sine wave with pulse width, t_p, that the hybrid inverse diode (IGBT in off-state) is able at a specified junction temperature T_j to withstand in the event of a malfunction (e.g. short circuit), provided it does not occur too often during the diode lifetime.
When the device is subjected to a current near I_{FSM}, the junction temperature can reach values in excess of the permissible $T_{j(max)}$, causing damage to the chip metallization. Additionally, the blocking voltage capability of the diode immediately following the surge current event is reduced. The datasheet value of I_{FSM} is valid for an event in which the diode is not expected to block any reverse voltage.
Therefore, should a reverse voltage occur immediately after a diode has been exposed to surge current load, the permissible surge forward current peak will be lower than if no subsequent reverse voltage is involved. The duration of single or several subsequent phases can be determined from the surge forward current characteristics, also for conventional diodes (Figure 7.3.15).

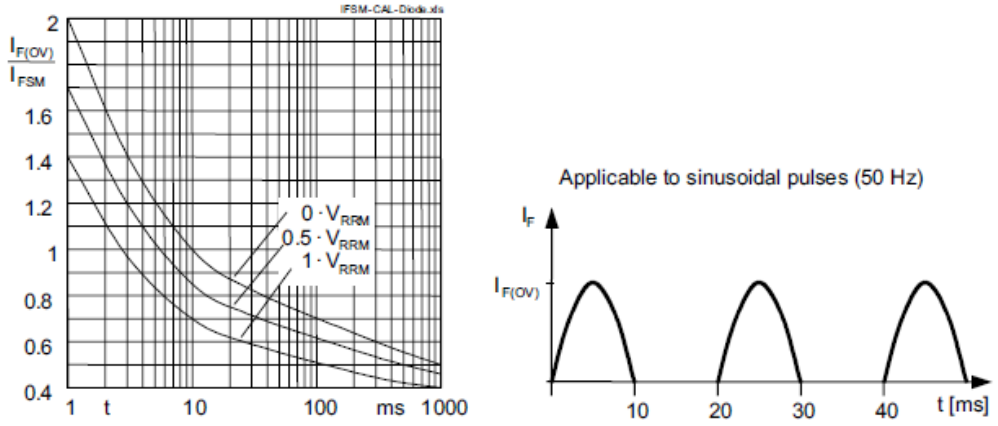


Figure 7.3.15 Surge forward current characteristics: Overload forward currents $I_{F(OV)}$ permissible in the event of a malfunction as a function of time related to surge forward current I_{FSM} at 10ms under different reverse voltage conditions directly after the last half sine wave.

The peak load integral required for the choice of fuses can be determined from I_{FSM} as follows.

$$\int_0^{t_{hw}} i_{FS}^2 \, dt = I_{FSM}^2 \cdot \frac{t_{hw}}{2}$$

t_{hw}: Duration of the sinusoidal half wave for which I_{FSM} applies (e.g. 10ms at 50Hz)

Junction temperature range T_j; $T_{j(min)}$...$T_{j(max)}$

Permissible junction temperature range $T_{j(min)}$ to $T_{j(max)}$. For continuous operation the maximum junction temperature $T_{j(op)}$ should be kept at least 25K below $T_{j(max)}$, see also "Remarks" in the shaded area to the left of the maximum ratings and characteristics.

7.3.2.3 Maximum module ratings

RMS terminal current $I_{t(RMS)}$

Maximum effective value of terminal current, averaged over a full operating cycle; is applicable to any current characteristic, conduction angle or cooling conditions. It depends on the current carrying capacity of the internal connections and the terminals of the IGBT module.

Storage temperature range T_{stg}; T_{stgmin}...T_{stgmax}

Temperature range within which the module may be stored or transported without being subject to electrical load; T_{stgmax} is also the maximum permissible case/housing temperature T_{cmax} for the modules in application. The housing material and especially the soft gel used for internal isolation is determining T_{stgmin}. Temperatures below that value might cause cracks in the gel which are not closing again after heating up and can cause isolation failure.
The storage temperature of the power module will also affect the Thermal Interface Material (TIM). The temperature limit values listed apply to an IGBT module without TIM coating. For TIM-coated modules, the permissible limit values of the specific TIM material must be adhered to.
Please check the maximum permitted operation condition in the relevant TIM datasheet resp. Technical Explanation [5.3].

Soldering temperature T_{sol} for the output terminals (for modules with soldered terminals)

Maximum temperature to which the output terminals may be exposed when soldered onto a PCB, with the parameter exposure time (see assembly instructions in chapter 10.1.3.4).

Insulation test voltage V_{isol}

RMS value of the permissible test voltage (50 Hz AC voltage) between the short circuited terminals and insulated module baseplate with the parameter test duration (1min or 1s); for details see chapter 10.3.5 and [7.19].

7.3.3 Characteristics

7.3.3.1 IGBT characteristics

In the datasheets, the characteristics are likewise specified separately for each individual component of an IGBT module. Again, all characteristics refer to one switch, irrespective of the number of paralleled IGBT or diode chips per switch in the transistor module (Figure 7.3.16).

Characteristics						
Symbol	Conditions		min.	typ.	max.	Unit
IGBT						
$V_{CE(sat)}$	I_C = 450 A, V_{GE} = 15 V, chiplevel	T_j = 25 °C		1.55	1.88	V
		T_j = 150 °C		1.80		V
V_{CE0}	chiplevel	T_j = 25 °C		0.87	0.95	V
		T_j = 150 °C		0.76		V
r_{CE}	V_{GE} = 15 V, chiplevel	T_j = 25 °C		1.51	2.1	mΩ
		T_j = 150 °C		2.3		mΩ
$V_{GE(th)}$	V_{CE} = 10 V, I_C = 45 mA		5.4	6	6.6	V
I_{CES}	V_{GE} = 0 V, V_{CE} = 1200 V, T_j = 25 °C				4.5	mA
C_{ies}	V_{CE} = 10 V, V_{GE} = 0 V	f = 1 MHz		90.0		nF
C_{oes}		f = 1 MHz		2.74		nF
C_{res}		f = 1 MHz		0.96		nF
Q_G	V_{GE} = -8V ... + 15V			4020		nC
R_{Gint}	T_j = 25 °C			1.0		Ω
$t_{d(on)}$	V_{CC} = 600 V, I_C = 450 A, V_{GE} = +15/-15 V, $R_{G\,on}$ = 1.1 Ω, $R_{G\,off}$ = 1.1 Ω, di/dt_{on} = 6300 A/µs, di/dt_{off} = 3800 A/µs, dv/dt = 5250 V/µs, L_s = 25 nH	T_j = 150 °C		280		ns
t_r		T_j = 150 °C		75		ns
E_{on}		T_j = 150 °C		39		mJ
$t_{d(off)}$		T_j = 150 °C		410		ns
t_f		T_j = 150 °C		100		ns
E_{off}		T_j = 150 °C		49		mJ
$R_{th(j-c)}$	per IGBT				0.083	K/W
$R_{th(c-s)}$	per IGBT (λ_{grease}=0.81 W/(m*K))			0.03		K/W
$R_{th(c-s)}$	per IGBT, pre-applied phase change material			0.021		K/W

Figure 7.3.16 IGBT characteristics of IGBT module SEMiX453GB12M7p

Collector-emitter saturation voltage $V_{CE(sat)}$

Saturation value of collector-emitter voltage (on-state voltage drop of the active IGBT) for a specified collector current I_C (usually at I_{Cnom}); parameters: gate-emitter voltage V_{GE}, junction temperature, e.g. T_j = 25°C/150°C.
At rated current, the $V_{CE(sat)}$ value of IGBT modules increases in proportion to temperature. $V_{CE(sat)}$ values usually refer to chip level (see relevant notes under "Conditions"). To calculate the saturation voltage across the main terminals, the voltage drop across the module lead resistors (bonding wires, terminals, ...) $R_{CC'+EE'}$ must be taken into account; when calculating chip losses, in contrast, this may be neglected.

Collector-emitter threshold voltage V_{CE0} and on-state slope resistance r_{CE} of the forward characteristic approximation

To calculate the forward losses, the elements of an equivalent straight line are given in the datasheets as

$$V_{CE(sat)} = f(I_C) = V_{CE0} + r_{CE} \cdot I_C$$

Figure 7.3.17 gives a definition of V_{CE0} and r_{CE}: r_{CE} is the slope of the line which results when $V_{CE(sat)}$ at 25% I_{Cnom} is connected with $V_{CE(sat)}$ at I_{Cnom}. V_{CE0} is the point where this line crosses the axis I_C = 0. Parameter: V_{GE}, T_j

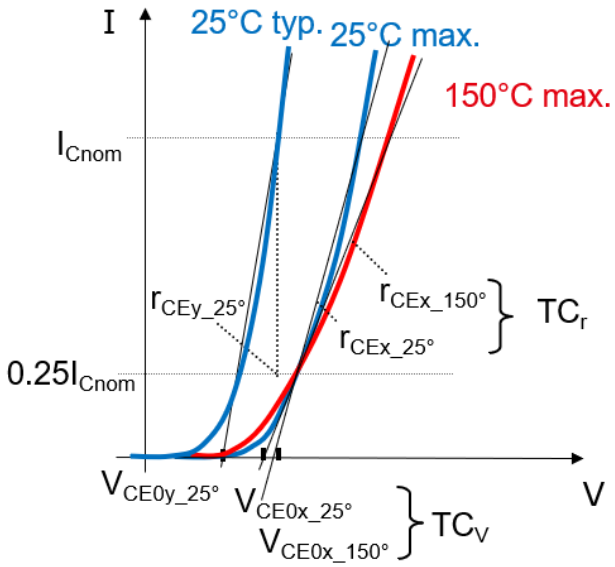


Figure 7.3.17 Forward characteristics of an IGBT and definition of the elements of an equivalent straight line

Gate-emitter threshold voltage $V_{GE(th)}$

Gate-emitter voltage above which considerable collector current I_C in the milliampere range (named in the datasheet) will flow at a given V_{CE} IGBT with low $V_{GE(th)}$ would switch on first and switch off later, which could lead to an imbalance in the switching losses of IGBT connected in parallel. Today's IGBT have a high degree of maturity in the production process, which guarantees a tight tolerance around the typical value.

Collector-emitter cut-off current I_{CES}

Collector-emitter blocking current at gate-emitter short circuited (V_{GE} = 0)
I_{CES} rises from sub µA range at T_j = 25°C to µA or even some mA at T_j = 150°C depending on the module size (rated current). Depending on V_{CES} this value multiplies by 1.5 to 2 every 10K of temperature rise. For modules with an integrated inverse diode, the blocking currents of both components are indicated only once as a common parameter I_{CES}.

Input capacitance C_{ies}

Low-signal, short circuit capacitance in common-emitter configuration between gate and emitter with collector-emitter short circuited for AC current; measured at specified collector-emitter direct voltage V_{CE} and specified measuring frequency f. It is electrically a parallel connection of C_{GE} and C_{GC}=C_{res}. (Table 7.3.7).

Output capacitance C_{oes}

Low-signal, short circuit capacitance in common-emitter configuration between collector and emitter with gate-emitter short circuited for AC current; measured at specified collector-emitter direct voltage V_{CE} and specified measuring frequency f. It is electrically a parallel connection of C_{CE} and C_{GC}=C_{res}.

Reverse transfer capacitance C_{res}

Low-signal capacitance in common-emitter configuration between collector and gate with gate-emitter short circuited for AC current; measured at specified collector-emitter direct voltage V_{CE} and specified measuring frequency f.
The increased C_{ies} value of Gen. 7 IGBT chips, can be solely attributed to an increased C_{GE} value while the Miller capacitance C_{GC} remains at a low level.
The combination of a large gate-emitter capacitance and a relatively small gate-collector capacitance makes the Gen. 7 IGBT chips very robust against undesired parasitic turn-on. This effect is usually induced from diode switching transients, which charge the gate through the Miller capacitance.

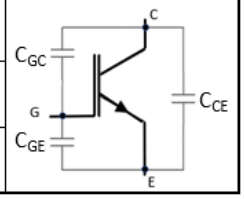
Description	IGBT	Equivalent Circuit
Input capacitance	$C_{ies} = C_{GE} + C_{GC}$	
Output capacitance	$C_{oes} = C_{GC} + C_{CE}$	
Reverse transfer capacitance	$C_{res} = C_{GC}$	

Table 7.3.7 Combination of internal transistor capacitances

Gate charge Q_G

The gate charge Q_G is the total charge required to transduce the IGBT from a defined off-state (gate-emitter voltage $V_{GE} = V_{GE(off)}$) to a defined saturation state ($V_{GE} = V_{GE(on)}$), specified at typical values of collector current I_C and operation voltage V_{CC} (Figure 7.3.18 and datasheet diagram, see Figure 7.3.32. The gate charge Q_G is almost independent of the junction temperature and only slightly dependent on the supply voltage.

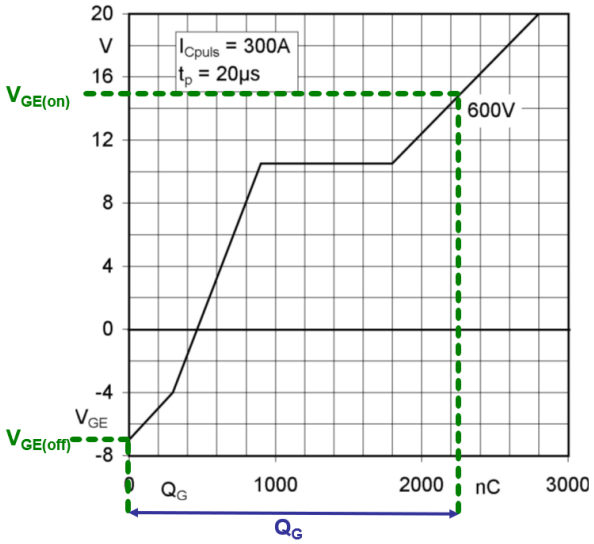


Figure 7.3.18 Gate charge characteristic of an IGBT

From Q_G using $I_{G(AV)} = Q_G \cdot f_{sw}$, the mean gate current supplied by the driver $I_{G(AV)}$ can be determined (f_{sw}: switching frequency).

Internal gate resistance R_{Gint}

Many IGBT chips are equipped with integrated gate resistors to avoid oscillations between paralleled chips. Consequently, the internal gate resistors of IGBT modules with paralleled IGBT chips are connected in parallel as well, where R_{Gint} is the total resistance resulting from paralleling. The datasheet Table contains a value for R_{Gint} at a junction temperature T_j = 25°C (R_{Gint} is temperature-dependent.). When configuring the driver circuit based on a minimum gate resistance or maximum gate peak current, the sum of the external gate resistances R_{Gon}, R_{Goff} and the internal gate resistance R_{Gint} given in the datasheet must be taken into account.

Switching times $t_{d(on)}$, t_r, $t_{d(off)}$, t_f and switching energies E_{on}, E_{off}

Switching times indicated in IGBT module datasheets are determined from a measuring circuit under inductive load in accordance with Figure 7.3.19 a). The load should be large enough to keep the current constant during freewheeling. When the IGBT is switched off, the current flows through the freewheeling diode, commutates to the IGBT at the second turn-on and back to the freewheeling diode on turn-off (hard switching). Switching times and energies refer to the gate-emitter voltage and collector current characteristics during turn-on and turn-off.
In the tabular datasheet characteristics, switching times and switching energies are given at maximum operational junction temperature $T_{j(op)}$ for a typical IGBT operating point, characterised by supply voltage V_{CC}, nominal collector current I_{Cnom}, gate control voltages $\pm V_{GE}$, external gate

resistances R_{Gon}, R_{Goff}, collector current slopes di/d_{ton} during turn-on and di/dt_{off} during turn-off, collector-emitter voltage slope dv/dt as well as commutation circuit stray inductance L_s.

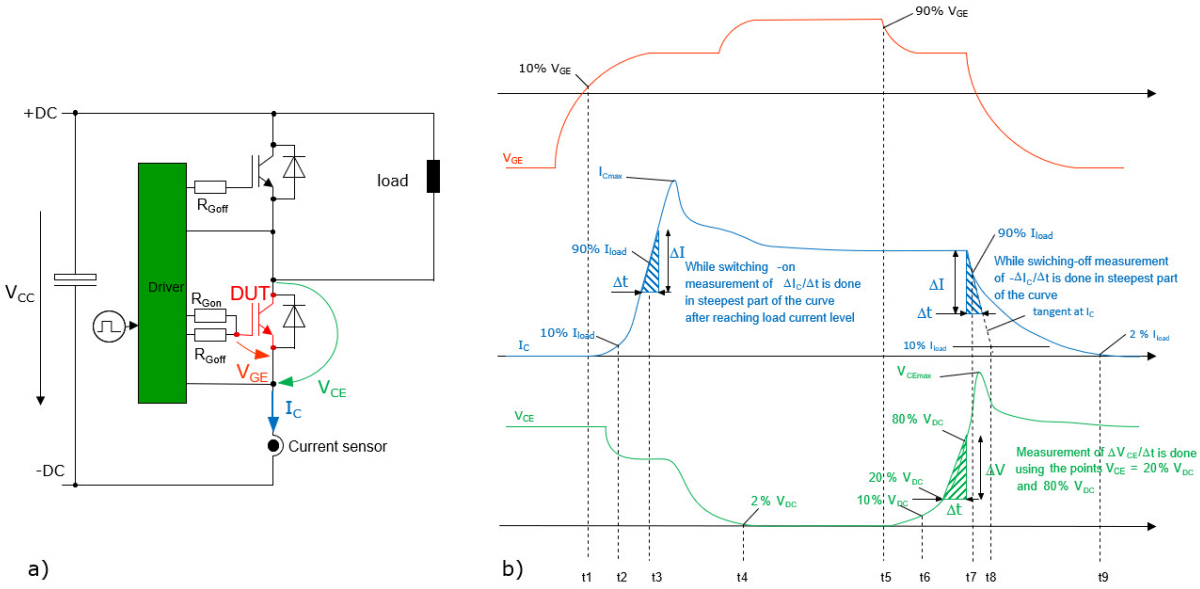


Figure 7.3.19 Switching times of IGBT: a) Measuring circuit; b) Definition of switching times at ohmic-inductive load [7.30]

The following explanations refer to the times t_1...t_9 shown in Figure 7.3.19 b).
The turn-on delay time $t_{d(on)}$ (interval t_1…t_2) is defined as the time interval between the moment when the rising gate-emitter voltage v_{GE} has reached 10% of its positive end value and the collector current i_C has increased to 10% of the load current. During the subsequent rise time t_r (interval t_2…t_3), the collector current i_C increases from 10% to 90% of the load current. The sum of turn-on delay time $t_{d(on)}$ and rise time t_r is called turn-on time t_{on}.
The turn-on energy E_{on} given in the datasheets for IGBT modules is calculated by

$$E_{on} = \int P_{on}\,dt = \int_{t2}^{t4} v_{CE} \cdot i_c\,dt$$

and includes the power losses caused by the peak reverse current I_{RRM} induced by the reverse recovery of the freewheeling diode. Furthermore, E_{on} comprises the integral of the turn-on power dissipation P_{on} up to the moment where the collector-emitter voltage v_{CE} has reached 2% of the dc supply voltage V_{CC}, i.e., the power losses during dynamic saturation of the IGBT described in chapter 2.4.3 are also included. The Figure 7.3.20 shows measured curves of v_{GE}, v_{CE}, i_c and $i_c \cdot v_{CE}$ during turn-on, including the current commutation from a conducting silicon freewheeling diode to the IGBT.
Please note that IGBT modules equipped with hybrid SiC Schottky diodes (hybrid SiC Modules) have significantly reduced turn-on losses, see also chapter 7.3.3.2.

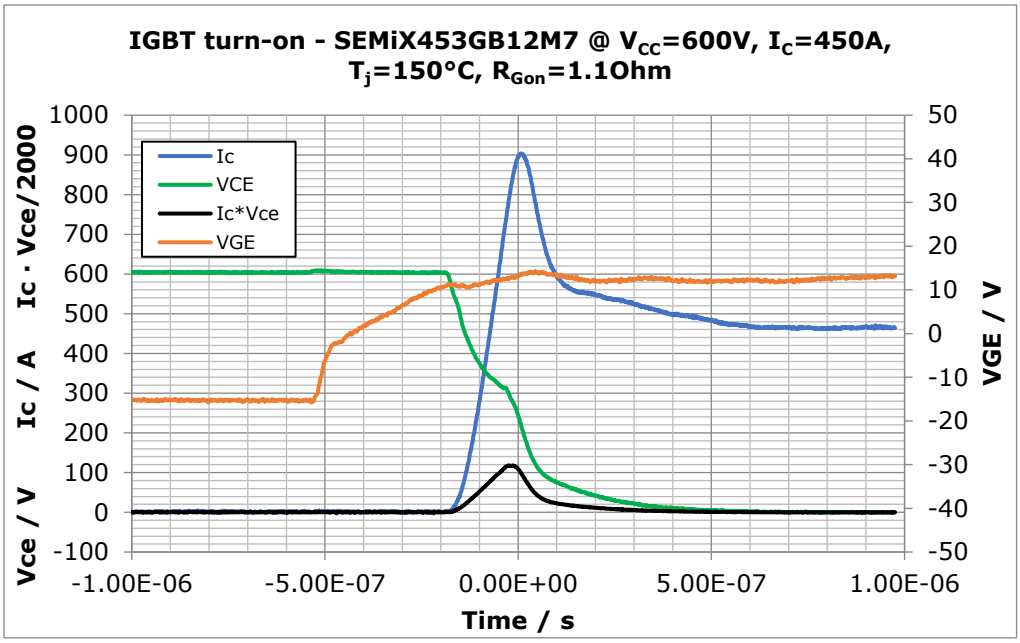


Figure 7.3.20 IGBT turn-on (commutation from conducting freewheeling diode to the IGBT)

The turn-off delay time $t_{d(off)}$ is defined as the time interval between the moment when the gate-emitter voltage v_{GE} has dropped to 90% of its on-state value and the collector current has declined to 90% of the load current value (interval $t_5 \ldots t_7$).
During the subsequent fall time t_f (interval $t_7 \ldots t_8$), the collector current i_C drops from 90% to 10% of the load current I_L.
The sum of turn-off delay time $t_{d(off)}$ and fall time t_f is called turn-off time t_{off}.
Please note that the range of the collector current drop between 10% of the load current I_L and the cut-off current is not included in the times t_f resp. t_{off} by definition. The collector current decreasing after t_{off} is called tail current I_t and results from the concentration of minority carriers in the n^- zone, which is mainly reduced by means of recombination (see chapter 2.4.3). Nowadays, tail current I_t and tail time t_t values are not specified explicitly in the datasheets.
Nevertheless, it contributes to the switching losses; this is owing to the collector-emitter supply voltage V_{CC} which has already been applied during that time interval.
The turn-off energy E_{off} given in the datasheets for IGBT modules is calculated by

$$E_{off} = \int P_{off}\,dt = \int_{t6}^{t9} v_{CE} \cdot i_c\,dt$$

and thus covers the time interval from v_{CE} is dropped to 10% of V_{CC} to i_C is dropped to 2% of the load current I_L. This means that the E_{off} includes the power losses during the tail current interval and also the losses caused by the v_{CE} overshoot during di_C/dt_{off}. The turn-off overvoltage results from the parasitic inductances in the commutation circuit, increasing proportionally with increasing turn-off speed $-di/dt_{off}$ of the IGBT.
Figure 7.3.21 shows measured curves of v_{GE}, v_{CE}, i_c and $i_c \cdot v_{CE}$ during turn-off, including the current commutation from IGBT to a freewheeling diode. It shows also that the gate is already closed (negative V_{GE} at t=0) but current is still flowing. The current is fed by the high charge carrier concentration inside the IGBT and makes the turn-off behaviour (E_{off}, t_f, di/dt, dv/dt) independent from chosen R_{Goff} in a wide range. Controllability can only be achieved with very large R_{Goff}. Switching times and losses linear rise with the junction temperature.

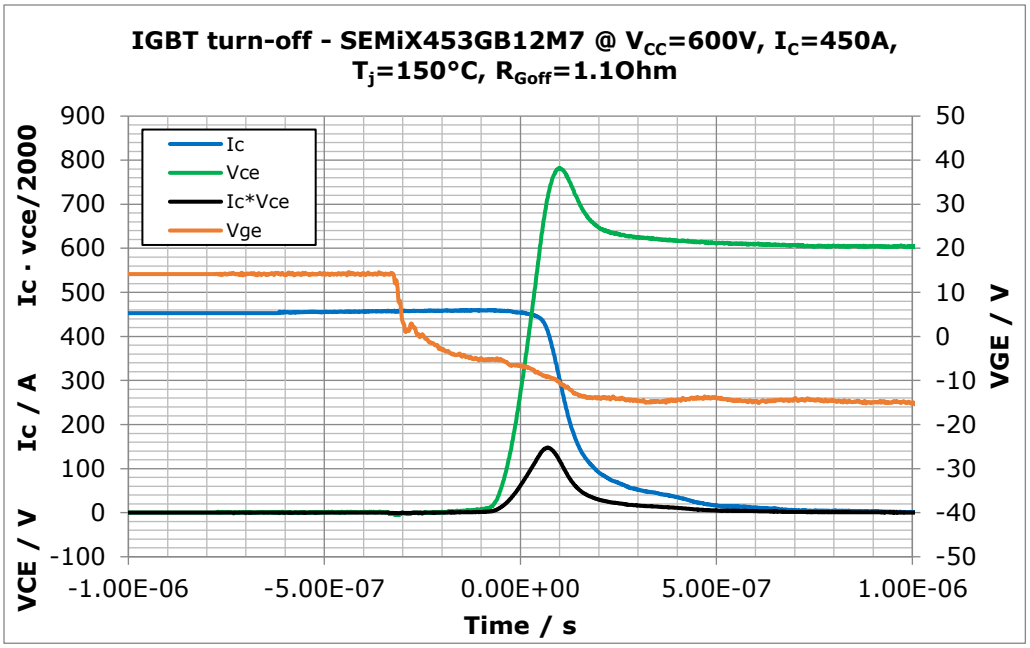


Figure 7.3.21 IGBT turn-off (commutation from the IGBT to a freewheeling diode)

The switching losses and times are given for the worst switch within a housing (e.g. TOP or BOT switch in halfbridge, depending on which has the higher losses). Several of those switches are measured and given as a typical value in the datasheet. The deviations of the switching parameters caused by the scattering of the semiconductor parameters are in the range of +/- 10%. Deviations in the same range or even higher are caused by the circuit itself. The switching parameter are determined under laboratory conditions using a powerful driver with stabilised power supply, ideal inductive load and a certain set of parasitic inductances (gate and commutation loop) and coupling capacitances. For sure the conditions will be different in the environment of the application. internal and external capacitances, inductances and resistances of the gate and collector circuit. That is one reason that the data given in the datasheets can be given only as typical values and must be seen as a guideline only. Furthermore for applications under operating conditions which differ clearly from the measuring conditions or in which the switching losses are the dominating losses, it is imperative that additional measurements be conducted in the real application environment to ensure safe layout of the circuitry.

Thermal resistances $R_{th(j-c)}$, $R_{th(c-s)}$ or $R_{th(j-s)}$ per IGBT switch

These thermal resistances are given for an IGBT switch within a module, irrespective of the number of IGBT chips connected in parallel. In chapter 6.2.1 the different thermal models for modules with baseplate (case rated devices) and without baseplate (heatsink rated devices) are explained.
In a module with baseplate, $R_{th(j-c)}$ describes the passage of heat between the IGBT chips (index j) and the module case (index c). $R_{th(j-c)}$ cannot be determined for modules without baseplate (SEMITOP, SKiiP, SKiM, MiniSKiiP), which is why, in these cases, the thermal resistance $R_{th(j-s)}$ between the IGBT chips and heatsink is indicated for every IGBT switch.
In current datasheets Semikron Danfoss usually specifies the thermal resistances with two different thermal interface materials:

- standard thermal grease (thermal conductivity λ_{grease} = 0.81W/(m · K)
- pre-applied phase change material or HPTP "High performance thermal paste" (thermal conductivity λ_{grease} = 0.81W/(m · K)

The R_{th} are given for the worst switch within a housing (e.g. TOP or BOT switch in halfbridge, depending on which has the value). Several of those switches are measured. The average of the worst switch is given as a typical value $R_{th(j-s)}$ for baseplate-less modules in the datasheet. The maximum measured value plus a certain safety margin is given as a maximum $R_{th(c-s)}$ in modules with baseplate.

7.3.3.2 Characteristics of integrated inverse diodes (freewheeling diodes)

The characteristic data of the module-integrated inverse diodes are illustrated in the table, shown in Figure 7.3.22.

Characteristics						
Symbol	Conditions		min.	typ.	max.	Unit
Inverse diode						
$V_F = V_{EC}$	I_F = 450 A V_{GE} = 0 V chiplevel	T_j = 25 °C		2.14	2.46	V
		T_j = 150 °C		2.07	2.38	V
V_{F0}	chiplevel	T_j = 25 °C		1.30	1.50	V
		T_j = 150 °C		0.90	1.10	V
r_F	chiplevel	T_j = 25 °C		1.87	2.1	mΩ
		T_j = 150 °C		2.6	2.8	mΩ
I_{RRM}	I_F = 450 A di/dt_{off} = 6400 A/µs V_{GE} = -15 V V_{CC} = 600 V	T_j = 150 °C		430		A
Q_{rr}		T_j = 150 °C		76		µC
E_{rr}		T_j = 150 °C		35		mJ
$R_{th(j-c)}$	per diode				0.107	K/W
$R_{th(c-s)}$	per diode (λ_{grease}=0.81 W/(m*K))			0.045		K/W
$R_{th(c-s)}$	per diode, pre-applied phase change material			0.036		K/W

Figure 7.3.22 Characteristic values of the inverse diodes (freewheeling diode), integrated in an IGBT module SEMiX453GB12M7p

Forward voltage $V_F = V_{EC}$ of an inverse diode

Voltage drop across the collector-emitter main terminals in reverse direction at V_{GE} = 0V; forward current I_F value at I_{Cnom} for junction temperatures T_j = 25°C/150°C.
V_F values included in the recent datasheets usually refer to chip level (see relevant notes under "Conditions"). To calculate the forward voltage across the main terminals, the voltage drop across the module lead resistors (bonding wires, terminals, ...) $R_{CC'+EE'}$ (explained under module layout characteristics) must be taken into account; when calculating chip losses, in contrast, this may be neglected. The forward characteristics diagram in Figure 7.3.38 illustrate the temperature coefficient of V_F which changes from negative to positive in the rated current range.

Threshold voltage V_{F0} and forward slope resistance r_F of an inverse diode

To calculate the inverse diode forward losses, the elements of an equivalent straight line are indicated in the datasheets; here, the definitions correspond to those for V_{CE0} and r_{CE} as given in "IGBT Characteristics": $V_F = f(I_F) = V_{F0} + r_F \cdot I_F$. V_{F0} and r_F are given at V_{GE} = 0V for junction temperatures T_j = 25°C/150°C.

Peak reverse recovery current I_{RRM}, recovered charge Q_{rr} and turn-off energy E_{rr} of the inverse diode

The dynamical characteristics of the module-integrated freewheeling diode indicated in the IGBT module datasheets are determined from a measuring circuit under inductive load in accordance with Figure 7.3.19 a). Normally, only the turn-off characteristics of the freewheeling diode are important for the power loss balance.
In the tabular datasheet characteristics, I_{RRM}, Q_{rr} and E_{rr} are given at maximum operational junction temperature $T_{j(op)}$ for a typical IGBT module operating point, characterised by supply voltage V_{CC}, diode current I_F before commutation (in the range of I_{Cnom} of the IGBT), IGBT turn-off gate control voltage $V_{GE(off)}$ and current slope di/dt_{off} (measured around zero crossing of the diode current). The following explanations refer to the curves shown in Figure 7.3.23, using the measuring circuit shown in Figure 7.3.19 a).

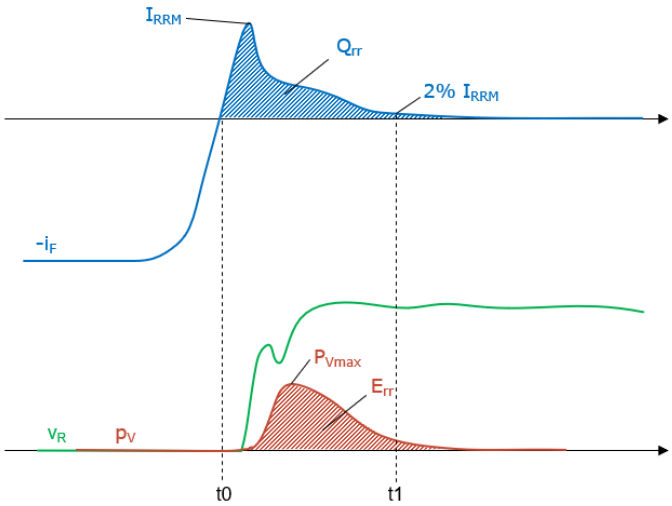


Figure 7.3.23 Dynamical characterisation of IGBT module's freewheeling diode

The current I_{RRM} is the peak value of the reverse current after inverse diode switchover from forward current I_F to reverse blocking state. The total recovered charge Q_{rr} - flowing from the diode to the outer circuit after switchover from forward current I_F at to reverse blocking state - has to be taken up by the IGBT during turn-on. Per definition, the measurement interval for the recovered charge Q_{rr} and the turn-off energy E_{rr} is from t_0 (zero crossing of diode current) to t_1 (reverse current is dropped down to 2% of peak reverse current I_{RRM}), see Figure 7.3.23.
For IGBT modules equipped with hybrid SiC Schottky barrier freewheeling diodes (Hybrid SiC Modules) the tabular "Characteristics" dataset is changed because of not existing reverse recovery behaviour. Information on I_{RRM}, Q_{rr} and E_{rr} are omitted. Instead, the values are given for the junction capacitance C_j, and stored charge Q_c of the Schottky barrier diode. Please refer to chapter 7.5.3 for more information. Figure 7.3.24 shows characteristics courses of v_{GE}, v_R, i and $i \cdot v_R$ during diode turn-off (current commutation to IGBT).

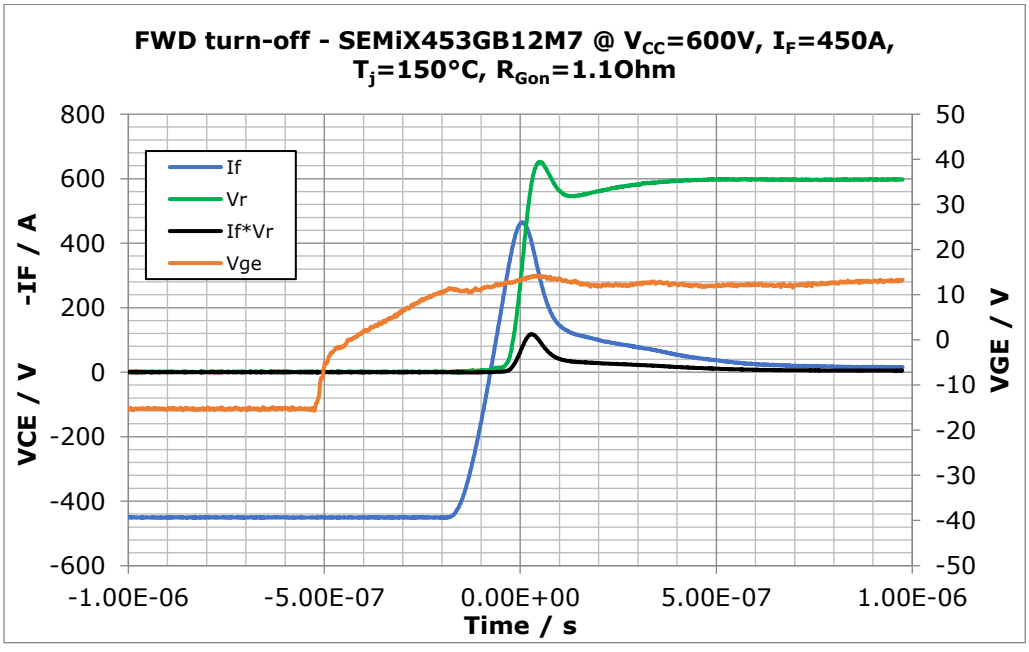


Figure 7.3.24 Voltage, current and switching loss curves during turning-off a conductive freewheeling diode (commutation from the diode to an IGBT), I_F inverted

As with the IGBT, the dynamic diode characteristics are also highly temperature-dependent.

Thermal resistances $R_{th(j-c)}$, $R_{th(c-s)}$ or $R_{th(j-s)}$ per inverse diode

The explanations given for the characteristic "Thermal resistances $R_{th(j-c)}$ and $R_{th(j-s)}$ per IGBT" also apply to inverse diodes, provided the "IGBT" is replaced by "inverse diode" and P_T is replaced by

P_D.

7.3.3.3 Module specific characteristics

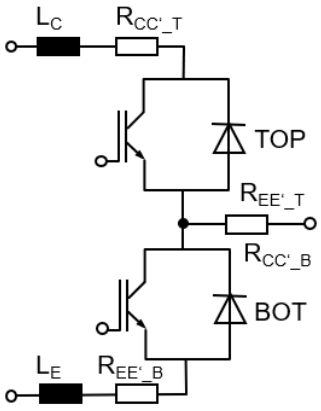
The characteristic data to be assigned to the complete IGBT module are illustrated in the Table, shown in Figure 7.3.25.

Characteristics						
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Unit**
Module						
L_{CE}				20		nH
$R_{CC'+EE'}$	measured per switch	T_C = 25 °C		0.95		mΩ
		T_C = 125 °C		1.25		mΩ
$R_{th(c-s)1}$	calculated without thermal coupling			0.009		K/W
$R_{th(c-s)2}$	including thermal coupling, T_s underneath module (λ_{grease}=0.81 W/(m*K))			0.014		K/W
$R_{th(c-s)2}$	including thermal coupling, T_s underneath module, pre-applied phase change material			0.010		K/W
M_s	to heat sink (M5)		3		6	Nm
M_t		to terminals (M6)	3		6	Nm
						Nm
w					350	g

Figure 7.3.25 Module-specific characteristics of an IGBT module SEMiX453GB12M7p

Collector-emitter commutation inductance L_{CE}

Sum of all (parasitic) stray inductances between collector (TOP) and emitter (BOT) terminal determined from the inductive voltage drop measured during switching. The partial inductances L_C and L_E depicted in Figure 7.3.26 represent the total inductances of the bond connections and terminals.



$L_{CE} = L_C + L_E$

L_C and L_E might be coupled inductances

$R_{CC'-EE'} = \mathrm{Max}(R_{CC'\_T} + R_{EE'\_T};\ R_{CC'\_B} + R_{EE'\_B})$

Figure 7.3.26 Simplified circuit of stray inductances and ohmic lead resistances of an IGBT module

Parasitic ohmic terminal-to-terminal lead resistances $R_{CC'+EE'}$

In recent datasheets, $V_{CE(sat)}$ and V_F are normally given at chip level (see relevant note under "Conditions"); for this reason the voltage drop across the module lead resistors (bond wires, terminals etc.) must be determined separately in order to calculate the saturation voltage across the main terminals. To do so, all partial resistances of one half-bridge module are pooled to obtain the terminal resistance $R_{CC'+EE'}$ indicated in the datasheet. The highest value from different pathes through a module is given in the datasheet, normally the BOT-path in an halfbridge module. Again, the partial resistances $R_{CC'}$ and $R_{EE'}$ depicted in Figure 7.3.26 also represent the sum of resistances of the bond connections and terminals. Because of the temperature dependence of the cooper leads, in the datasheets the ohmic resistance $R_{CC'+EE'}$ is given at two case temperatures, e.g. at T_c =25°C/125°C.

Thermal resistance $R_{th(c-s)1}$ and $R_{th(c-s)2}$ per IGBT baseplate module

For IGBT modules with baseplate, Semikron Danfoss specifies two thermal resistances $R_{th(c-s)}$ between the baseplate and heatsink in current datasheets, which are determined in different ways: $R_{th(c-s)1}$ per module is calculated without thermal coupling of switches by a virtual parallel connection of all $R_{th(c-s)}$ of the module.

$$R_{th(c-s)1} = \left(\frac{n}{R_{th(c-s)I}} + \frac{n}{R_{th(c-s)D}}\right)^{-1}$$

n: number of switches per module
$R_{th(c-s)I}$: thermal resistance case-heatsink per IGBT switch
$R_{th(c-s)D}$: thermal resistance case-heatsink per diode switch

This theoretical value could be reached only if the distance between all switches is wider than 3…4 times the thickness of the material stack "chip-to-heatsink" (15mm…20mm), but this seldom the case in recent IGBT modules. Therefore, this theoretical value can never be reached.
The value of $R_{th(c-s)2}$ per module is valid for a typical distribution of power dissipation between the switches, includes thermal coupling and is specified for thermal interface material with λ = 0.81W/(m·K) or pre-applied phase changer material. The $R_{th(c-s)}$ specified in older datasheets alone was determined under similar conditions to the current $R_{th(c-s)2}$. Please refer to [7.21] for more detailed explanations. In actual IGBT module datasheets (from 2014 onwards), the previously used reference point beside of the module T_s to measure heatsink temperature is replaced by the reference point T_s underneath the module, as it is already used for other module families.
Please note, that all $R_{th(j-s)}$ and $R_{th(c-s)}$ datasheet statements are valid only if the modules are mounted according to the mounting instructions using the specified thermal grease material and layer thickness.

Mechanical data Ms, M_t, w

The following mechanical data is provided in the datasheets:

- Mounting torque M_s of the fixing screws (minimum and maximum values)
- Mounting torque M_t of the terminals (minimum and maximum values)
- Module weight w.

Characteristics of an internal temperature sensor R_{ts}, R100, B100/125, tolerance

The modules in various Semikron Danfoss product lines (SEMiX, MiniSKiiP, SKiiP, SEMITOP, SKiM) are equipped with temperature sensors positioned next to the chips on the DBC ceramic substrate. Depending on their position, these sensors represent a temperature that is close to that of the baseplate (for modules with bas plate) or that of the heatsink (for baseplate-less modules). Depending on the product line, PTC (Positive Temperature Coefficient) or NTC (Negative Temperature Coefficient) resistors are used, the resistance of which rises or falls linear to the temperature. In the datasheets, temperature sensor specifications include the internal resistance R_{ts} or R100 at 25°C and 100°C, for a measuring tolerance at 100°C and in some cases the coefficient B100/125.
Table 7.3.8 lists the IGBT modules in which temperature sensors with a positive (PTC) or negative (NTC) temperature coefficient characteristic are integrated.

Product group	Temperature Sensor characteristic	Description included in Technical Explanation
SEMITRANS classic	n. a.	
SEMITRANS 10	NTC	
SEMITRANS 20	NTC	
MiniSKiiP	PTC	[7.31]
SEMITOP	NTC	[7.32], [7.33]
SEMiX	NTC	[7.34]
SKiiP	PTC	[7.36], [7.37], [7.38]
SKiM	NTC	[7.39]
SEMIPONT 6	PTC	[7.40]

Table 7.3.8 Characteristics of temperature sensors in various IGBT module product lines

The types of sensors used in specific products, as well as their properties are explained in detail in chapter 3.2.8 and in the product line specific Technical Explanation, see Table above,
For deeper explanations about calculating T_j by using the module temperature sensor please refer [7.41].

7.3.4 Diagrams

Similar to the sequence in the datasheets, this chapter provides information on the diagrams in Semikron Danfoss IGBT module datasheets, which generally refer to one IGBT or freewheeling diode switch or to the module behaviour. Some diagrams presented here are not shown in all of the datasheets, as some are specific to certain product line. Also, a different sequence is possible, individual diagrams may be missing or additional diagrams may be included.

Typical output characteristics $I_C = f(V_{CE})$ including $R_{CC'+EE'}$

The diagrams illustrates the positive temperature coefficient of the collector-emitter saturation voltage $V_{CE(sat)}$ and the decrease of this voltage in line with the increase in gate-emitter voltage V_{GE}. Different reference options are used in different datasheets to illustrate the IGBT output characteristic.
Figure 7.3.27 a) shows the typical output characteristic for T_j = 25°C and 150°C in saturation region using parameter V_{GE}. In contrast to the tabular data, the diagrams illustrate the voltage drop across the module terminals; the V_{CE} value includes the voltage drops over the parasitic terminal resistances $R_{CC'+EE'}$.
Figure 7.3.27 b) show the typical output characteristic for T_j = 25°C, 125°C and 150° for a fixed gate voltage V_{GE} = 15V without taking into account the voltage drops over the parasitic terminal resistances and according to the tabular information in the datasheet.
Figure 7.3.27 c) shows the typical IGBT output characteristic for the V_{GE} range 8V to 20V at T_j = 150°C, including also the desaturation region.

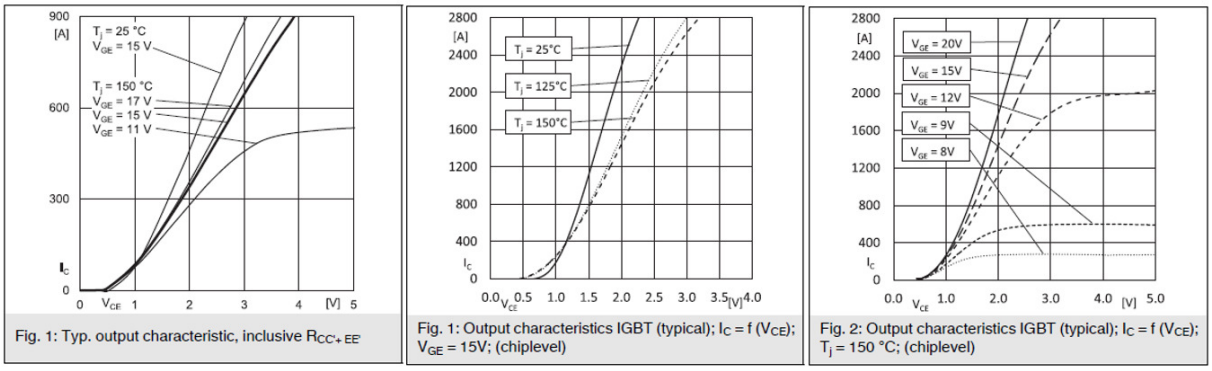


Fig. 1: Typ. output characteristic, inclusive $R_{CC'+EE'}$

Fig. 1: Output characteristics IGBT (typical); $I_C = f(V_{CE})$; V_{GE} = 15V; (chiplevel)

Fig. 2: Output characteristics IGBT (typical); $I_C = f(V_{CE})$; T_j = 150 °C; (chiplevel)

a) b) c)

Figure 7.3.27 Typical IGBT output characteristics $I_C = f(V_{CE})$ of an IGBT module; a) SEMiX453GB12M7p including $R_{CC'+EE}$; b) and c) SKM1400GB17R8 [7.41] on chip level

Collector current I_C derating versus case temperature T_c

Figure 7.3.28 shows different diagrams of the derating of the maximum continuous collector current (without additional switching losses) which is required if the case resp. sink temperatures differ from the reference temperatures T_c = 25°C (or T_s = 25°C for baseplate-less modules), often given as a parameter for the maximum I_C in the datasheet Table "Absolute Maximum Ratings". At temperatures above T_c = 25°C, the relation is:

$$I_C = \frac{(T_{jmax} - T_c)}{R_{th(j-c)} \cdot V_{CE(sat)}}$$

At case or sink temperatures below 25°C, the maximum rated collector current is limited to the 25°C value. In some diagrams for baseplate-less modules, the influence of different thermal interface materials is taken into account. Figure 7.3.28 b) shows an example for derating curves of the rated collector current as a function of the heatsink temperature for thermal paste Wacker P12 (λ_{paste} = 0.8W/(m·K) and for high-performance thermal paste (λ_{paste} = 2.5W/(m·K). If the permissible collector current is limited by the effective current carrying capacity of the load terminals, the diagram also contains this restriction, see example Figure 7.3.28 c).

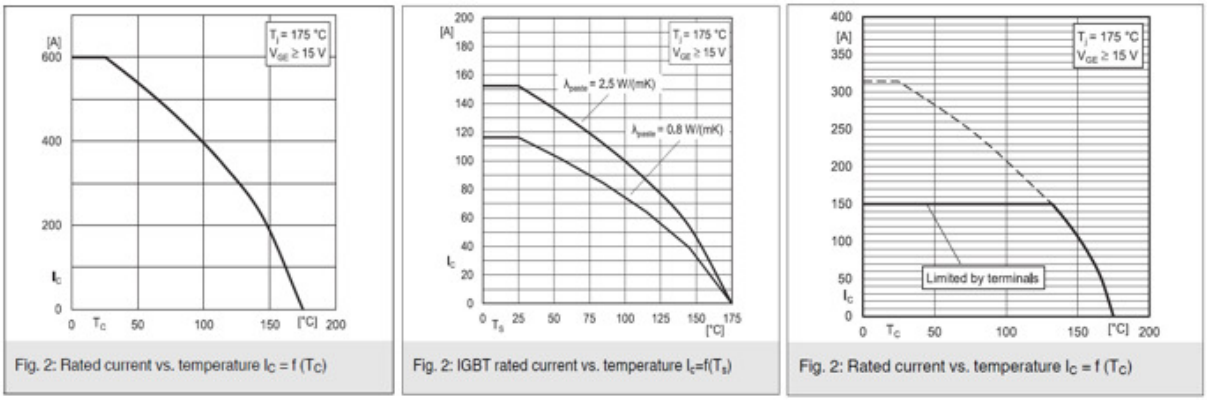


Figure 7.3.28 Derating of I_C versus T_C of an IGBT module: a) SEMiX 3p module SEMiX453GB12M7p with baseplate; b) SEMITOP E2 module SK100GD12T7ETE2 [7.43] without baseplate; c) SEMiX 6p module SEMiX206GD12T4p [7.44] with additional current limiting by the current capability of load terminals

Please note, that here the term case temperature T_c (T_s) refers to the baseplate (sink) temperature under the chips. The maximum permissible frame temperature of the plastic case is significantly lower. It corresponds to the maximum permissible storage temperature T_{stgmax} of the module or is indicated as "Electrical Relative Thermal Index (RTI)" temperature which relates to electrical insulating performance. The RTI-value is the characteristic parameter related to thermal degradation of the plastic material; related long-term tests are specified in the standard UL 746B [7.45].

Typical switching energies E_{on}, E_{off} and E_{rr} as a function of the collector current I_C

Figure 7.3.29 shows different diagrams for the typical turn-on / turn-off energies E_{on}, E_{off} of the IGBT and the turn-off energy E_{rr} of the freewheeling diode. The measurement was carried out at the highest recommended operating temperature, a typical working voltage V_{CC} (e.g. 600V for 1200V or 900V for 1700V IGBT) and the further conditions under which the typical switching energies are specified in the table section of the datasheet. The diagrams of some IGBT modules additionally contain curves for lower junction temperatures and/or a separate diagram for the freewheeling diodes E_{rr}.

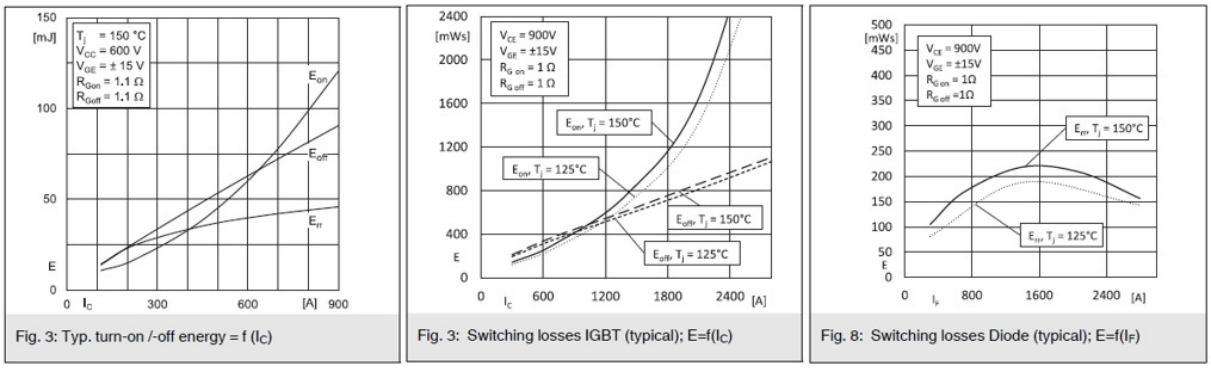


Figure 7.3.29 Turn-on/turn-off energies of IGBT and freewheeling diode versus collector current: a) SEMiX453GB12M7p, common depiction for T_j = 150°C; b), c) SKM1400GB12P4 [7.46], displayed in separate diagrams at T_j = 125°C and 150°C

Typical switching energies E_{on}, E_{off} and E_{rr} versus external gate resistances R_{Gon}, R_{Goff}

Figure 7.3.30 shows the typical turn-on / turn-off energies E_{on}, E_{off} of the IGBT at a typical high-current operating point and the turn-off energy E_{rr} of the freewheeling diode. The measurement was carried out at the highest recommended operating temperature, a typical working voltage V_{CC} (e.g. 600V for 1200V or 900V for 1700 IGBT) and the further conditions under which the typical switching energies are specified in the table section of the datasheet. The diagrams of some IGBT

modules additionally contain curves for lower junction temperatures and/or a separate diagram for the freewheeling diodes E_{rr}.

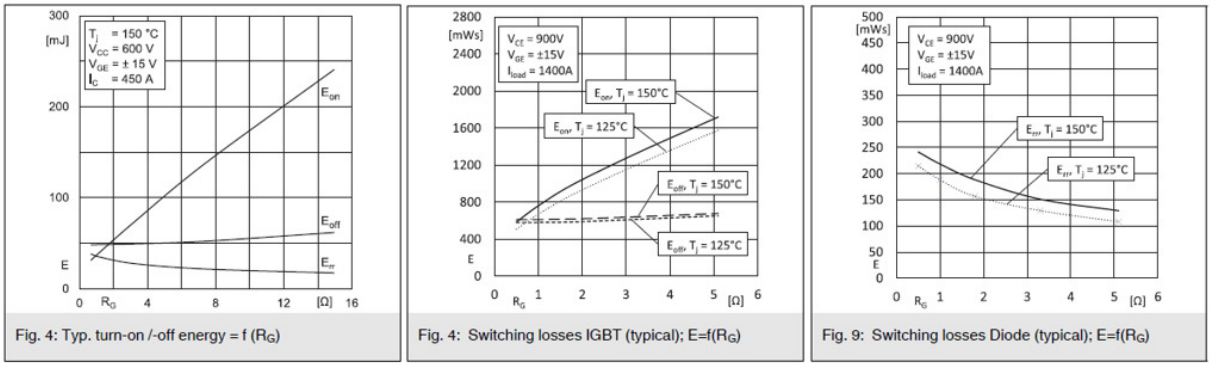


Fig. 4: Typ. turn-on /-off energy = f (R_G)

Fig. 4: Switching losses IGBT (typical); E=f(R_G)

Fig. 9: Switching losses Diode (typical); E=f(R_G)

a) b) c)

Figure 7.3.30 Turn-on/turn-off energies of IGBT and freewheeling diode versus gate resistance: a) SEMiX453GB12M7p, common depiction for T_j = 150°C; b), c) SKM1400GB12P4, displayed in separate diagrams, T_j = 125°C and 150°C

Transfer characteristic $I_C = f(V_{GE})$

The typical transfer characteristic in Figure 7.3.31 illustrates the behaviour of the IGBT in the active operating area at V_{CE} = 20V (linear operation). The collector current is coupled with the gate-emitter voltage via $I_C = g_{fs} \cdot (V_{GE} - V_{GE(th)})$. Especially during turn-on is the rising collector current linked to the rising V_{GE} according to this characteristic.

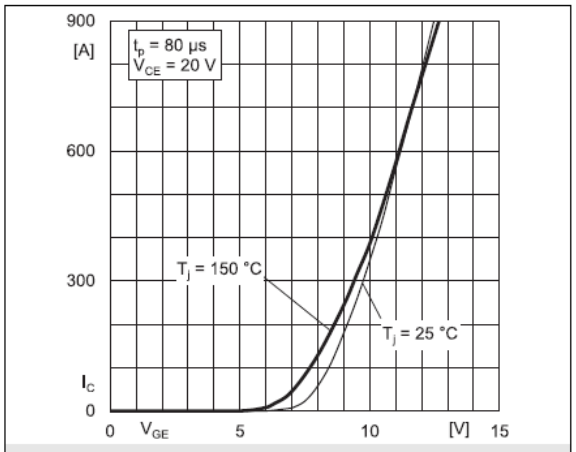


Fig. 5: Typ. transfer characteristic

Figure 7.3.31 IGBT transfer characteristic of an IGBT module SEMiX453GB12M7p

Typical gate charge characteristic $V_{GE} = f(Q_G)$

Figure 7.3.32 shows the typical dependency of the IGBT gate-emitter voltage V_{GE} on the gate charge Q_G at I_{Cnom} and a typical working voltage V_{CC} (600V/900V for 1200V/1700V IGBT).
The gate charge characteristic illustrates the course of V_{GE} between off-state at a conventional negative gate-emitter voltage V_{GE} (-8V or -15V) and on-state at maximum permissible V_{GE}.

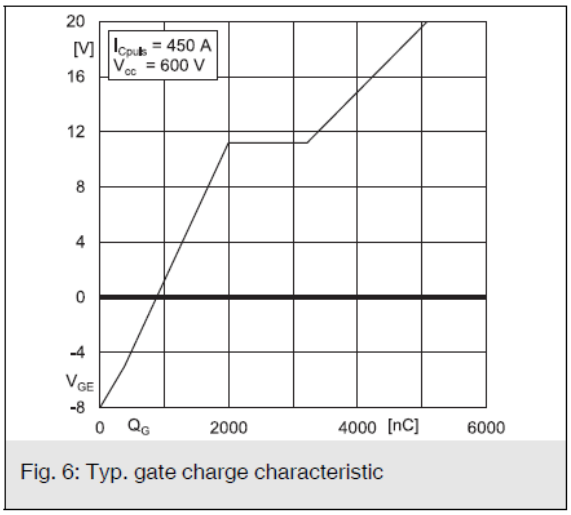


Fig. 6: Typ. gate charge characteristic

Figure 7.3.32 IGBT gate charge characteristic of an IGBT module SEMiX453GB12M7p

This diagram may be used to determine the required gate charge Q_G required to transduce the IGBT from off-state to saturation state; see explanations in 9.5.2.4.

Typical dependencies of the switching times $t_{d(on)}$, t_r, $t_{d(off)}$ and t_f on collector current I_C

Figure 7.3.33 illustrates the dependencies of the IGBT switching times $t_{d(on)}$ (turn-on delay time), t_r (rise time), $t_{d(off)}$ (turn-off delay time) and t_f (fall time) on the collector current I_C.
The measurement was carried out at the highest recommended operating temperature, a typical working voltage V_{CC} (e.g. 600V for 1200V or 900V for 1700V IGBT) and the driving conditions under which the typical switching energies are specified in the Table section of the datasheet.

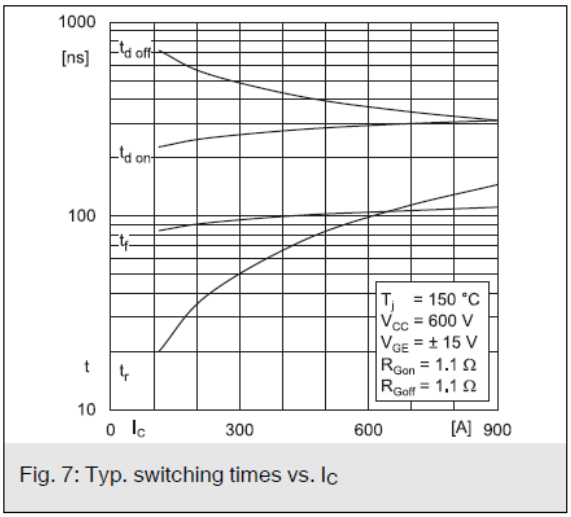


Fig. 7: Typ. switching times vs. I_C

Figure 7.3.33 IGBT switching times versus collector current of an IGBT module SEMiX453GB12M7p

Typical dependencies of the switching times $t_{d(on)}$, t_r, $t_{d(off)}$ and t_f on external gate resistance R_G

Figure 7.3.34 illustrates the dependencies of the switching times $t_{d(on)}$ (turn-on delay time), t_r (rise time), $t_{d(off)}$ (turn-off delay time) and t_f (fall time) on the external gate resistance R_G. The measurement was carried out at the highest recommended operating temperature at a typical supply voltage V_{CC} (e.g. 600V for 1200V or 900V for 1700V IGBT) and the nominal collector current I_{Cnom} as a function of the external gate series resistances R_G.

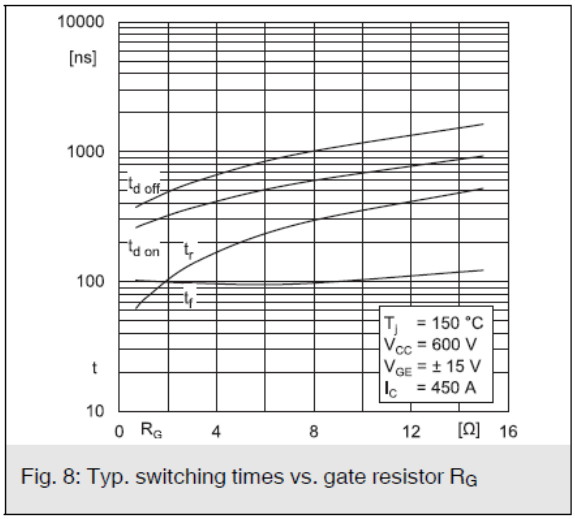


Fig. 8: Typ. switching times vs. gate resistor R_G

Figure 7.3.34 IGBT switching times versus gate resistance R_G of an IGBT module SEMiX453GB12M7p

Typical thermal impedances $Z_{th(j-c)}$ or $Z_{th(j-s)}$ of IGBT and inverse freewheeling diode

Figure 7.3.35 a) - using a logarithmic time scale - shows the thermal impedances $Z_{th(j-c)}$ between chip and baseplate for the IGBT- and diode switch of a case rated IGBT module SEMiX453GB12M7p in single-pulse operation as a function of the pulse duration t_p.
The diagram in Figure 7.3.35 b) shows the corresponding dependence of the thermal impedances $Z_{th(j-s)}$ between chip and heatsink for the IGBT- and diode switch of a heatsink rated MiniSKiiP IGBT module SKiiP24AC12T7V1 [7.47].

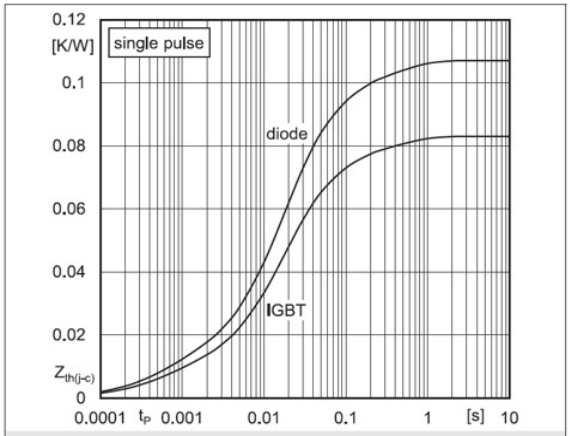


Fig. 9: Transient thermal impedance

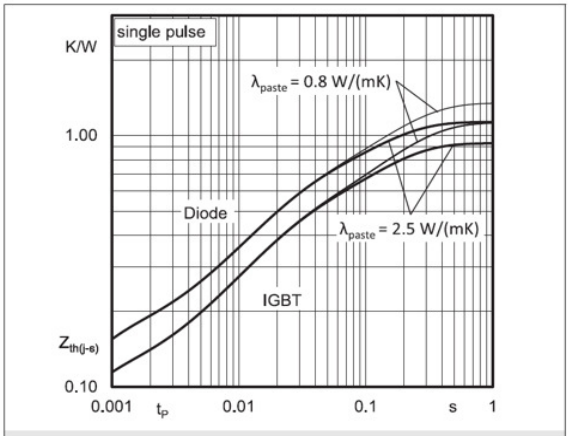


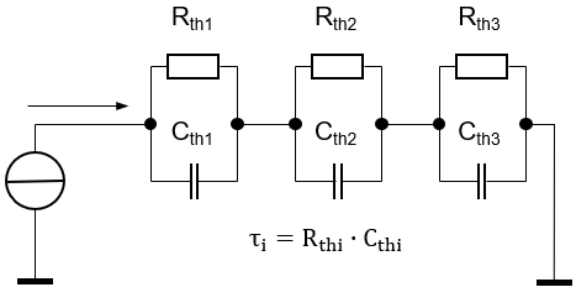
Fig. 9: Typ. transient thermal impedance

a) b)

Figure 7.3.35 Thermal impedances $Z_{th(j-c)}$ for IGBT and inverse diode of an IGBT baseplate module SEMiX453GB12M7p; b) Thermal impedances $Z_{th(j-s)}$ for IGBT and inverse diode of an IGBT module SKiiP24AC12T7V1 without baseplate

Some IGBT module datasheets contain separate diagram for IGBT and freewheeling diodes.
As Figure 7.3.35 b) shows, the $Z_{th(j-s)}$ of baseplate-less modules are dependent on the thermal conductivity λ of the thermal interface medium. After the junction temperature has a quasi-static value, $Z_{th(j-c)}$ resp. $Z_{th(j-s)}$ will reach their static end values $R_{th(j-c)}$ resp. $R_{th(j-s)}$, listed in the Table section of datasheet too.

Figure 7.3.36 shows a thermal equivalent circuit diagram with three time-constants $\tau_i = R_{thi} \cdot C_{thi}$ to describe the dynamic heat dissipation behaviour. The thermal impedances Z_{th} are indicated either numerically as parameters R_{thi} and τ_i of a thermal model or in the form of diagrams like Figure 7.3.35.



$$Z_{th} = \sum_{i=1}^{n} R_{thi} \cdot \left(1 - e^{\frac{t}{\tau_i}}\right)$$

Figure 7.3.36 Dynamic thermal model, where $\tau_i = R_{thi} \cdot C_{thi}$

IGBT Reverse Bias Safe Operating Area (RBSOA)

In the typical case of fast switching of ohmic-inductive load (hard switching applications), the IGBT Module has to reach a virtually rectangular characteristic i = f(v) between DC operating Voltage V_{CC} and load current I_L, expanded by the non-ideal properties of freewheeling diode, see example in Figure 7.3.37.
The datasheet-diagram in Figure 7.3.37 describes the permitted operating conditions at IGBT turn-off (RBSOA) at chip level (dashed line) and at the module terminal's level (continuous line).
Currently, such diagrams are only included in the datasheets of selected IGBT module families, e.g. SEMITRANS 10 and SEMITOP E or can be found in the technical explanations of the module family. The diagram is not included in the SEMiX453GB12M7p datasheet, for example.

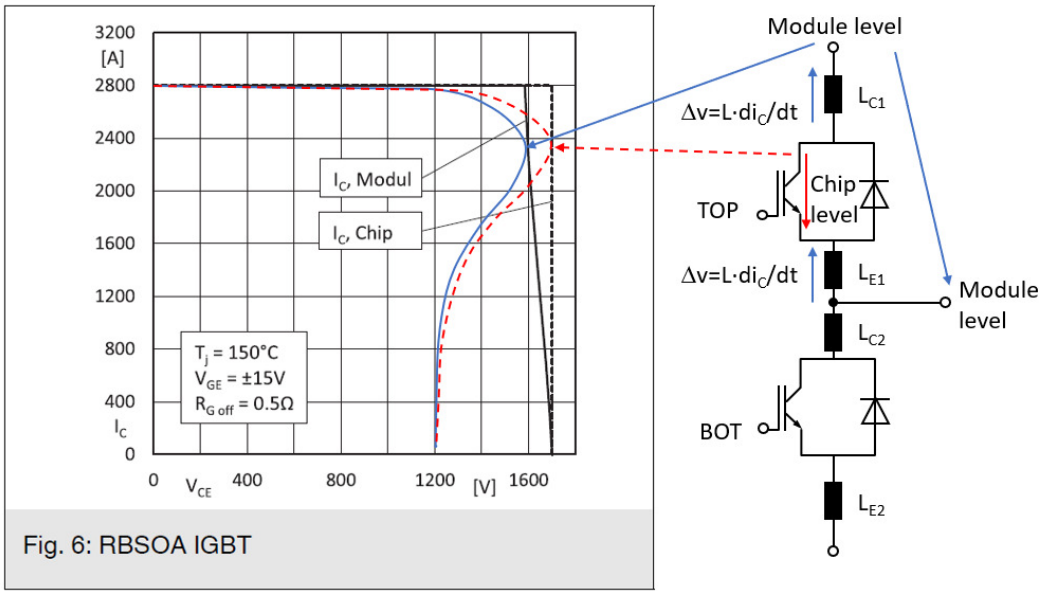
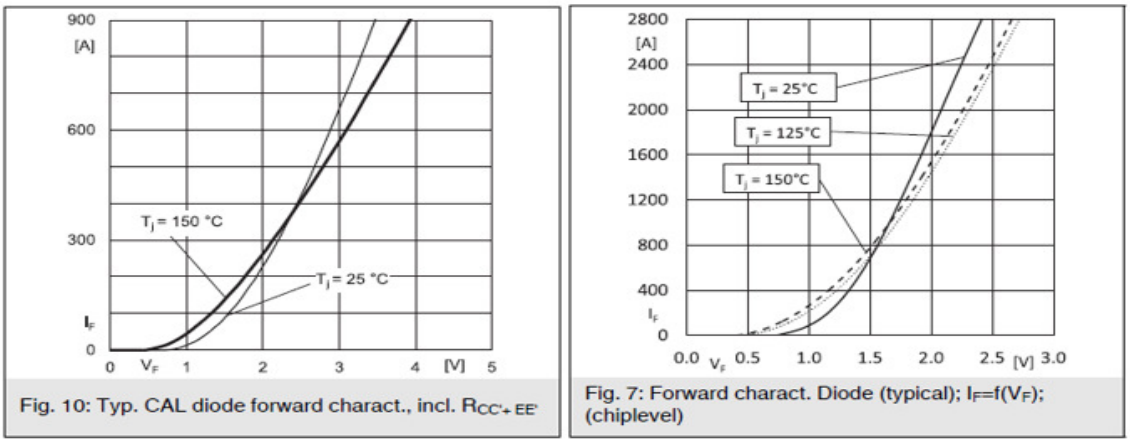


Figure 7.3.37 a) IGBT RBSOA of an 1700V IGBT module SKM1400GB17R8 with operating point curve at fast turn-off ohmic-inductive load; b) Equivalent IGBT module circuit diagram including parasitic inductances

Under the specified turn-off switching conditions (V_{GE}, R_G), the IGBT chips of SKM1400GB17R8 module can operate within its maximum collector-emitter voltage V_{CES} up to twice its nominal collector current I_{Cnom} if T_j = 150°C is not exceeded. Owing to the voltage induced at the parasitic module inductances L_{CE} during turn-off, the permitted collector-emitter voltage V_{CE} during turn-off decreases in dependence of the collector current, the turn-off speed and the permissible DC- link voltage V_{CC} is reduced for high currents.
Because this derating strongly depends on system related parameters, like stray inductance of the load circuit and the driver-dependent current commutation slope during the switching transitions, values of $\pm V_{GE}$ and R_{Goff} indicated in the RBSOA diagram. For these values, in the characteristic's tabular datasheet, the current commutation slope and the stray inductance L_s are listed.
Remark: For IGBT modules, it is no longer usual to specify the graphs SOA for single-pulse operation that was previously included in some datasheets or Technical Explanation. The SOA-graph referred to the limit values of V_{CES} (vertical limit) and I_{CRM} (horizontal limit). The minimum voltage limitation was defined by the IGBT output characteristics, but only during switching operation may IGBT modules touch the linear characteristic area.

Typical inverse diode forward characteristic $I_F = -I_C = f(V_F)$

Different reference options are used in different datasheets to illustrate the forward characteristic of inverse diode. Figure 7.3.38 a) shows the typical forward characteristics of an IGBT module integrated inverse diode at T_j = 25°C and 150°C. In contrast to the tabular data, the diagrams illustrate the voltage drop across the module terminals; the V_F value includes the voltage drops over the parasitic terminal resistances $R_{CC'+EE'}$.
Figure 7.3.38 b) shows the typical forward characteristics of an IGBT module integrated inverse diode at T_j = 25°C, 125°C and 150°C on chip level, i.e., without taking into account the voltage drops over the parasitic terminal resistances and according to the tabular information in the datasheet.



a) b)

Figure 7.3.38 Inverse diode forward characteristics of an IGBT module: a) SEMiX453GB12M7p (including the voltage drops over the parasitic terminal resistances $R_{CC'+EE'}$); b) SKM1400GB17R8 (on chip level)

The changing temperature coefficients of the forward voltage V_F from negative at low currents to positive at high currents can be seen in both diagrams.

Typical peak reverse recovery current I_{RR} of an inverse diode versus slope $-di_F/dt$ of the forward current I_F

Figure 7.3.39 shows typical ratings of the peak reverse recovery current I_{RRM} of the inverse diode at a typical operating point where the IGBT are under high load versus the diode forward current falling slope $-di_F/dt$ at diode turn-off. The turn-on speed of the commutating IGBT (di_C/dt) determines the $-di_F/dt$ of the diode in dependence of the IGBT external and internal gate series resistances R_{Gon} + R_{Gint}. For easy dimensioning, ratings for external R_G (R_{Gon}) of the IGBT are assigned to the di_F/dt values in this diagram. The I_{RRM} of the freewheeling diode increases in proportion to collector current and $-di_F/dt$.

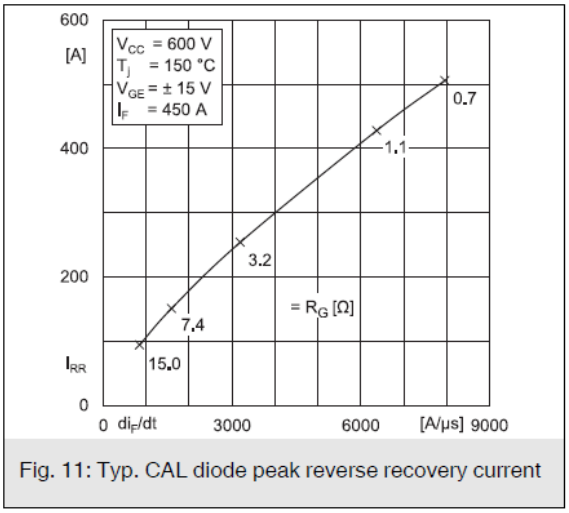


Fig. 11: Typ. CAL diode peak reverse recovery current

Figure 7.3.39 Peak reverse recovery current of the freewheeling diode (CAL diode) of an IGBT module SEMiX453GB12M7p

Typical recovered charge Q_{rr} of a freewheeling diode versus $-di_F/dt$ and forward current I_F before diode turn-off/IGBT turn-on

Figure 7.3.40 shows typical ratings of the recovered charge Q_{rr} at a typical operating point (e.g V_{CC} = 600V for 1200V IGBT or 990V for 1700V IGBT) where the IGBT are under high load versus diode forward current falling slope $-di_F/dt$ during diode turn-off and versus forward current I_F conducted before turn-off.
The diode forward current falling slope $-di_F/dt$ is determined by the turn-on speed of the commutating IGBT (di_C/dt), which depends on the IGBT gate series resistance R_G (R_{Gon}). For easy dimensioning, ratings for R_G (R_{Gon}) are assigned to the $-di_F/dt$ – values in this diagram.
The recovered charge of the freewheeling diode increases in proportion to the collector current and increases slightly as the $-di_F/dt$ increases.

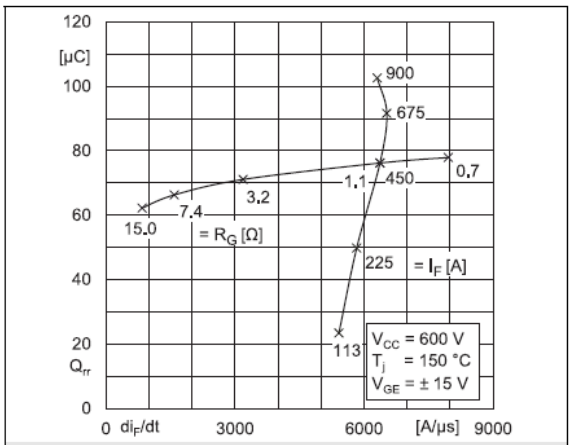


Fig. 12: Typ. CAL diode recovery charge

Figure 7.3.40 Recovered charge of freewheeling diode (CAL diode) of an IGBT module SEMiX453GB12M7p

In datasheets for hybrid SiC Modules with SiC Schottky barrier inverse diodes, all figures regarding the dynamical behaviour are omitted.

Inverse diode Reverse Bias Safe Operating Area (RBSOA)

The diagram in Figure 7.3.41 is included exclusively in the datasheets of selected high-power IGBT module platform e.g. SEMITRANS 10 and SEMITOP E2. The RBSOA diagram of an IGBT module-internal freewheeling diode describes the permissible limits of the turn-off power dissipation P_{rr} during current commutation on the complementary IGBT. Thus, in the current-voltage diagram, the permissible diode's operation is limited on the abscissa axis by the peak reverse voltage V_R and on

the ordinate axis by the maximum repetitive forward current I_{FRM}. The curved curve represents the maximum permissible power dissipation $p(t) = v_R(t) \cdot i_R(t)$ in the diode during a typical commutation cycle. For general explanations see also the descriptions according IGBT Reverse bias safe operating area above.

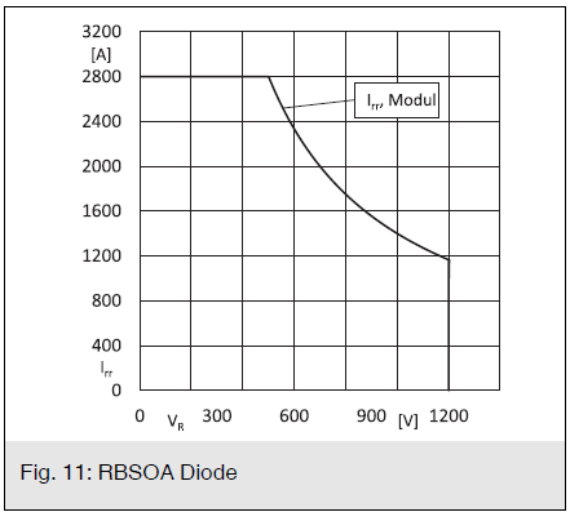


Figure 7.3.41 Freewheeling diode's RBSOA of an IGBT module SKM1400GB12P4

Built-in NTC characteristics

The diagram in Figure 7.3.42 is also included exclusively in the datasheets of selected IGBT module families, e.g. SEMITRANS 10. It illustrates the information, given in the characteristic data of datasheet Table "Temperature Sensor".

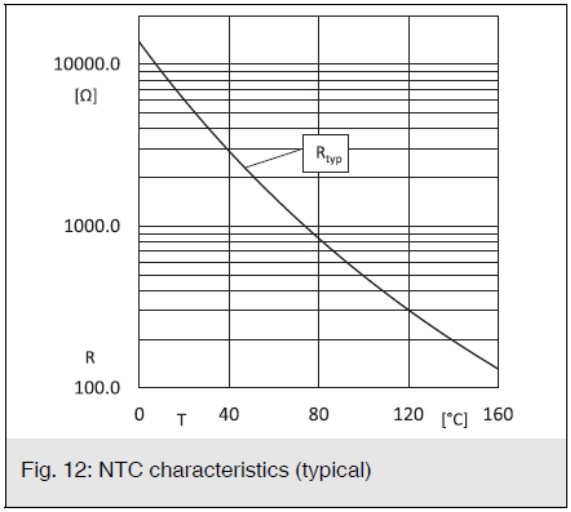


Figure 7.3.42 Typical NTC resistance characteristics vs. temperature of an IGBT module SKM1400GB17R8

7.3.5 Additional statements for 3-level power modules

As 3-level modules contain additional transistors and diodes with different data, these must also be characterised in the datasheets separately. The general information on the module given under "Features", "Typical Applications", "Remarks" and "Footnotes" in the shaded area to the left of the maximum ratings and characteristics contains important details on the semiconductors used and the numbering of the components in the datasheet in accordance with the circuit diagram which is also shown in Figure 7.3.43.

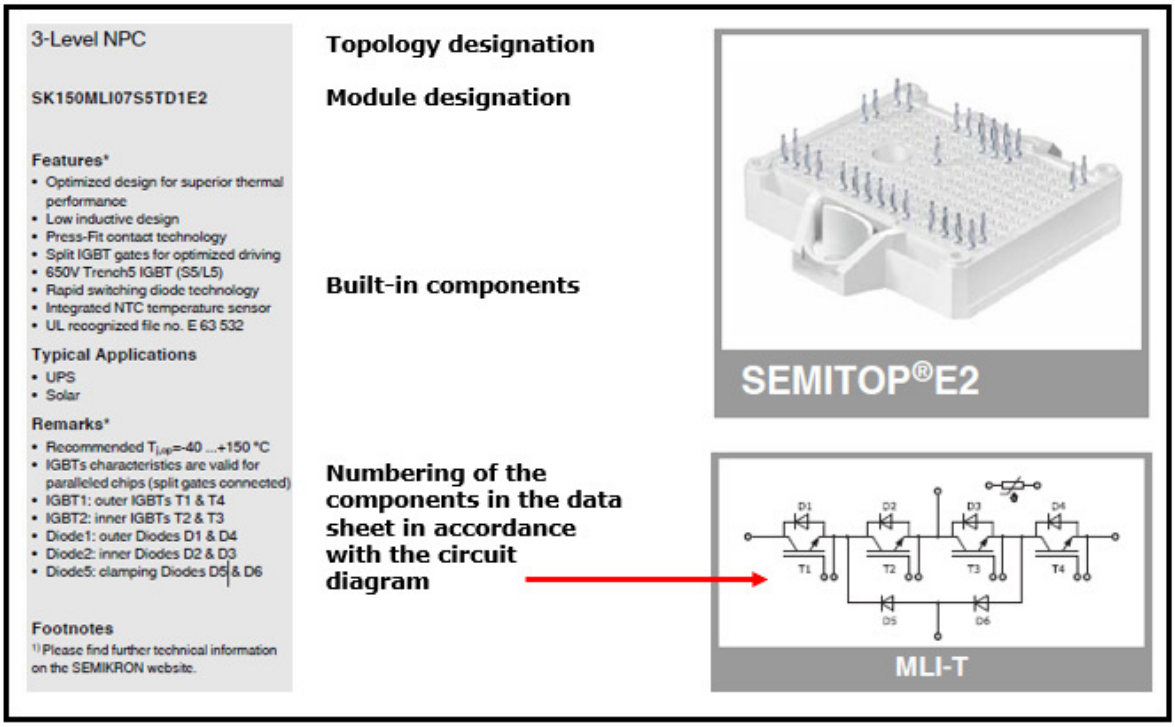


Figure 7.3.43 General information on a 3-level module

In principle, the datasheets for 3-Level modules follow the same structure as those for IGBT and SiC MOSFET modules, except that they contain some more data sets of the additional diodes and transistors.

7.4 Datasheet specifications for SKiiP® IPMs

7.4.1 SKiiP® high power IPM, topologies and type designation

In addition to the power semiconductors, IPMs (Intelligent Power Modules) also feature an integrated driver stage (complete or at least most of the driver circuit) with protective functions and sensors. SKiiP IPMs for high-power applications also include a cooling system, i.e., IGBT module and driver are joined in one unit which is mounted onto a heatsink. For this reason, IPM datasheets have additional data that is not included in other power module datasheets; this is because users do not have access to some IGBT- specific parameters.
The SKiiP IPM module product line covers the platforms SKiiP 3, SKiiP 4 and SKiiP 7. The Table 7.4.1 shows which IGBT chips are currently used in the various SKiiP series.

Voltage class	Shortcut	IGBT Chip series designation	SKiiP 3	SKiiP 4	SKiiP 7
	126	Infineon IGBT3 Standard Type	✔		
	12E4	Infineon IGBT4 Medium Power (M-Type)		✔	
	12M7	Mitsubishi Gen. 7 IGBT			✔
1200V	12E7	Infineon IGBT7			✔
	176	Infineon IGBT3 Standard Type	✔		
1700V	17E4	Infineon IGBT3 (shrink) Medium Power (M-Type)		✔	✔
Silicon Carbide MOSFET versions under development 2025					
	20IE1	Infineon CoolSiC™		✔	
2000V	20RM4	Rohm SiCMOS Trench Gen. 4		✔	

Table 7.4.1 Transistor chips used in the SKiiP series SKiiP 3/4/7

Currently projects for the optional integration of SiC chips in the SKiiP 4 series are in progress. The Table 7.4.2 shows the topologies of SKiiP IPM modules.

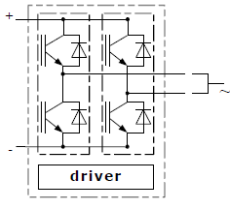
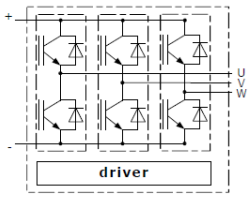
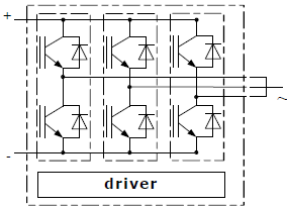
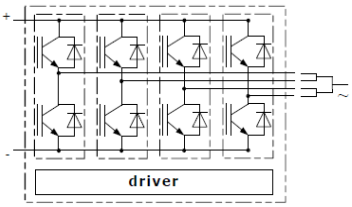
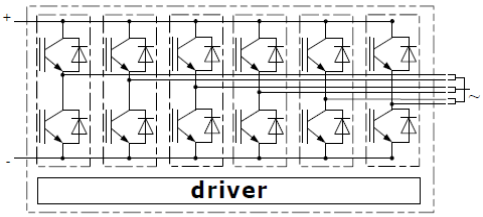
SKiiP 3	SKiiP 4	SKiiP 7	SKiiP® IPM Topology	
			2-fold GB Halfbridge	3-fold GD Sixpack
✔				
			3-fold GB Halfbridge	4-fold GB Halfbridge
✔	✔	✔		
			6-fold GB Halfbridge	
	✔	✔		

Table 7.4.2 Topologies of SKiiP IPM modules

Figure 7.4.1 and Figure 7.4.2 show the SKiiP housing images, alternatively available mounted on water- or forced air coolers.

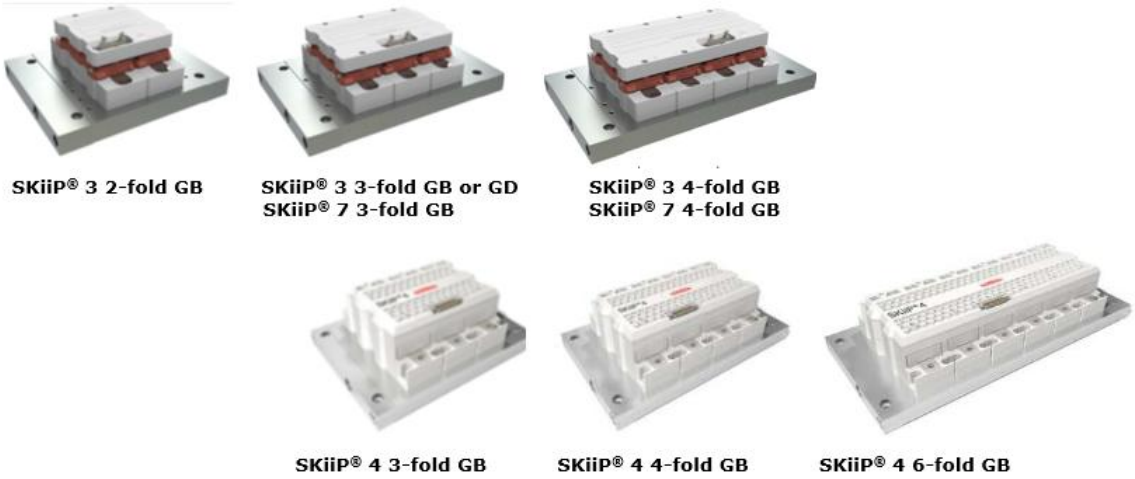


Figure 7.4.1 Housing images of SKiiP on watercooled standard heatsinks

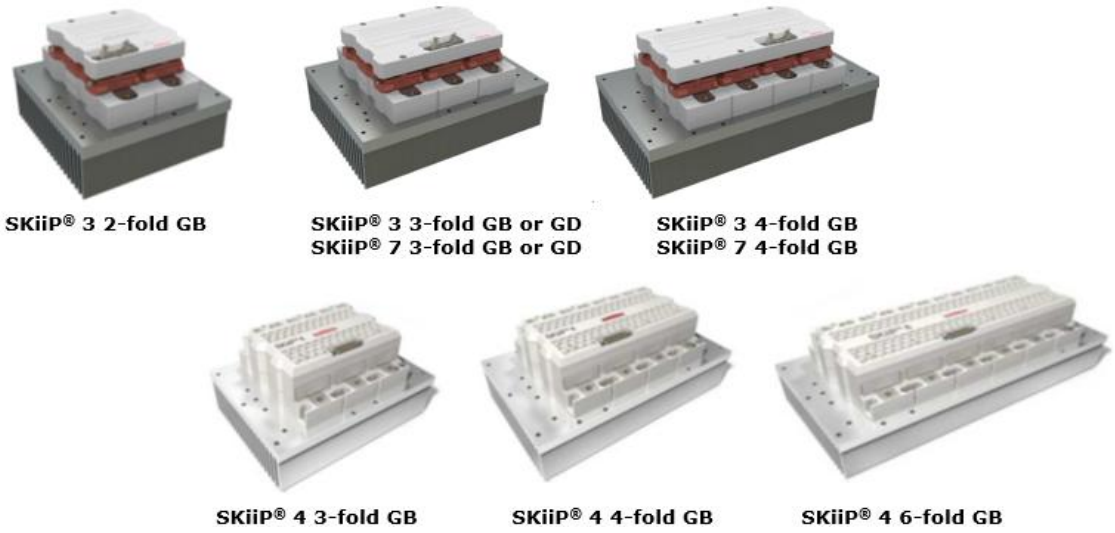


Figure 7.4.2 Housing images of SKiiP on aircooled standard heatsinks

The type designation code for SKiiP IPM modules is shown in Figure 7.4.3. Please refer to chapter 3.3 for further details.

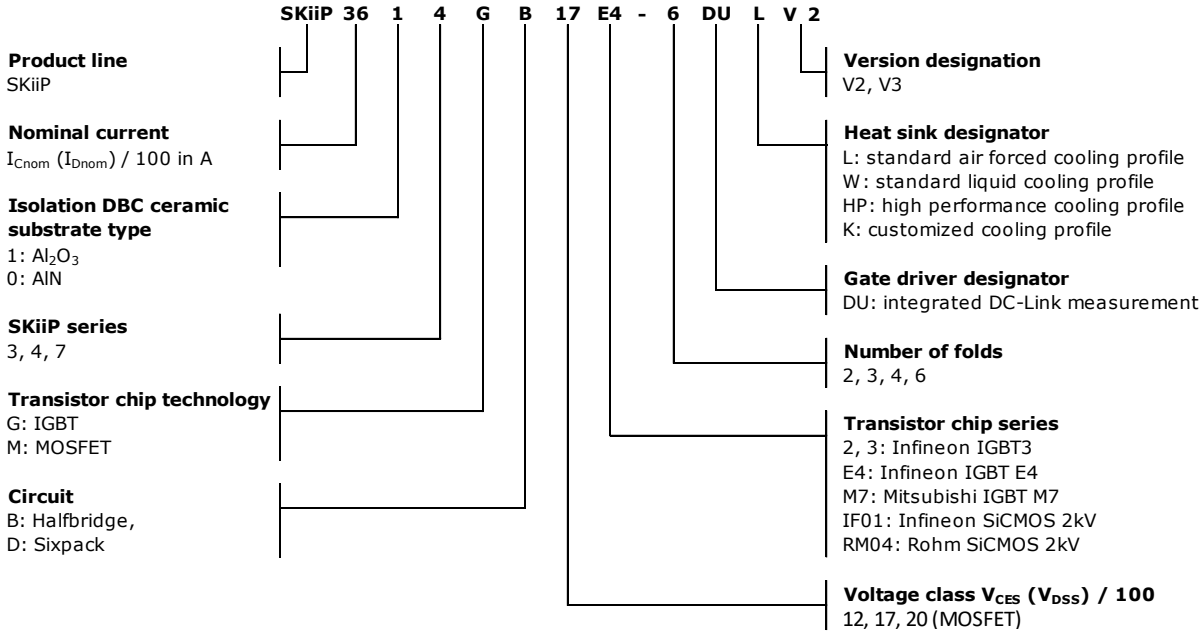


Figure 7.4.3 SKiiP type designation code

Essentially, SKiiP datasheets correspond to those of IGBT modules with respect to their content and tabular layout, although in the SKiiP datasheets some parameters which apply to sections not accessible to the user are omitted, whereas other additional system-specific parameters are included. The final page of the tabular part contains information on the realised insulation coordination (according to EN 60178 / IEC 61800-5-1) and the permissible environmental conditions according to the IEC 60721 standard.

7.4.2 Absolute maximum ratings

7.4.2.1 Maximum system ratings

Operating DC link supply voltage V_{CC}

Maximum permissible DC supply voltage applied between the DC terminals of a SKiiP module in operation; Parameter: Heatsink temperature T_s = 25°C. This maximum rating will be applicable provided that the DC terminals are connected to adequate high-frequency suitable (MKP) snubber

capacitors (for selection refer to SKiiP Technical Explanations [7.37] and the Application Note [7.48]).
If the DC and AC busbar system has a sufficiently minimal low-inductance design, the SKiiP module will be able to turn off short circuits within the rated DC supply voltage range without that V_{CES} is exceeded across the chips. Information on the key busbar system properties and design are also included in the Technical Explanations and the above-mentioned application note.
V_{CC} may be exceeded briefly only and up to a maximum value of V_{CES} even for blocked IGBT.

Insulation test voltage V_{isol}

DC value of the permissible test voltage between the short-circuited terminals and SKiiP heatsink with 1s test duration with each polarity; for details see chapter 10.3.5 and [7.19]. DC test is the preferred test method, because the large footprint of a SKiiP causes a large coupling capacitance to ground and with an AC test capacitive currents flow which cannot be distinguished for currents caused by an isolation failure,

RMS on-state current per terminal, $I_{t(RMS)}$

Maximum current load applied to the power terminals of a half-bridge (fold) I_{AC}-terminal, which corresponds to $I_{t(RMS)}$ of an IGBT module. Since the terminal temperature affects the operating temperature of the SKiiP 3 gate driver. In the SKiiP 3 datasheets the maximum terminal temperature $T_{terminal}$ (< 115°C) is also given as a parameter.

Maximum peak current of power section $I_{max(peak)}$ (only listed in SKiiP 4 datasheets)

Highest current per SKiiP that the AC current sensors can display in total. Its value is relevant for measurement of current, and corresponds to the overcurrent trip level.

Surge forward current I_{FSM} of inverse diodes and peak load integral I^2t

If the inverse diodes are used as line rectifiers, their non-repetitive short-time overload capability is definitive for the choice of protective circuits. As is the case with conventional rectifier diodes, the surge forward current I_{FSM} is the forward current surge peak in the form of a 50Hz sinusoidal half wave which the diode is able to withstand without being damaged in the event of a malfunction (short circuit), provided this is does not occur too often during the diode lifetime. If a rectifier diode is exposed to surge forward current load, the junction temperature may temporarily rise to as much as 400°C. Therefore, should a reverse voltage occur immediately after a diode has been exposed to surge current load, the permissible surge forward current peak will be lower than if no subsequent reverse voltage is involved. For further details please refer to chapter 7.3.2.2.

Fundamental frequency of the output current f_{out}

Maximum permissible fundamental frequency of sinusoidal output current at T_s = 25°C, limited by the properties of the integrated SKiiP current sensors and their evaluation electronics.
This rating is applicable to the pulse frequency f_{sw} with PWM, provided that the amplitude $I_{peak(1)}$ of the current sensor's first harmonic does not exceed the rated current I_{Cnom}. The amplitude for a rectangular signal may be calculated as follows:

$$I_{peak(1)} = \frac{\pi}{\sqrt{3}} \cdot \frac{I_{RMS}}{\sqrt{2}}$$

In addition, it has to be taken into account that the *RMS on-state current per terminal, $I_{t(RMS)}$* is limited and that the maximum permissible collector current I_C is temperature-dependent.

Storage temperature range T_{stg}; T_{stgmin}...T_{stgmax}

Temperature range within which the module may be stored or transported without being subject to electrical load. The maximum storage temperature is also the maximum permissible housing temperature for SKiiP IPM modules in application.

7.4.2.2 Maximum ratings of the SKiiP IGBT

Collector-emitter voltage V_{CES}

Maximum permissible voltage between the collector and emitter terminals of the IGBT chips with gate-emitter short circuited at junction temperature T_j = 25°C. The V_{CES} increases in proportion to the temperature owing to the temperature dependency of the breakdown voltage. Irrespective of the load conditions, the sum of the collector-emitter supply voltage V_{CC} and the switching

overvoltage $\Delta V_{CE} = L_\sigma \cdot di_C/dt$ must not exceed voltage V_{CES} (L_σ: sum of the parasitic inductances in the commutation circuit).

Continuous collector current I_C

Maximum permissible continuous direct current over the collector output at which the permissible maximum junction temperature with heatsink temperature T_s = 25°C / 70°C. Since I_C designates a static maximum value, it is not relevant to switching operation.

Nominal collector current I_{Cnom}

Rated current of IGBT chips indicated in the chip manufacturer's datasheet multiplied by the number of IGBT chips per switch connected in parallel in the module.
For SKiiP IPM modules, I_{Cnom} is the naming current, i.e., the current encoded in the module's type designation.

Junction temperature range T_j; $T_{j(min)}$...$T_{j(max)}$

Permissible chip temperature range $T_{j(min)}$ to $T_{j(max)}$. For continuous operation the maximum chip temperature $T_{j(op)}$ should be kept at least 25K below $T_{j(max)}$.

7.4.2.3 Maximum ratings of the SKiiP freewheeling diodes

Repetitive peak reverse voltage V_{RRM}

Maximum permissible values for repetitive transient peak voltages in the reverse blocking state of the inverse diode at T_j = 25°C…T_{jmax}. Please note that V_{RRM} is lower at very low temperatures.

Inverse diode forward current I_F

Maximum permissible direct reverse collector current at maximum permissible junction temperature T_{jmax} for heatsink temperature T_s = 25°C / 70°C.

Nominal diode current I_{Fnom}

Rated current of the diode chips used as indicated in the chip manufacturer's datasheet, e.g., for CAL diodes "Nominal diode I_F rating, verified by design and characterisation”, multiplied by the number of diode chips connected in parallel in the module per switch.

Junction temperature range T_j; $T_{j(min)}$...$T_{j(max)}$

Permissible chip temperature range $T_{j(min)}$ to $T_{j(max)}$. For continuous operation the maximum chip temperature $T_{j(op)}$ should be kept at least 25K below $T_{j(max)}$.

7.4.2.4 Maximum ratings of the SKiiP gate driver

Driver supply voltage V_s

The SKiiP 3 gate driver features a wide-range power supply for primary voltages between 13V and 30V. The input voltage rating for the SKiiP 4 gate driver supply voltage is 19.2V to 28.8V (24V±20%).

Input signal voltage (HIGH) V_{iH}

The maximum input signal voltage is derived from the high-level specification of the driver logic used to form the input signal.

Insulation test voltage V_{isolPD} (only listed in SKiiP 3 datasheets)

Effective value of the permissible test voltage (50 Hz AC voltage) between the short circuited driver input and the power terminals; parameters: test duration, e.g., t = 2s.: maximum partial discharge $Q_{PD} \leq 10pC$.

Rate of rise of voltage on the secondary side dv/dt

Maximum rate of rise of voltage on the secondary side (power side) during IGBT switching under which the driver can still operate uninhibited.

Switching frequency f_{sw}

Maximum permissible PWM frequency limited by the gate drivers’ maximum average output current and the power dissipation of driver, power semiconductors and AC current sensors and ambient/heatsink temperature (datasheet rating at T_s = 25°C).

In case of higher ambient temperature, the derating of the switching frequency must be considered for 2-fold and 3-fold SKiiP 3 GB-types as well as GD-type. Diagrams are shown in chapter 3.3.4.5, Figure 3.3.11).
At SKiiP 3 and SKiiP 7, no error signal will be set if the maximal allowed switching frequency for the particular SKiiP will be exceeded. It is the user's responsibility to limit the frequency according to the datasheet given maximum ratings.
All SKiiP 4 gate drivers are equipped with a protection function against exceeding the maximum permissible switching frequency f_{sw}. In order to prevent the module against overheating, the switching signal inputs HB_TOP and HB_BOT are monitored with respect to oscillations.

7.4.3 Characteristics

7.4.3.1 Characteristic ratings of the SKiiP IGBT

Collector-emitter saturation voltage $V_{CE(sat)}$

IGBT saturation voltage measured at the power terminals of a SKiiP module, i.e.
voltage drops across the internal module resistances $R_{CC'+EE'}$ (bond wires, terminals, …) are also included in $V_{CE(sat)}$). Parameter: I_C, T_j = 25°C / T_{jmax} – 25K.

Collector-emitter threshold voltage V_{CE0} and on-state slope resistance r_{CE} of the forward characteristic approximation

To calculate the forward losses, the elements of an equivalent straight line are given in the datasheets as

$$V_{CE(sat)} = f(I_C) = V_{CE0} + r_{CE} \cdot I_C$$

Figure 7.3.17 gives a definition of V_{CE0} and $r_{CE.}$ By analogy with $V_{CE(sat)}$, r_{CE} is calculated across the internal module resistances $R_{CC'+EE'}$ (bond wires, terminals, …).

Switching energy E_{on} + E_{off}

The sum of turn-on and turn-off energies E_{on} + E_{off} is given at T_j = T_{jmax} – 25K for two typical SKiiP operating points.

Thermal resistances $R_{th(j-s)}$ and $R_{th(j-r)}$ per IGBT switch

Thermal resistances between IGBT chips and sink respective temperature sensor per switch, irrespective of the number of IGBT chips connected in parallel.
Figure 7.4.4 describes the thermal model of baseplate-less IGBT modules. Due to the power losses generated inside the module by the IGBT and the diodes, all of the chips are heated to

$$T_j = T_a + P_T \cdot (R_{th(j-s)} + R_{th(s-a)})$$

Because the temperature T_r of an integrated temperature sensor is referred to in the datasheet, it has to be taken into account that the sensor temperature lies between chip temperature T_j and heatsink temperature T_s, respectively.

$$T_j = T_a + P_T \cdot (R_{th(j-r)} + R_{th(r-a)})$$

The thermal model must be adapted similar to Figure 7.4.4. It should be noted that the placement of the temperature sensor differs between SKiiP 3/SKiiP 7 and SKiiP 4. This affects the thermal coupling between chips and temperature sensor and thus also the ratio of sensor temperature to chip temperature and heatsink temperature.

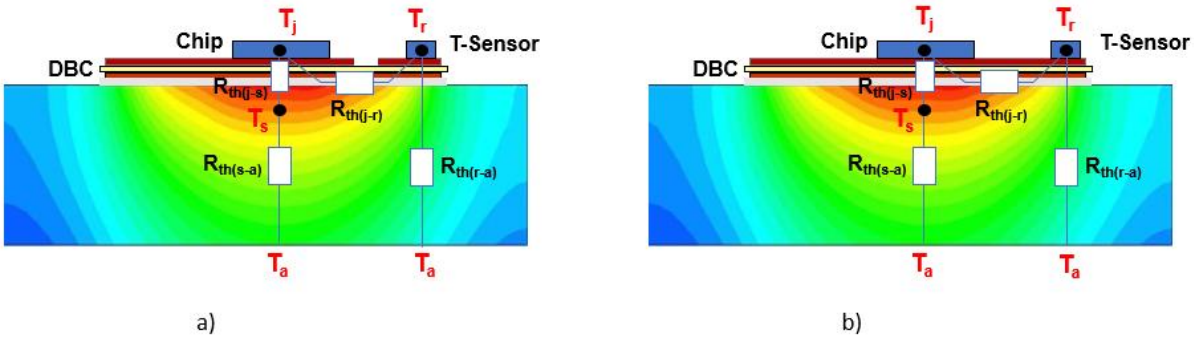


Figure 7.4.4 SKiiP 3/SKiiP 7 – SKiiP 4 Differences of thermal coupling between IGBT/diode chips and temperature sensor: a) SKiiP 3/SKiiP 7: Isolation gap between IGBT/diode Chips and temperature sensor chip; b) SKiiP 4: no isolation gap between IGBT/diode Chips and temperature sensor chip

7.4.3.2 Characteristic ratings of the freewheeling diodes

Forward voltage $V_F = V_{EC}$ of an inverse diode

Collector-emitter voltage drop in reverse direction at specified forward current I_F value at I_{Cnom} for chip temperatures T_j = 25°C / T_{jmax} – 25K). The rating refers to the saturation voltage measured at the power terminals of a SKiiP module, i.e. voltage drops across the internal module resistances $R_{CC'+EE'}$ (bond wires, terminals, …) are also included. Parameters: I_C, T_j = 25°C / T_{jmax} – 25K.

Threshold voltage V_{F0} and forward slope resistance r_F of an inverse diode

Forward voltage $V_F = V_{EC}$ of an inverse diode, Collector-emitter voltage drop in reverse direction at V_{GE} = 0V; forward current I_F value at a specified current for chip temperatures T_j = 25°C / T_{jmax}-25K. The rating refers to the forward voltage measured at the power terminals of a SkiiP module, i.e., voltage drops across the internal module resistances $R_{CC'+EE'}$ are included.

Turn-off Energy E_{rr}

Turn-off energy of an inverse diode at T_{jmax} – 25K at inverse diode switchover from forward current I_F value at I_{Cnom} to reverse state. E_{rr} is given for two typical SKiiP operating points The switching losses P_{off} of the inverse diodes during freewheeling operation can be determined by multiplying energy E_{rr} and switching frequency f_{sw}.

Thermal Resistances $R_{th(j-s)}$ and $R_{th(j-r)}$ per diode switch

The explanations given for the characteristic "Thermal resistances $R_{th(j-s)}$ and $R_{th(j-r)}$ per IGBT switch" also apply to inverse diodes, provided the "IGBT" is replaced by "inverse diode" and P_T is replaced by P_D.

7.4.3.3 Characteristic ratings of the SKiiP gate driver

Range of non-stabilised supply voltage V_s

For all SkiiP series, the nominal non-stabilised supply voltage is 24V. As already mentioned in the limit values, SKiiP 3/SKiiP 7 and SKiiP 4 have different permissible input voltage ranges: The SKiiP 3 gate driver features a wide-range power supply for primary voltages between 13V and 30V. The input voltage rating for the SKiiP 4 gate driver supply voltage is 19.2V to 28.8V. For all SKiiP, the external power supply must ensure that the voltage at the interface of the SKiiP rises continuously and fast (rise time lower than 2s) and without any plateau formation.

Supply bias current I_{S0}

Standby current consumption of the gate driver, given at nominal supply voltage, no switching, no AC output current.

Input current in operation I_S

The data sheets contain the following formula and the SKiiP-type specific k-values for calculating the supply current required during operation, assuming a supply voltage of 24V and a 50Hz, sinusoidal AC output current:

$$I_S = I_{S0} + k_1 \cdot f_{sw} + k_2 \cdot I_{AC}^2$$

I_{S0} - current consumption during standby, No switching signals are applied, no AC-current is flowing.
$k_1 \cdot f_{sw}$ - current consumption of the driver in switching mode
$k_2 \cdot I_{AC}^2$ - current consumption required by the integrated current sensor to compensate the actual value of I_{AC}.

It is recommended to choose a power supply with a rated current at least 50% higher than the maximum driver input current datasheet rating I_S.

Input threshold voltage (HIGH) V_{IT+}, Input threshold voltage (LOW) V_{IT-}

The switching signal inputs TOP IN for the TOP and BOT IN for the BOT IGBT have a digital positive /active high logic (input HIGH = IGBT on; input LOW = IGBT off) characteristic. A non-connected input will be considered as LOW signal.
Minimum threshold voltage that guarantees that input voltage level is recognized to switch on the IGBT. Maximum threshold that guarantees that input voltage level is recognized to switch off the IGBT (Figure 7.4.5). For SKiiP 3/SKiiP 7, V_{IT+} and V_{IT-} are fixed values, for SKiiP 4 the values are related to the supply voltage V_s.

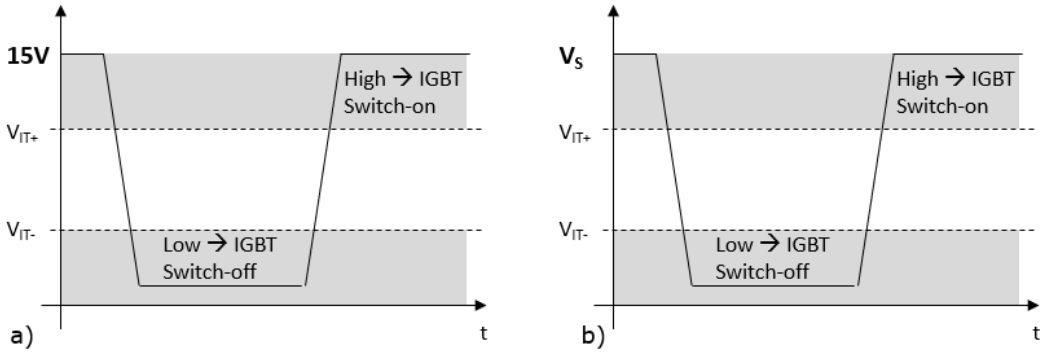


Figure 7.4.5 Input voltage thresholds of SKiiP 3/SKiiP 7 (a) and SKiiP 4 (b)

For driving the signal inputs, it is mandatory to use line drivers with a push-pull characteristic. Pull up and open collector output stages must not be used for driving these inputs.

Input resistance R_{IN} / Input capacitance C_{IN}

Driver input properties at T_a = 25°C: The input resistance R_{IN} is about 10kΩ at SKiiP 3/SKiiP 7 and about 13kΩ at SKiiP 4. For all SKiiP the input capacitance C_{IN} is 1nF, to obtain high noise immunity (Figure 7.4.6). This capacitor can cause a delay of few ns for current limited line drivers, which can be neglected.

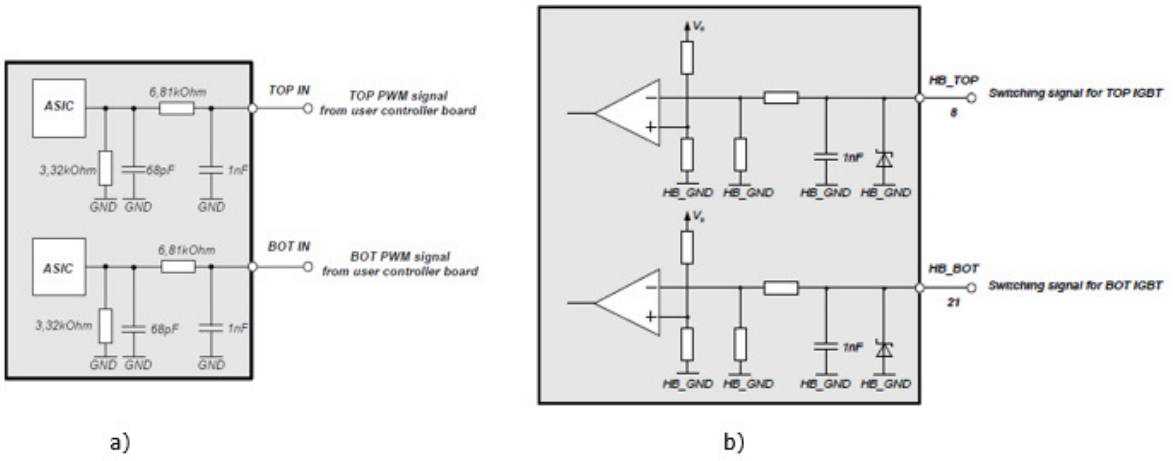


Figure 7.4.6 TOP/BOT signal input topologies of SKiiP 3/SKiiP 7 (a) and SKiiP 4 (b)

Error memory reset time t_{pReset}

In case of an error caused by

- Undervoltage of the primary side
- Undervoltage of the secondary side (only at SKiiP 3/SKiiP 7)
- Exceeding the maximum switching frequency (only at SKiiP 4)
- Overlapping of TOP/BOT switching signals (only at SKiiP 4)
- SKiiP internal bridge short circuit
- Load overcurrent (OCP)
- Exceeding the maximum DBC-sensor temperature
- Exceeding the maximum driver PCB temperature (only at SKiiP 4)
- DC link overvoltage (only at SKiiP 4 and SKiiP 3/SKiiP 7 with option U)
- Internal driver error (only at SKiiP 4),

the gate driver acts as follows (Table 7.4.3).

SKiiP 3/SKiiP 7 Gate driver	**SKiiP 4 Gate driver**
sets the ERROR output to HIGH state (not ready to operate)	sets the HALT output to LOW state (not ready to operate)
The IGBT will be turned-off and switching pulses from the controller won't be transferred to the output stage.	
During this time the driver will check if the switching input signals are set to LOW.	
If this is the case and no error is present anymore the driver will release the ERROR signal.	If this is the case and no error is present anymore the driver will release the HALT signal.
If the input signals have not been switched to LOW state the driver will pull the ERROR signal to HIGH as long as the switching input signals are not LOW	If the input signals have not been switched to LOW state the driver will pull the HALT signal to LOW as long as the switching input signals are not LOW
In case of error the switching input signals must be LOW within t_{pRESET} to continue with switching again when error is removed.	

Table 7.4.3 Gate driver processing at detected errors

If the SKiiP 7 has entered the error state, it must be reset before the driver resumes to operation mode. The driver could be reset under the following conditions:

- >30µs non-error condition (reaction on controller side should happen within that time)
- >9µs no input signals at TOP IN/BOT IN (controller confirms error)

After completing the reset sequence, the driver returns "ready for operation" by setting the error output to high-level.

Overcurrent reset time $t_{pReset(OCP)}$ (only relevant for SKiiP 4 with FRT-function)

With FRT function activated via the CANbus interface, the period $t_{pReset(OCP)}$ of 200µs - starting when the rotor current is dropped below I_{TRIPSC} and the control signals are blocked by the customer - the SKiiP 4 driver enables the switching signals again as long as I_{TRIPSC} is not exceeded again. For further details please refer to chapter 3.3.4.6 SKiiP 4 FRT (Fault Ride Through) – function.

Top / bottom switch interlock time t_{TD}

A deadtime circuit prevents that TOP and BOT IGBT of one halfbridge are switched on simultaneously. The internal interlock time is adapted to the IGBT, i.e., is chosen as small as possible to allow high duty cycle but guarantees a safety margin against shoot through losses. The interlock time is not added to a deadtime provided by the controller, see Figure 7.4.7.
It is allowed to control SKiiP by inverted pulses, e.g., without controller generated deadtime but it is not allowed, that TOP and BOT IGBT of a halfbridge are turned-on at the same time. Such an overlapping condition is observed and in case it persists for minimum 3µs all IGBT are turned-off. After the overlapping situation has ended and the interlock time has elapsed the IGBT with the valid on-signal will be turned-on.

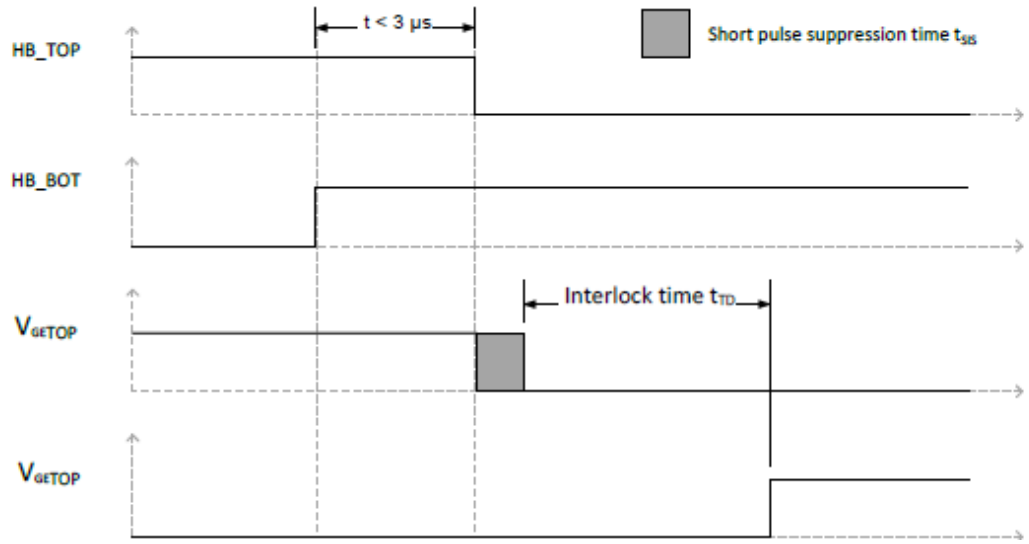


Figure 7.4.7 SKiiP 4 interlock time and short pulse suppression [3.20]

Power-On-Reset time t_{POR} (exclusively specified in SKiiP 4 datasheets)

The jitter clock time is the maximum deviation of the switching signal propagation delay time at constant environmental conditions, see chapter 9.5.4.2. It is caused by the processing of signals with an internal clock frequency and is randomly distributed between 0 and maximum value. The jitter clock time is significant for the parallel connection of SKiiP IPM modules, see chapter 9.3.7.2.

Short pulse suppression time t_{SIS}

This function suppresses short turn-on and off-pulses at the signal input pins. In this way the IGBT are protected against noise which can occur due to burst on the signal lines. If a pulse is shorter than t_{SIS}, it will be suppressed, the other channel remains on (see example of SKiiP 3 behaviour, Figure 7.4.8). No error signal will be issued.
The short pulse suppression time is included in the drivers input-output turn-on and turn-off propagation times $t_{d(on)IO}$ and $t_{d(off)IO}$.

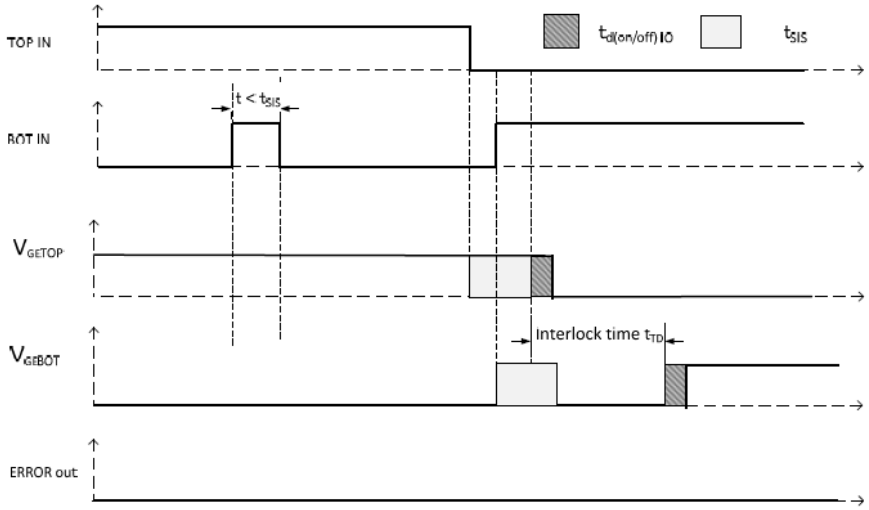


Figure 7.4.8 SKiiP 3 short pulse suppression behaviour at input pulse duration $t_{pulse} < t_{sis}$ [7.36]

Power-On-Reset time t_{POR} (exclusively specified in SKiiP 4 datasheets)

The driver board processes a Power-On-Reset after turning on the supply voltage. At SKiiP 3/SKiiP 7 The Power-On-Reset is completed after the supply voltage will reach the level of 13V and its time duration t_{POR} can be up to 150ms.
After ERROR output will be reset (typ. 8ms) no error will be signalized during the remaining time of power on rese. To assure a high level of system safety the high and low side signal inputs should stay in a defined OFF-state during driver turn-on time. Only after the end of the power on reset, the IGBT operation is permitted.

At SKiiP 4, during t_{POR} the HALT signal is set to LOW and the IGBT remain blocked. Without any error being present, the HALT signal will be released after the Power-On-Reset is completed (Figure 7.4.9).

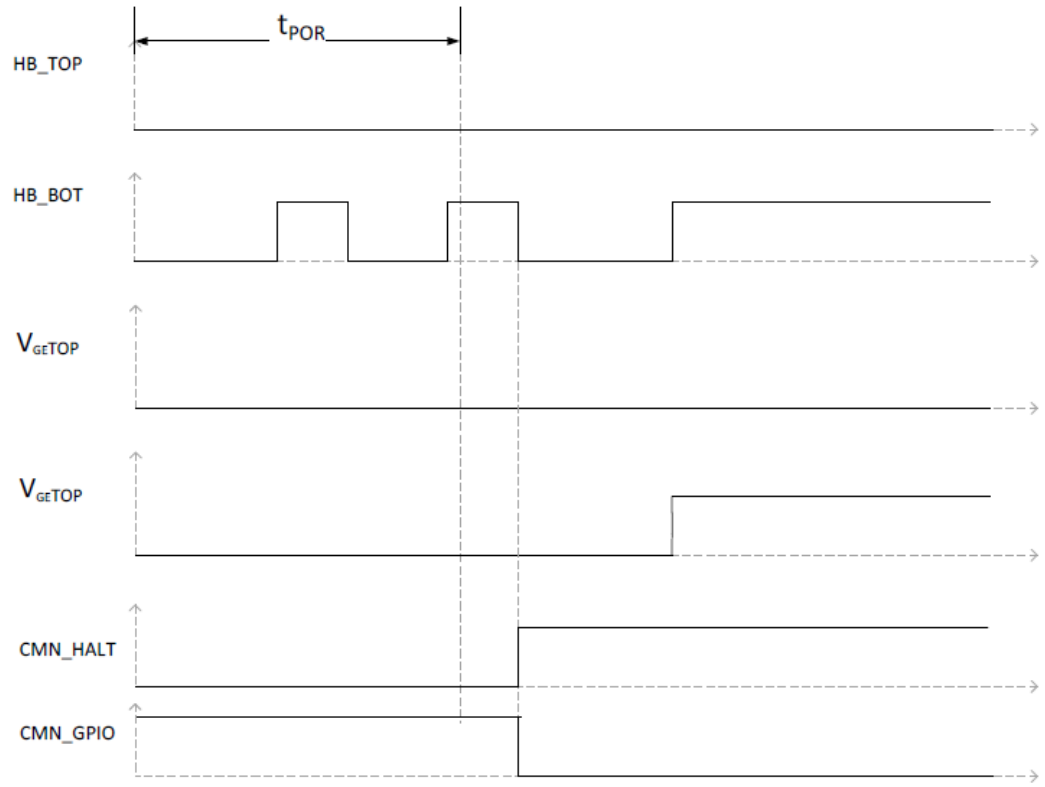


Figure 7.4.9 SKiiP 4 power-on-reset timing diagram [7.37]

Digital output sink current $I_{digiout}$ (HALT-signal, only SKiiP 4)

Maximum permissible output current from driver connector, pin 13 (CMN_HALT)

HALT input threshold voltages Vit+ (LOW-HIGH) and Vit- (HIGH-LOW), (only SKiiP 4)

Minimum threshold voltage V_{it+} at pin 13 that guarantees that input voltage level is recognized to set the HALT signal from LOW to HIGH state and maximum threshold voltage V_{it-} at pin 13 that guarantees that input voltage level is recognized to set the HALT signal from HIGH to LOW state.

Error delay time $t_{d(err)}$ (only SKiiP 4)

The error delay time is the propagation delay time of an error (from detection to HALT). This time is different for the different types of errors. The precise values for each specific error type are summarized in Table 7.4.4.

Type of error	Typical error delay time [µs]
DC-Link overvoltage	160
Overcurrent protection (OCP-error)	2
Short circuit protection (SCP) by V_{CEsat} monitoring	3
DBC-sensor overtemperature	6000 (except special SKiiP types)
Exceeding maximum switching frequency	6

Table 7.4.4 SKiiP 4 error delay times for various error types

Overcurrent trip level I_{TRIPSC}

Among other protective functions, SKiiP offers overcurrent protection (OCP) as soon as the integrated current sensors detect an AC output current above a trip level of 125% of the rated $I_{analogOUT}$. Irrespective of the SKiiP version, the OCP trip level thus corresponds to a voltage of 10V applied at the $I_{analogOUT}$ terminal. For SKiiP modules with identical chip sets and different DBC substrates Al_2O_3 or AlN), it is therefore identical. As soon as the trip level is reached, the error

memory will be set with the ERROR output switched to HIGH (SKiiP 3/SKiiP 7) respective the HALT output to LOW (SKiiP 4) and the IGBT turned off. The error memory is not reset until no further internal error signals are detected and both control signals have been set to LOW for at least $t_{pERRRESET}$, or until power-on reset occurs.

Overtemperature trip level T_{trip}

The temperature T_r, which is approximately equal to the heatsink temperature, is detected by the temperature sensor integrated in the SKiiP module. As soon as T_r reaches the level of T_{trip} indicated in the datasheets, the error memory will be set with the ERROR output switched to HIGH (SKiiP 3/SKiiP 7) respective the HALT output to LOW (SKiiP 4) and the IGBT is turned off. The output OVERTEMP OUT, which is only available on SKiiP 3/SKiiP 7, is also set from LOW to HIGH.
The error memory is not reset until no further internal error signals are detected and both control signals have been set to LOW for at least $t_{pERRRESET}$, or until power-on reset occurs.
Since T_{trip} is not much lower than the maximum permissible chip temperature, a safe thermal protection is not always guaranteed by the internal overtemperature protection alone in highly efficient cooling systems.

PCB Overtemperature trip level $T_{DriverTrip}$ (only SKiiP 4)

Although the gate drive circuit can operate at ambient temperatures of up to T_a = 85°C, it is recommended that the average ambient temperature of the driver board usually does not exceed 40°C. The actual temperature of the gate driver T_{Driver} is measured by means of a temperature sensor located at the bottom side of the driver PCB (see Figure 7.15 in [7.37][3.20]). The value of the sensor could be read out via CAN-bus interface. Please refer to the CANopen documentations [7.49], [7.50] for further information). If the temperature exceeds the $T_{DriverTrip}$ value the switching operation will be blocked and a HALT signal will be issued correspondingly. If necessary, the trip level of the temperature sensor can be adjusted to a lower level by the CANbus interface.

Overvoltage trip level V_{DCtrip}

An overvoltage protection is coupled with DC link voltage monitoring, implemented in all SKiiP 3/SKiiP 7 GD sixpacks types, all SKiiP 4 types and optionally available for SKiiP 3/SKiiP 7 GB halfbridge types except for SKiiP 3 2GB. As soon as the DC link voltage passes the trip levels listed in Table 7.4.5 the error memory will be set, the ERROR OUT output switched to HIGH (SKiiP 3/SKiiP 7) respective the HALT output to LOW (SKiiP 4) and the IGBT turned off.

V_{CES}	1200V	1700V
SKiiP 3	900V ± 4%	1200V ± 4%
SKiiP 4	980V ± 3%	1340V ± 3%
SKiiP 7	930V ± 4%	1200V ± 4%

Table 7.4.5 DC overvoltage trip levels

The error memory is reset if no further internal error signals are detected and both control signals have been set to LOW for at least $t_{pERRRESET}$, or until power-on reset occurs.
A low-pass filter provides interference suppression for a time constant of 500µs. This monitoring function is therefore not suitable for detecting extreme voltage jumps. At SKiiP 4, the overvoltage trip level V_{DCtrip}, can be deactivated via CAN interface, see [7.49] and [7.50] for further information.

Input-output turn-on and turn-off propagation times $t_{d(on)IO}$ and $t_{d(off)IO}$ (specified in the characteristics system ratings section)

Delay times between driver input switchover and IGBT power section switching as caused by the internal driver signal run times. The delay times allow for the suppression of short interference pulses at the SKiiP input. Turn-on or turn-off signals with a pulse duration < $t_{d(on)IO}$ resp. < $t_{d(off)IO}$ are reliably suppressed, while signals of longer pulse durations are reliably processed (see explanations for "Short pulse suppression time t_{SIS}" above.
The SKiiP 3/SKiiP 7 datasheet values are specified at the maximum permissible operating DC link voltage V_{CC}, 0.5 · I_{Cnom} (SKiiP 3/SKiiP 7) resp. I_{Cnom} (SKiiP 4) and T_j = 25°C.

7.4.3.4 Characteristic system ratings

Voltage slopes dV_{CE}/dt_{on}, dV_{CE}/dt_{off} (only SKiiP 4)

Typical voltage slope values for IGBT turn-on and turn-off, specified the maximum permissible operating DC link voltage V_{CC}, T_j = 25°C for switching at I_C = 0A (only applicable for dV_{CE}/dt_{on}) and I_{Cnom}.

Thermal resistance temperature sensor to ambient $R_{th(r-a)}$ (SKiiP 3/SKiiP 7) or heatsink to ambient $R_{th(s-a)}$ (SKiiP 4)

Thermal resistance of SKiiP power section between temperature sensor respective heatsink and ambient (cooling medium). The Figure 7.4.4 illustrates the different reference points between SKiiP 3/SKiiP 7 and SKiiP 4 for thermal specification. The datasheet values of $R_{th(r-a)}$ and $R_{th(s-a)}$ are specified under the cooling conditions in Table 7.4.6.

SKiiP series	Cooling system	Number of folds	Cool. media flow rate	Cooling conditions
SKiiP 3	standard air cooler	2 3 4	460m³/h 420m³/h 390m³/h	T_a = 25°C, altitude 500m above sea level
	standard water cooler	2 3 4	8l/min	$T_{coolant}$ = 50°C, water-glycol ratio 50% : 50%
SKiiP 4	standard air cooler	3 4 6	610m³/h 550m³/h 500m³/h	T_a = 25°C, altitude 500m above sea level
	standard water cooler	3 4 6	15l/min	$T_{coolant}$ = 40°C, water-glycol ratio 50% : 50%
	High Performance water cooler	3 4 6	9l/min 12l/min 18l/min	$T_{coolant}$ = 40°C, water-glycol ratio 50% : 50%
SKiiP 7	standard air cooler	3 4 6	610m³/h 550m³/h 500m³/h	T_a = 25°C, altitude 500m above sea level
	standard water cooler	3 4	15l/min	$T_{coolant}$ = 40°C, water-glycol ratio 50% : 50%
	High Perform. water cooler	3 4	tbd. tbd.	$T_{coolant}$ = 40°C, water-glycol ratio 50% : 50%

Table 7.4.6 SKiiP datasheet specifications of cooling conditions for $R_{th(r-a)}$ or $R_{th(s-a)}$ on various air- or watercooled heatsinks.

Parasitic ohmic terminal-to-terminal lead resistances $R_{CC'+EE'}$

All partial resistances of the SKiiP power part (resistances per switch from all halfbridges in parallel) are pooled to obtain the terminal resistance $R_{CC'+EE'}$ indicated in the datasheet. The partial resistances $R_{CC'}$ and $R_{EE'}$ depicted in Figure 7.3.26 also represent the sum of resistances of the bond connections and terminals. In the SKiiP datasheets the ohmic resistance $R_{CC'+EE'}$ is given at case temperature T_c =25°C. The SKiiP specific pressure system ensures that the pressure is evenly applied to the numerous contacts situated next the chips, thus, resulting in a very low ohmic resistance $R_{CC'+EE'}$.

Collector-emitter commutation inductance L_{CE}

All partial inductances of the SKiiP power section (inductances of all parallel connected halfbridges) are combined to obtain the commutation inductance L_{CE} specified in the data sheet. The partial inductance L_{CE} depicted in Figure 7.3.26 also represent the sum of inductances of the bond connections and terminals.

Coupling capacitance secondary to heatsink C_{CHC}

Small signal coupling capacitance between SKiiP secondary side and the heatsink, measured between AC output and heatsink potential

Coupling capacitance primary to secondary C_{ps} (only SKiiP 4)

Small signal coupling capacitance between a SKiiP primary and secondary side.

Cut-off current I_{CES} + I_{RD}

Sum of IGBT collector-emitter cut-off current and freewheeling diodes direct reverse current (all paralleled switches) at gate-emitter short circuit (V_{GE} = 0V), V_{CE} = V_{CES} and T_j = 25°C

Mechanical data M_{dc}, M_{ac}, w, w_h

The following mechanical data are provided in the datasheets as minimum and maximum values

- Mounting torque M_{dc} of the DC terminals
- Mounting torque M_{ac} of the AC terminals
- Weight w of SKiiP without heatsink
- Weight w_h of heatsink

7.4.4 Information regarding isolation coordination

Included in all SKiiP datasheets, a table provides an overview of the insulation properties of the individual SKiiP series, according to EN 50178, IEC 61800-5-1 and UL 840. There is different information for SKiiP 3/SKiiP 7 and SKiiP 4, listed and explained in chapter 3.3.7.2.
More detailed information on structural dimensioning, isolation limits and also the required voltage reduction for higher installation altitudes can also be found in chapter 3.3.7.2 and in the Technical Explanations specified for the individual SKiiP series.

7.4.5 Information regarding environmental conditions

Also included in all SKiiP datasheets, is a tabular overview of the environmental conditions acc. to IEC 60721 that fulfil the SKiiP IPMs. Please refer to chapter 3.3.7.1 for more detailed explanations.

7.4.6 Diagrams

Similar to the sequence in the datasheets, this chapter provides information on the diagrams in IGBT datasheets, which generally refer to one IGBT switch, freewheeling diode or SKiiP cooling system properties. If the relevant diagrams have already been explained in the IGBT modules chapter, please refer to the relevant descriptions above.

Typical IGBT and freewheeling diode output characteristics $I_C = f(V_{CE})$ and $I_F = f(V_F)$ including $R_{CC'+EE'}$

Figure 7.4.10 shows the typical output characteristics of IGBT and freewheeling diode for the selected SKiiP at T_j = 25°C and the maximum permissible $T_{j(op)}$ in the IGBT's saturation region. The forward voltage is measured at the main terminals inclusive $R_{CC'-EE'}$.

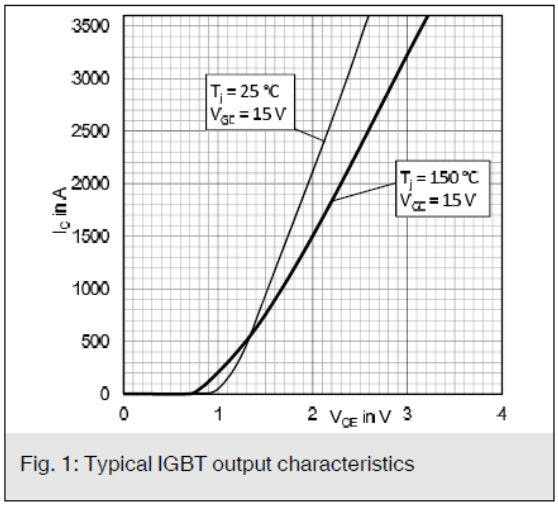


Fig. 1: Typical IGBT output characteristics

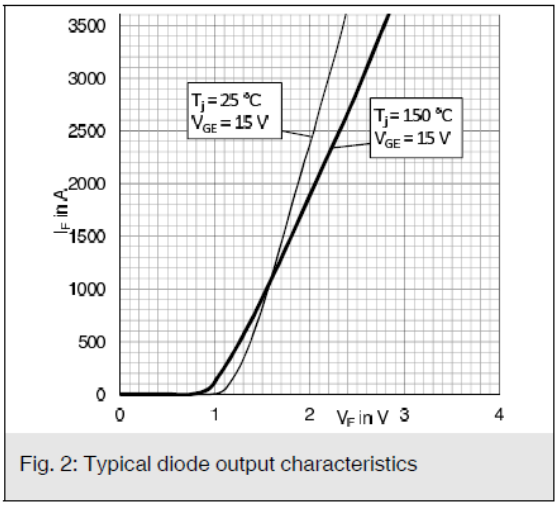


Fig. 2: Typical diode output characteristics

Figure 7.4.10 Typical IGBT and freewheeling diode output characteristics $I_C = f(V_{CE})$ and $I_F = f(V_F)$ including $R_{CC'+EE'}$ of SKiiP2414GB17E4-4DUW

Typical switching energies E_{on}, E_{off} and E_{rr} as a function of the collector current I_C

Figure 7.4.11 shows the typical turn-on and turn-off energy E_{on} + E_{off} of the IGBT as a function of the collector current I_C, determined from a measuring circuit at ohmic-inductive load. Differences in the commutation inductance of the DC link change the ratio from E_{on} and E_{off}. A higher inductance reduces E_{on} but increases E_{off}. Both effects largely compensate for each other. This is the reason to specify only the sum of E_{on} + E_{off} = E_{sw}. Also shown is the turn-off energy E_{rr} of the freewheeling diode. The measurements were carried out at the highest recommended operating temperature at two typical DC link working voltages (e.g. 600V and 900V for 1200V-IGBT or at 900V and 1300V for 1700V-IGBT).

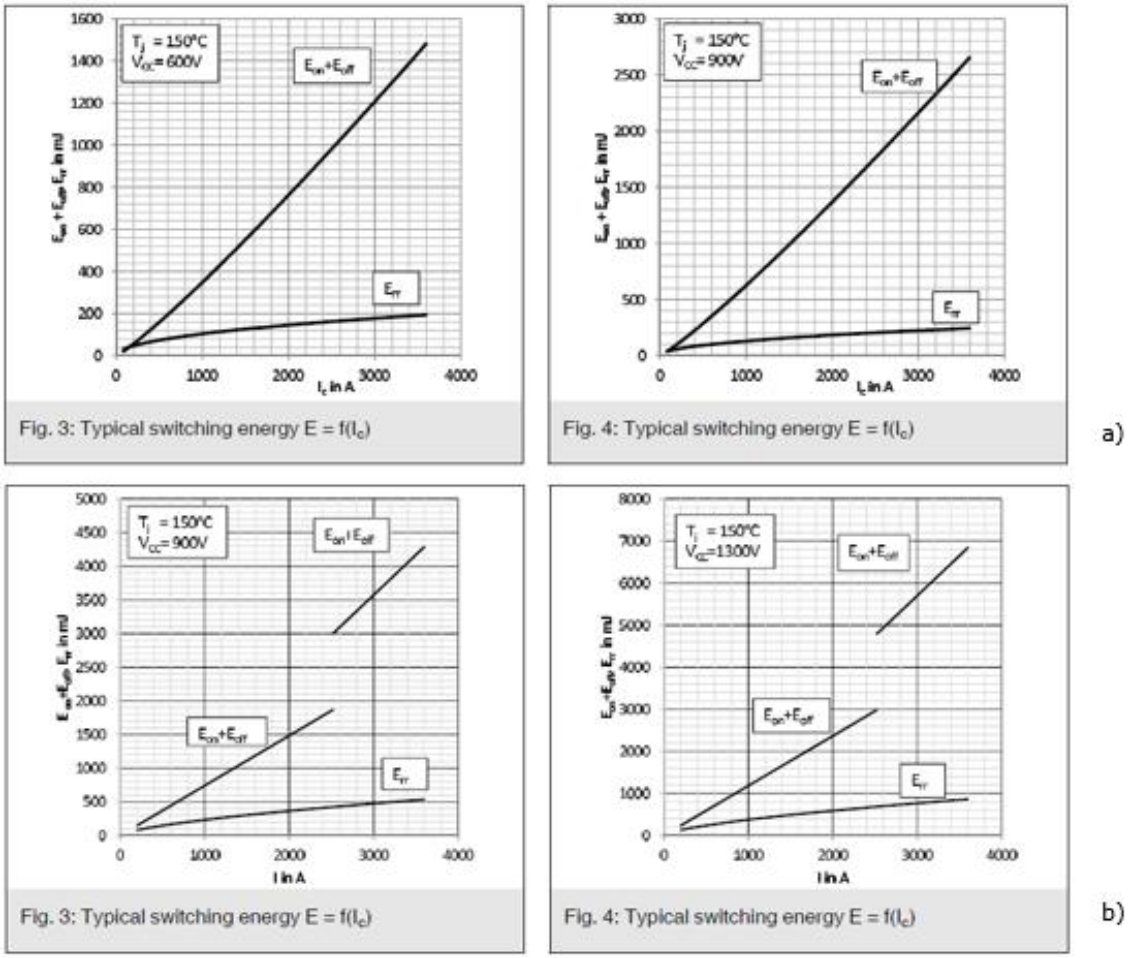


Figure 7.4.11 Typical turn-on/turn-off energy of SKiiP IGBT and inverse diode versus collector current at maximum permissible $T_{j(op)}$ and two different DC link voltages for: a) SKiiP2414GB12E4-4DUW (1200V SKiiP 4 without "IntelliOff" function); b) SKiiP2414GB17E4-4DUW (1700V SKiiP 4 with "IntelliOff" function)

At the most types of 1700V SKiiP 4 the protection against short circuit and overcurrent situations is realised by initiating a called "IntelliOff" soft turn-off function, described in chapter 3.3 above. This dedicated soft turn-off function generates two different gate turn-off speeds determined by optimized gate resistors of the internal the gate driver. The suitable gate turn-off speed will be chosen as a function of the actual measured AC current value. As already shown in Figure 3.3.8, the two different turn-off speed scenarios are:

- Hard turn-off: optimised for low switching losses
- IntelliOff: optimised fur reduced overvoltage at overload

The diagram in Figure 7.4.11 b) illustrates the consequence of switchover to a lower turn-off speed: If the AC output current exceeds a threshold value and initiates the IntelliOff function, the turn-off losses E_{off} (and therefore the switching energy E_{on} + E_{off}) rises sharply to then continue to run at a higher level proportional to the AC output current.

SKiiP 3 - Typical thermal impedances $Z_{th(j-r)}$ and $Z_{th(r-a)}$ of IGBT and freewheeling diode

Figure 7.4.12 shows the thermal impedances $Z_{th(j-r)}$ and $Z_{th(r-a)}$ for the IGBT- and diode switches of a watercooled SKiiP 3 IPM SKiiP2403 GB172-4DW V3 in single-pulse operation as a function of the pulse duration t.

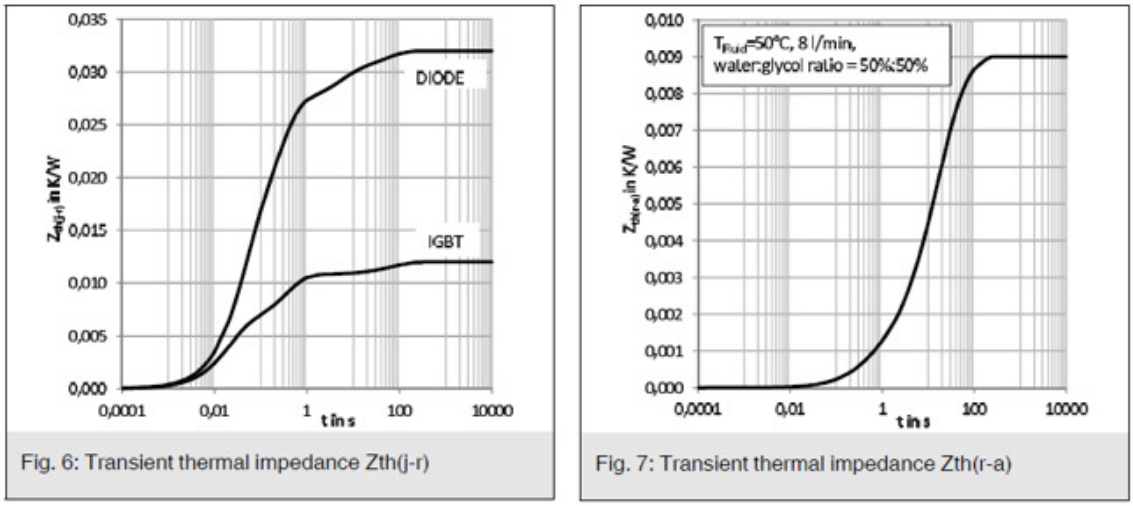


Figure 7.4.12 Typical thermal impedances $Z_{th(j-r)}$ and $Z_{th(r-a)}$ for IGBT and freewheeling diode of SKiiP2403GB172-4DW

Please refer in the "characteristics" parts of chapter 7.4.3 for more detailed explanations about the meaning of the symbols and the differences of thermal models between SKiiP 3 and SKiiP 4.

SKiiP 4 - Typical thermal impedances $Z_{th(j-s)}$, $Z_{th(j-r)}$ and $Z_{th(s-a)}$ of IGBT and freewheeling diode

Figure 7.4.13 shows the thermal impedances $Z_{th(j-s)}$, $Z_{th(j-r)}$ and $Z_{th(s-a)}$ for the IGBT- and diode of a watercooled SKiiP 4 IPM SKiiP2414GB17E4-4DUW V2 in single-pulse operation as a function of the pulse duration t.

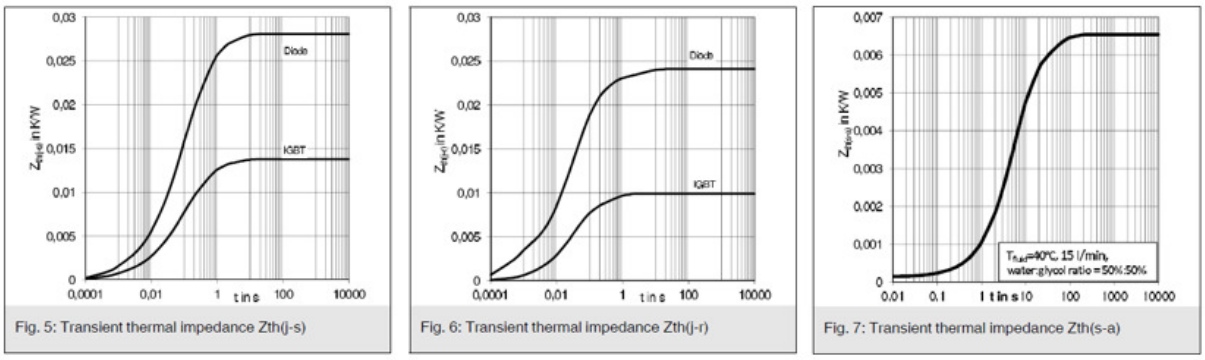


Figure 7.4.13 Typical thermal impedances $Z_{th(j-c)}$, $Z_{th(j-r)}$ and $Z_{th(s-a)}$ at IGBT and freewheeling diode switches of SKiiP2414GB17E4-4DUW

Coefficients R_{th} and τ_{th} for thermal modelling

The thermal impedances Z_{th} can determine numerically as parameters R_{thi} and τ_{th} of a thermal model, see example in Figure 7.3.36.

$$Z_{th} = \sum_{i=1}^{n} R_{thi} \cdot \left(1 - e^{-t/\tau_{hi}}\right)$$

In Figure 7.4.14 the coefficients R_{thi} and τ_{thi} of a four time-constant model are listed for customer-side thermal modelling. These coefficients are also used for modelling with Semikron Danfoss's SemiSel simulation tool.

	Rth [K/W]				
	1	2	3	4	5
Zth(j-r) I	0,0012	0,0050	0,0058	0,0000	0,0000
Zth(j-r) D	0,0020	0,0030	0,0135	0,0135	0,0000
Zth(r-a)	0,0027	0,0046	0,0011	0,0006	0,0000
	tau [s]				
	1	2	3	4	5
Zth(j-r) I	69,0000	0,3500	0,0200	1,0000	1,0000
Zth(j-r) D	50,0000	5,0000	0,2500	0,0400	1,0000
Zth(r-a)	48,0000	14,600	2,8000	0,3500	1,0000

Fig. 8: Coefficients of thermal impedances

a)

	R_{th} [K/W]				
	1	2	3	4	5
$Z_{th(j-s)}$ I	0,0010	0,0049	0,0055	0,0017	0,0007
$Z_{th(j-s)}$ D	0,0020	0,0100	0,0112	0,0034	0,0015
$Z_{th(j-r)}$ I	0,0020	0,0048	0,0023	0,0008	
$Z_{th(j-r)}$ D	0,0012	0,0039	0,0104	0,0054	0,0032
$Z_{th(s-a)}$	0,0014	0,0050	0,0001		
	tau [s]				
	1	2	3	4	5
$Z_{th(j-s)}$ I	3,6500	0,4100	0,0650	0,0090	0,0008
$Z_{th(j-s)}$ D	3,6500	0,4100	0,0650	0,0090	0,0008
$Z_{th(j-r)}$ I	0,4500	0,0475	0,0142	0,0016	
$Z_{th(j-r)}$ D	4,1546	0,2644	0,0497	0,0107	0,0005
$Z_{th(s-a)}$	34,2609	5,2284	0,0005		

Fig. 8: Coefficients of thermal impedances

b)

Figure 7.4.14 Coefficients R_{th} and τ_{th} of a four time-constant model for customer-side thermal modelling: a) SKiiP2403GB172-4DW; b) SKiiP2414GB17E4-4DUW

Thermal resistances $R_{th(r-a)}$ or $R_{th(s-a)}$ of SKiiP IPM depending on cooling media flow rate V

The diagrams in Figure 7.4.15 show the respective dependence of the thermal heatsink resistance $R_{th(r-a)}$ (SKiiP 3) or $R_{th(s-a)}$ (SKiiP 4) on the coolant flow rate V_{air} in m³/h (air cooling) or V_{fluid} in l/min (fluid cooling) for SKiiP with air or water cooling. Note the different reference point "r" or "s" for the thermal heatsink resistance between SKiiP 3 and SKiiP 4.

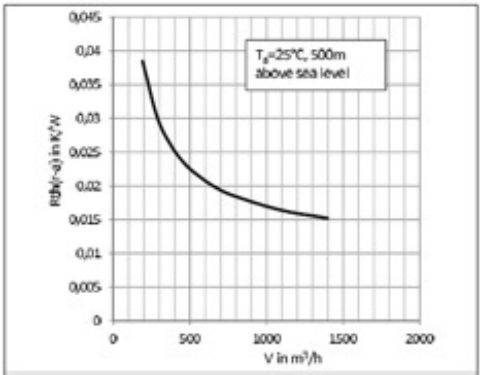


Fig. 9: Thermal resistance Rth(r-a) versus flow rate V

a)

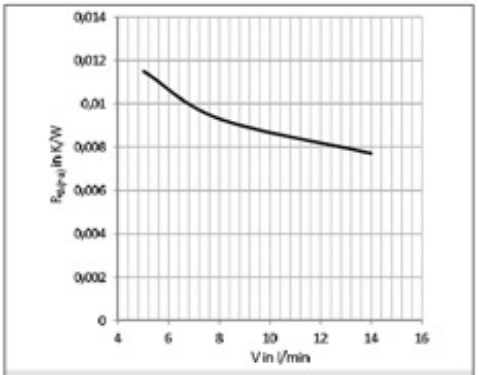


Fig. 9: Thermal resistance Rth(r-a) versus flow rate V

b)

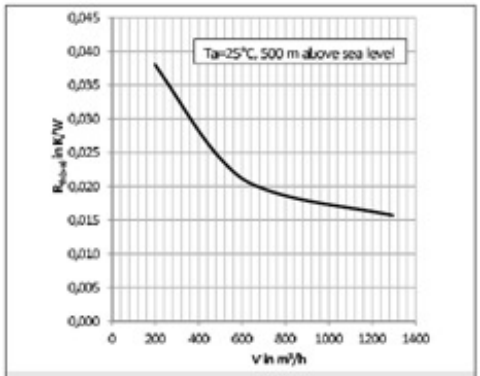


Fig. 9: Thermal resistance Rth(s-a) versus flow rate V

c)

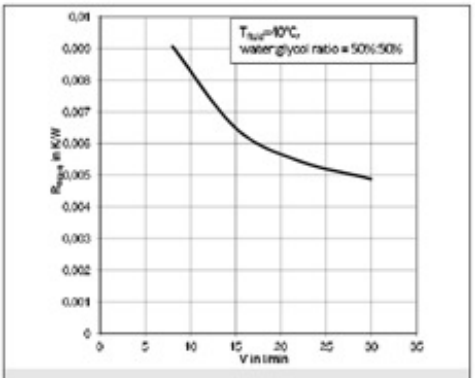


Fig. 9: Thermal resistance Rth(s-a) versus flow rate V

d)

Figure 7.4.15 Dependence of thermal heatsink resistance on the coolant flow rate: a) $v_{air} = f(R_{th(r-a)}$ of aircooled SKiiP2013GB172-4DL; b) $v_{liquid} = f(R_{th(r-a)}$ of watercooled SKiiP2013GB172-4DW; c) $v_{air} = f(R_{th(s-a)})$ of aircooled SKiiP2414GB17E4-4DUL V2; d) $v_{liquid} = f(R_{th(s-a)}$ of watercooled SKiiP2414GB17E4-4DUW

Coolant pressure drop ΔP depending on coolant flow rate V

The diagrams in Figure 7.4.16 show the dependence of the coolant pressure drop ΔP on the coolant flow rate v_{air} in m³/h (air cooling) or v_{fluid} in l/min (fluid cooling) for SKiiP with air or water cooling on an example from SKiiP 3 datasheet. Please refer in the chapters 5.4.2 and 5.4.3 for more detailed explanations regarding the properties of cooling systems.

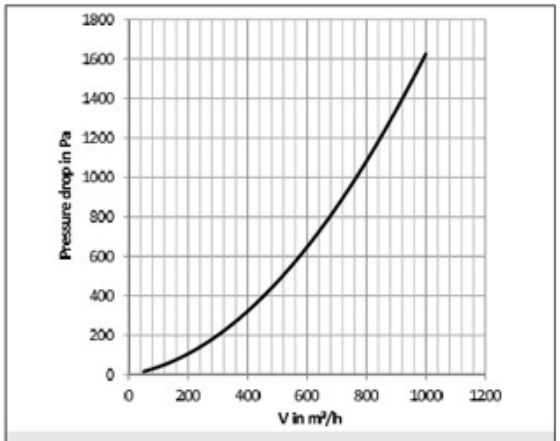


Fig. 5: Pressure drop Δp versus flow rate V

a)

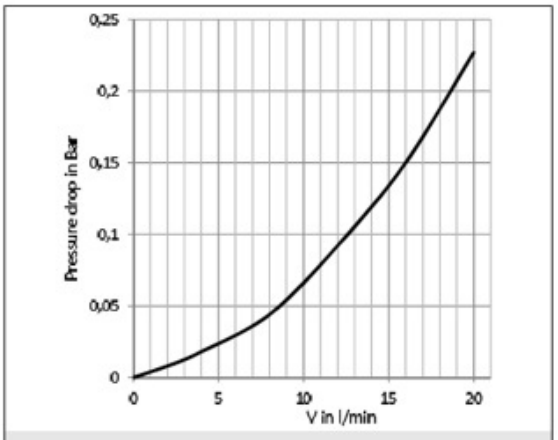


Fig. 5: Pressure drop Δp versus flow rate V

b)

Figure 7.4.16 Dependence of the cooling media pressure drop on the cooling media flow rate for a) aircooled SKiiP2013GB172-4DL; b) watercooled SKiiP2013GB172-4DW

7.5 Datasheet specifications for SiC MOSFET Modules

7.5.1 Topologies and type designation of power modules with SiC MOSFET

Semikron Danfoss offers Silicon Carbide MOSFET modules (Full SiC Modules) in SEMITOP and SEMITRANS housings, see Table 7.3.1 above. Due to their connection flexibility and very low internal inductances, especially SEMITOP modules allow the integration of a large number of topologies.
Achieve high switching frequency, minimal losses and maximum efficiency using SiC MOSFET and SiC Schottky barrier diodes (SBD) chips diode from leading suppliers. Silicon Carbide also offers excellent power density.
The SiC market and development is very dynamic and chip supplier and generations used in the modules will change very fast. The SiC MOSFET modules are available from 20A to 540A in 1200V and 1700V, with and without anti-parallel freewheeling SBDs. Power modules e.g. including halfbridge sixpack and boost converters topologies are available, see Table 7.5.1 and Table 7.5.2.
This chapter contains explanations of the datasheets for power modules that exclusively contain SiC MOSFET and partly also SiC Schottky barrier diodes. For explanation on power modules with "mixed" Si ad SiC semiconductors please refer to chapter 7.3.
Some of the common topologies of SiC MOSFET modules and the above-mentioned product lines in which these are being integrated are shown in Table 7.5.1 and Table 7.5.2.

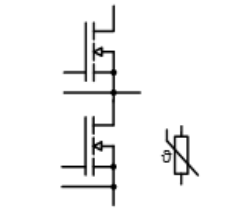
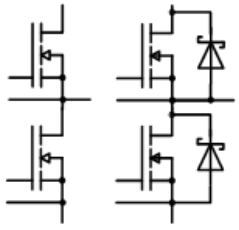
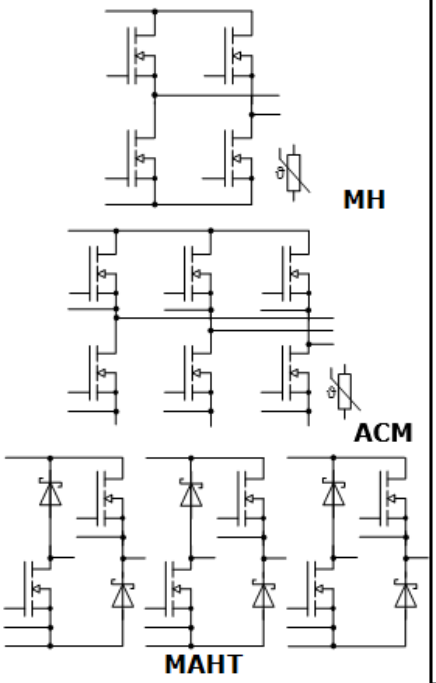
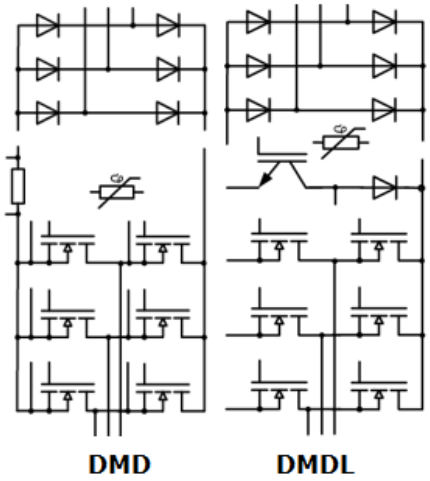
Halfbridge modules	H-Bridge and 3-phase Bridge modules	3-phase CI and CIB modules
 		
MB: SiC MOSFET Halfbridge SEMITOP (MB...T) SEMITRANS (SC/SCH15, SCH17)	**MH: Symmetrical H-Bridge** SEMITOP **ACM: Sixpack (open Emitter)** SEMITOP **MAHT: 3-Phase asymmetrical Halfbridge** SEMITOP	**DMD: Converter-Inverter** SEMITOP **DMDL: Converter-Inverter-Brake** SEMITOP

Table 7.5.1 Topology examples of SiC MOSFET converter bridge modules

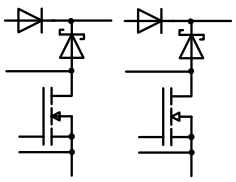
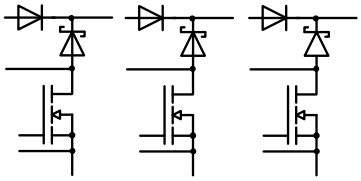
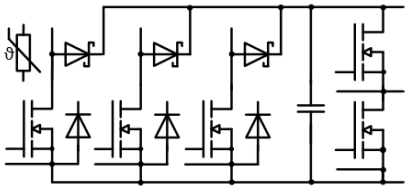
Double Boost converter modules	Triple Boost converter modules
 **MLLE: Double Boost converter + bypass diodes** SEMITOP	 **MLET: Triple Boost converter + bypass diodes** SEMITOP
	 **MLTB: Triple Boost converter + bypass diodes + halfbridge** SEMITOP

Table 7.5.2 Topology examples of SiC MOSFET modules for boost converter applications

The images of the module housings per product line are already listed in chapter 7.3.1. The respective designation codes are shown in Figure 7.5.1 and Figure 7.5.2.

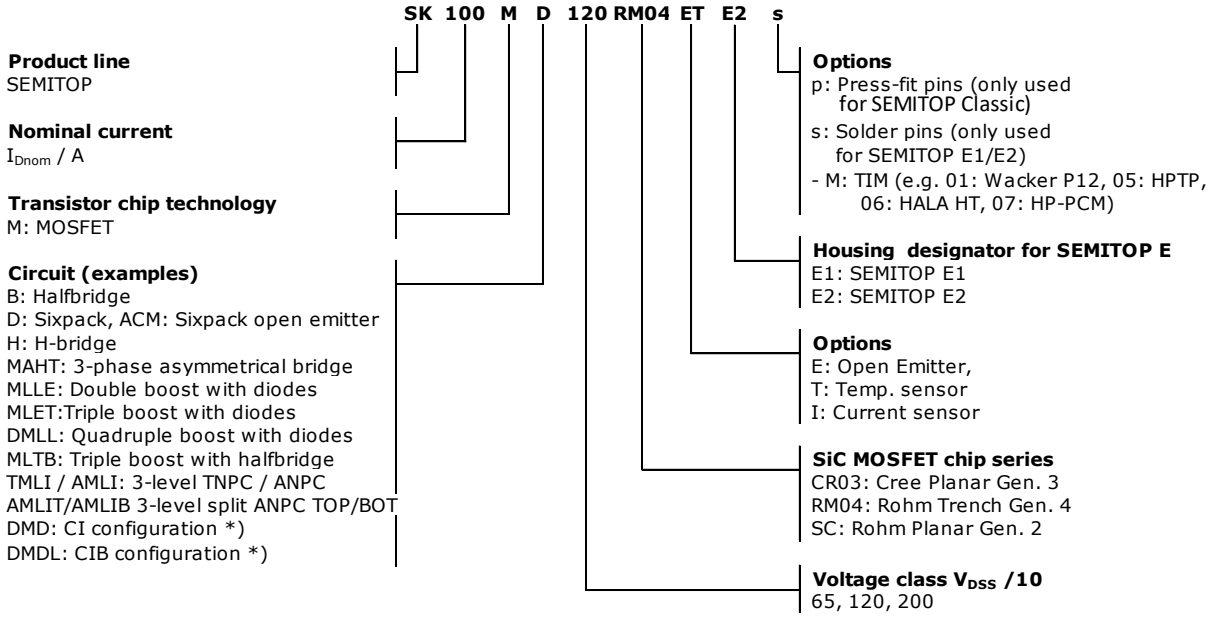


Figure 7.5.1 SEMITOP SiC MOSFET module type designation code; *) see chapter 7.3.1.3 for additional statements about CIB modules)

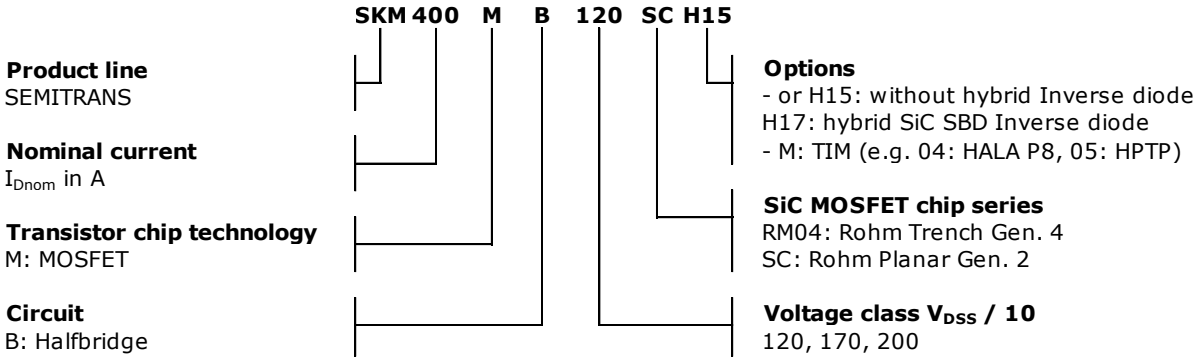


Figure 7.5.2 SEMITRANS SiC MOSFET module type designation code

7.5.2 Absolute maximum ratings

In the datasheets, the maximum ratings are specified separately for each individual component of the power module (SIC MOSFET, body or hybrid integrated inverse diode, module structure and temperature sensor if available), see Figure 7.5.3. All ratings for SiC MOSFET and diodes refer to one switch (arm), irrespective of the number of chips actually connected in parallel per switch (arm) inside the power module.

Absolute Maximum Ratings				
Symbol	**Conditions**		**Values**	**Unit**
MOSFET				
V_{DSS}	T_j = 25 °C		1200	V
I_D	HPTP / HP-PCM T_j = 175 °C	T_s = 25 °C	267	A
		T_s = 70 °C	223	A
I_{DM}	Pulse witdh t_p limited by T_{vjmax}		720	A
V_{GS}	Transient Gate - Source voltage (t<100ns)		-8 ... 19	V
T_j			-40 ... 175	°C
Integrated body diode				
I_{FM}	Pulse width t_p limited by T_{vjmax}		720	A
I_{FSM}	t_p = 10 ms, sin 180°, T_j = 150 °C		1076	A

Absolute Maximum Ratings			
Symbol	**Conditions**	**Values**	**Unit**
Module			
$I_{t(RMS)}$	$\Delta T_{terminal}$ at PCB joint = 30 K, per pin	30	A
T_{stg}	module without TIM	-40 ... 125	°C
V_{isol}	AC, sinusoidal, t = 1 min	2500	V

Figure 7.5.3 Maximum ratings of SiC MOSFET module SK250MB120CR03TE2 without integrated inverse diode [7.51]

7.5.2.1 SiC MOSFET maximum ratings

Drain-Source voltage V_{DSS}

Maximum permissible voltage between the drain and source terminals of the SIC MOSFET chips with gate-source short circuited at junction temperature T_j = 25°C. The maximum drain-source voltage increases in proportion to the temperature owing to the temperature dependency of the breakdown voltage. Irrespective of the load conditions, the sum of the drain-source supply voltage V_{DD} and the switching overvoltage $\Delta V_{DS} = L_\sigma \cdot di_D/dt$ must not exceed voltage V_{DSS} (L_σ: sum of the parasitic inductances in the commutation circuit).

Continuous Drain current I_D

Calculated maximum direct current at the drain at which the permissible chip temperature is reached. The current is calculated with a fixed case or heatsink temperature and $T_j = T_{j(max)}$

$$I_D = \sqrt{\frac{T_j - T_n}{R_{th(j-n),max} \cdot R_{DS(on),max,Tj}}}$$

n: case (c) or sink (s) - depending on whether the module has a baseplate or not

The datasheet values are given for case temperatures T_c = 25°C / 80°C (baseplate modules) or T_s = 25°C / 70°C (baseplate-less modules) for a specified thermal interface medium. e.g. pre applied High Performance Thermal Paste (HPTP), pre-applied phase changer material (HP-PCM) or thermal grease with a specified thermal conductivity λ_{grease}.
Since I_D designates a static value (direct current), it is not relevant for switching operation. The value is used only as a comparison to other devices to give an indication of the current capability.

Peak value of a pulsed drain current I_{DM}

Repetitive peak drain current that the MOSFET (in on-state) is able to withstand under normal operation without damage. The duration of the current pulse must be limited to prevent the junction temperature from exceeding $T_{j(max)}$. This value is similar to I_{CRM} for a silicon IGBT and is valid for current flowing in either direction through the on-state drain-source channel.

Gate-source voltage V_{GS}

Permitted range of voltage (usually indicated as transient (t<100ns) or static) between the gate and source terminals with drain-source shorted (V_{DS} = 0). This value varies with chip technology/generation). Recommended turn-off / turn-on gate-source voltages are given in the shaded area "Remarks" to the left of the maximum ratings and characteristics.

Junction temperature range T_j; $T_{j(min)}$...$T_{j(max)}$

Permissible chip temperature range $T_{j(min)}$ to $T_{j(max)}$. For continuous operation the maximum chip temperature $T_{j(op)}$ should be kept at least 25K below $T_{j(max)}$, see also "Remarks" in the shaded area to the left of the maximum ratings and characteristics.

7.5.2.2 Maximum ratings of body diode or integrated inverse diodes

Peak value of pulsed diode forward current I_{FM}

Repetitive peak forward current that the body diode (MOSFET in off-state) is able to withstand under normal operation without damage. The duration of the current pulse must be limited to prevent the junction temperature from exceeding $T_{j(max)}$. This value is similar to I_{FRM} for a silicon diode.

Surge forward current I_{FSM}

If the inverse diodes are used as line rectifiers, their non-repetitive short-time overload capability is definitive for the choice of protective circuits. The non-repetitive peak forward current I_{FSM} in the form of a half-sine wave with pulse width, t_p, that the body or hybrid inverse diode (MOSFET in off-state) is able at a specified junction temperature T_j to withstand in the event of a malfunction (e.g. short circuit), provided it does not occur too often during the diode lifetime.
When the device is subjected to a current near I_{FSM}, the junction temperature can reach values in excess of $T_{j(max)}$, causing damage to the chip metallization. Additionally, the blocking voltage capability of the diode immediately following the surge current event is reduced. The datasheet value of I_{FSM} is valid for an event in which the diode is not expected to block any reverse voltage. Therefore, should a reverse voltage occur immediately after a diode has been exposed to surge current load, the permissible surge forward current peak will be lower than if no subsequent reverse voltage is involved. The duration of single or several subsequent phases can be determined from the surge forward current characteristics, see Figure 7.3.15.
Exclusively, datasheets of SiC MOSFET modules with hybrid integrated SBC inverse diodes may contain further maximum data of the inverse diode (Figure 7.5.4).

Absolute Maximum Ratings				
Symbol	Conditions		Values	Unit
Inverse diode				
V_{RRM}	T_j = 25 °C		1200	V
I_F	T_j = 175 °C	T_c = 25 °C	187	A
		T_c = 80 °C	143	A
I_{Fnom}			100	A
I_{FRM}			300	A
I_{FSM}	t_p = 8.3 ms, sin 180°, T_j = 25 °C		373	A
T_j			-40 ... 175	°C

Figure 7.5.4 Additional maximum ratings of integrated inverse SiC diode of SiC MOSFET module SKM350MB120SCH17 [7.53]

Repetitive peak reverse voltage V_{RRM}

Maximum permissible values for repetitive transient peak voltages in the reverse blocking state of the inverse diode at T_j = 25°C…T_{jmax}. Please note that V_{RRM} is lower at very low temperatures.

Inverse diode forward current (continuous drain current in reverse direction) $I_F = -I_D$

Maximum rated direct reverse current at drain output; maximum ratings and parameters are identical to those for forward direction.

Nominal diode current I_{Fnom}

Rated current of the diode chips used as indicated in the chip manufacturer's datasheet, multiplied by the number of diode chips connected in parallel in the module per switch.

Repetitive peak forward current of the inverse diode I_{FRM}

The permissible repetitive peak forward current depends on the feasible power dissipation and the thermal impedance Z_{th}, but also takes into account bonding wire failure mechanisms and overvoltage. The datasheet value I_{FRM} specifies this repetitive forward current considering the practical limitations of the power module. Up to I_{FRM}, switching operation of the diode is permissible.
This value is similar to I_{FRM} for a silicon freewheeling diode.

Junction temperature range of hybrid integrated inverse diode T_j; $T_{j(min)}$...$T_{j(max)}$

Permissible chip temperature range $T_{j(min)}$ to $T_{j(max)}$. For continuous operation the maximum chip temperature $T_{j(op)}$ should be kept at least 25K below $T_{j(max)}$.

7.5.2.3 Maximum module ratings

Maximum terminal RMS current $I_{t(RMS)}$

The value is applicable to any current characteristic or cooling conditions. It depends on the current carrying capacity of the internal connections and the terminals of the IGBT module. For the example of module with Press-fit terminals above, $I_{t(RMS)}$ is specified at a given terminal temperature difference per pin at PCB joint.

Storage temperature range T_{stg}; T_{stgmin}...T_{stgmax}

Temperature range within which the module may be stored or transported without being subject to electrical load; T_{stgmax} is also the maximum permissible case/housing temperature T_{cmax} for the module in application.
The storage temperature of the power module will also affect the Thermal Interface Material (TIM). The temperature limit values listed apply to an IGBT module without TIM coating. For modules with pre-applied TIM, the permissible limit values of the specific TIM material must be adhered too. Please check the maximum permitted operation condition in the relevant TIM datasheet resp. Technical Explanation [7.29].

Insulation test voltage V_{isol}

RMS value of the permissible test voltage (50 Hz AC voltage) between the short circuited terminals and insulated module baseplate with the parameter test duration (1min or 1s); for details see

chapter 3.2.1 and [7.19].

7.5.3 Characteristics

7.5.3.1 SiC MOSFET characteristics

In the datasheets, the characteristics are likewise specified separately for each individual component. Again, all characteristics refer to one switch, irrespective of the number of paralleled chips per switch (Figure 7.5.5).

Characteristics						
Symbol	**Conditions**		**min.**	**typ.**	**max.**	**Unit**
MOSFET						
$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 0.6 mA, T_j = 25 °C		1200			V
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 69 mA, T_j = 25 °C		1.8	2.5	3.6	V
I_{DSS}	V_{GS} = 0 V, V_{DS} = 1200 V, T_j = 25 °C				0.6	mA
I_{GSS}	V_{DS} = 0 V, V_{GS} = 15 V, T_j = 25 °C				400	nA
$R_{DS(on)}$	V_{GS} = 15 V, I_D = 248 A, chiplevel	T_j = 25 °C		5.3	7.2	mΩ
		T_j = 150 °C		8.3		mΩ
C_{iss}	V_{GS} = 0 V, V_{DS} = 1000 V, T_j = 25 °C	f = 0.1 MHz		20400		pF
C_{oss}		f = 0.1 MHz		780		pF
C_{rss}		f = 0.1 MHz		60		pF
Q_G	V_{GS} = -4…15V, V_{DD} = 800V, I_D = 248 A			708		nC
R_{Gint}	T_j = 25 °C			2.3		Ω
$t_{d(on)}$	V_{DD} = 600 V I_D = 240 A V_{GS} = -4/+15 V $R_{G\ on/off}$ = 0.5 Ω di/dt_{off} = 15 kA/µs di/dt_{on} = 22 kA/µs dv/dt = 29 kV/µs L_s = 5 nH	T_j = 150 °C		49		ns
$t_{d(off)}$		T_j = 150 °C		120		ns
t_r		T_j = 150 °C		17		ns
t_f		T_j = 150 °C		29		ns
E_{on}		T_j = 150 °C		2.97		mJ
E_{off}		T_j = 150 °C		2.57		mJ
$R_{th(j-s)}$	per MOSFET, HPTP / HP-PCM			0.19		K/W

Figure 7.5.5 MOSFET characteristic data of module SK250MB120CR03TE2

Drain-source breakdown voltage $V_{(BR)DSS}$

Breakdown voltage (minimum value) between drain and source with gate-source shorted (V_{GS} = 0V). Value given for impressed leakage current I_D at junction temperature T_j = 25°C. As most SiC MOSFET devices do not allow operation in the avalanche region. The minimum value of $V_{(BR)DSS}$ will usually be equal to V_{DSS}.

Gate-source threshold voltage $V_{GS(th)}$

Gate-emitter voltage (minimum/typical and maximum value) above which a specified considerable source current will flow at junction temperature T_j = 25°C and equal values of drain-source voltage V_{DS} and gate-source voltage V_{GS}.

Drain leakage current I_{DSS}

Leakage current (maximum value) between drain and source with gate-source shorted (V_{GS} = 0) at maximum permissible drain-source voltage and specified junction temperature.

Gate leakage current I_{GSS}

Leakage current (maximum value) between gate and source with drain-source shorted (V_{DS} = 0) at specified gate-source voltage and junction temperature.

Static drain-source on-state resistance $R_{DS(on)}$

Quotient of measured drain-source voltage V_{DS} on SiC MOSFET chip-level and drain current I_D, in a fully gate-controlled at specified gate-source voltage, drain current and junction temperatures T_j = 25°C and T_j = 150°C (typical value). $R_{DS(on)}$ is strongly dependent on V_{GS}. T_j and to a certain extend also on the current, see also chapter 2.5.2.

Input capacitance C_{iss}

Low-signal, short circuit capacitance in common-source configuration between gate and source with drain-source short circuited for AC current (typical value); measured at specified drain-source direct voltage V_{DS} and specified measuring frequency f at junction temperature T_j = 25°C

Output capacitance C_{oss}

Low-signal, short circuit capacitance in common-source configuration between drain and source with gate-source short circuited for AC current (typical value); measured at specified drain-source direct voltage V_{DS} and specified measuring frequency f at junction temperature T_j = 25°C

Reverse transfer capacitance C_{rss}

Low-signal capacitance in common-source configuration between drain and gate with gate-source short circuited for AC current (typical value); measured at specified drain-source direct voltage V_{DS} and specified measuring frequency f at junction temperature T_j = 25°C
In the equivalent circuit diagram, to describe the switching behaviour, the input capacitance C_{iss} is divided into the gate-source capacitance C_{GS} and the gate-drain (Miller) capacitance C_{GD} (Table 7.5.3).

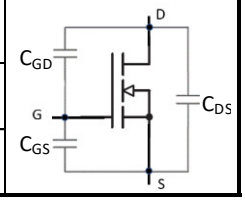
Description	SiC MOSFET	Equivalent Circuit
Input capacitance	$C_{iss} = C_{GS} + C_{GD}$	
Output capacitance	$C_{oss} = C_{GD} + C_{DS}$	
Reverse transfer capacitance	$C_{rss} = C_{GD}$	

Table 7.5.3 Combination of internal transistor capacitances

Gate charge Q_G

Total charge (typical value) required to transduce the SiC MOSFET at a given operation voltage V_{DD} from defined off-state (specified gate-source voltage $V_{GS} = V_{GS(off)} \leq 0V$) to the static on-state with specified drain current I_D and $V_{GS} = V_{GS(on)}$. The gate charge Q_G is almost independent of the chip temperature and only slightly dependent on the operation voltage. From Q_G using $I_{G(AV)} = Q_G \cdot f_{sw}$, the mean gate current supplied by the driver $I_{G(AV)}$ can be determined (f_{sw}: switching frequency).

Internal gate resistance R_{Gint}

SiC MOSFET chips are equipped with integrated gate resistors to avoid oscillations between paralleled chips. R_{Gint} is the total resistance resulting from paralleling of MOSFET chips. The datasheet table contains a typical value for R_{Gint} at a junction temperature Tj = 25°C (R_{Gint} is temperature-dependent.). When configuring the driver circuit based on a minimum gate resistance or maximum gate peak current, the sum of the external gate resistances R_{Gon}/R_{Goff} and the internal gate resistance R_{Gint} given in the datasheet must be taken into account.

Switching times $t_{d(on)}$, t_r, $t_{d(off)}$, t_f and switching energies E_{on}, E_{off}

For unipolar devices are the switching times and losses almost independent of the junction temperature, the values in the tabular are given as typical values for the maximum recommended junction temperature, e.g. T_j = 150°C. Switching times and losses as well as current and voltage curves are strongly influenced by the real operating conditions in the application. Due to the fast switching, internal and external capacitances, gate and commutation inductances as well as the tolerance of the gate power supply have a much greater influence on the switching behaviour than is known from IGBT. For applications with operating conditions where switching losses are dominant, the data given in the datasheets must be seen as a rough guideline only. In such cases, it is strongly recommended to perform additional measurements under real application conditions to ensure safe layout of the circuitry.
Switching times and energies indicated in Semikron Danfoss datasheets for modules are determined in double pulse test with inductive load in accordance with Figure 7.5.6 a) and measured similar to the specifications of IEC 60747-8 [7.4].
When the SiC MOSFET is in off-state, the current will flow through the freewheeling diode or the body diode of the opposite MOSFET dependent on the circuit in the module. commutate to the

transistor during turn-on and back to the freewheeling diode on turn-off (hard switching). For deadtime > 2µs it does not matter of the MOSFET channel is opened for reverse conduction or not. The reverse recovery charge of the body diode will contribute to the switching losses to the same amount. Only for very short deadtimes in the range of a few 100ns Q_{rr} is reduced [7.56]. The typical switching losses are that of the worst switch in the circuit realised in one housing, e.g. for a halfbridge the highest value of TOP or BOT switch.

In the tabular datasheet characteristics, switching times and switching energies are given at maximum operational junction temperature $T_{j(op)}$ for a typical MOSFET operating point, characterised by supply voltage V_{DD}, nominal drain current I_{Dnom}, gate control voltages $\pm V_{GS}$, external gate resistances R_{Gon}, R_{Goff}, collector current slopes di/d_{ton} during turn-on and di/dt_{off} during turn-off, drain-source voltage slope dv/dt as well as commutation circuit stray inductance L_s.

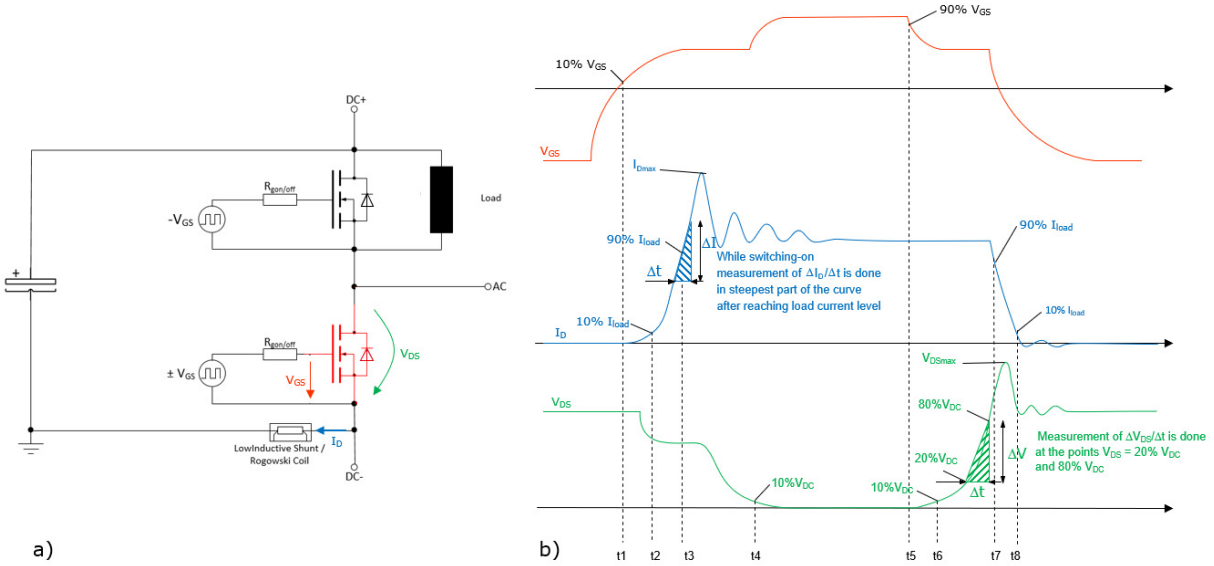


Figure 7.5.6 Switching times of SiC MOSFET: a) Measuring circuit; b) Definition of switching times [7.4], [7.5]

The following explanations refer to the times t_1...t_8 shown in Figure 7.5.6 b):

Turn-on

The turn-on delay time $t_{d(on)}$ (interval t_1...t_2) is defined as the time interval between the moment when the rising gate-source voltage v_{GS} has reached 10% of its positive end value and the drain current i_D has increased to 10% of the load current. During the subsequent rise time t_r (interval t_2...t_3), the drain current i_D increases from 10% to 90% of the load current. The sum of turn-on delay time $t_{d(on)}$ and rise time t_r is called turn-on time t_{on}.
The turn-on energy E_{on} is calculated by

$$E_{on} = \int P_{on}\, dt = \int_{t2}^{t4} v_{DS}\,(t) \cdot i_D\,(t)$$

In the interval t_2 (i_D = 10% of I_L) to t_4 (v_{DS} = 10% of V_{DD}). This means that E_{on} includes the power losses caused by the peak reverse current I_{RRM} induced by the reverse recovery process of the body diode of a complementary MOSFET (freewheeling diode). Please note that SiC MOSFET modules equipped with inverse SiC Schottky barrier freewheeling diodes have significantly reduced turn-on losses, see chapter 7.5.3.2

Turn-off

The turn-off delay time $t_{d(off)}$ is defined as the time interval between the moment when the gate-source voltage v_{GS} has dropped to 90% of its on-state value and the collector current has declined to 90% of the load current value (interval t_5...t_7). During the subsequent fall time t_f (interval t_7...t_8), the drain current i_D drops from 90% to 10% of the load current I_L. The sum of turn-off delay time $t_{d(off)}$ and fall time t_f is called turn-off time t_{off}.
The turn-off energy E_{off} is calculated by

$$E_{off} = \int P_{off}\,dt = \int_{t6}^{t8} v_{DS}\,(t) \cdot i_D\,(t)\,dt$$

and thus covers the time interval from v_{DS} is risen to 10% of V_{CC} (t_6) to i_C is dropped to 10% of the load current I_L (t_8). This means that the E_{off} includes the power losses caused by the v_{DS} overshot during di_D/dt_{off}. This overshoot mainly results from the parasitic inductances in the commutation circuit, increasing proportionally with increasing turn-off speed $-di/dt_{off}$ of the SiC MOSFET.

Maximum turn-on time during short circuit t_{psc}

Maximum duration at which the MOSFET limits the current with full DC voltage applied caused by a short circuit is specified at high junction temperature T_j and a given control voltages $V_{GS(on)}$ / $V_{GS(off)}$ up to maximum values of DC supply voltage V_{DD}, drain-source voltage V_{DS} and short circuit energy E_{SC}.
In contrast to IGBT chips, power dissipation during short circuit is produced almost entirely within the channel structure and only heats the surface of the chip, not the complete chip volume. Also SiC MOSFET chips are much smaller than an equivalent IGBT with a higher current density. Therefore, SiC MOSFET reach critical temperatures at shorter pulses. Some SiC MOSFET only allow short circuit durations of less than 2µs, while others are not capable of withstanding any short circuit.
Please note that, unlike the corresponding specifications for IGBT, the specified times are not guaranteed limit values. If no t_{psc} value is present in the datasheet table, the chip does not have any short circuit capability.

Thermal resistances $R_{th(j-c)}$ and $R_{th(c-s)}$ respective $R_{th(j-s)}$ per SiC MOSFET switch

Thermal resistances for a MOSFET switch within a module, irrespective of the number of MOSFET chips connected in parallel:

modules with baseplate:
$\Delta T_{(j-c)} = T_j - T_c = P_T \cdot R_{th(j-c)}$
$\Delta T_{(c-s)} = T_j - T_c = P_T \cdot R_{th(c-s)}$

baseplate-less modules:
$\Delta T_{(j-s)} = T_j - T_s = P_T \cdot R_{th(j-s)}$

The datasheet values are given for a specified thermal interface medium. e.g. pre-applied High Performance thermal paste (HPTP), pre-applied phase changer material (HP-PCM) or thermal grease with a specified thermal conductivity λ_{grease}. Usually, $R_{th(j-c)}$ is given as a maximum value but $R_{th(c-s)}$ and $R_{th(j-s)}$ are given as typical values. If there is more than one switch in a package, the R_{th} is given for the switch with the highest value. The typical value is the average value of measurements from several of the worse switches.

7.5.3.2 Characteristics of body diode or integrated inverse diodes

Figure 7.5.7 from a SiC MOSFET module datasheet illustrates its reverse conducting (freewheeling diodes) characteristics with or without hybrid integrated SiC Schottky inverse diode. For modules without hybrid integrated diode, the characteristics of the MOSFETs body diode are shown.

Characteristics						
Symbol	Conditions		min.	typ.	max.	Unit
Integrated body diode						
$V_F = V_{SD}$	$-I_D$ = 124 A, V_{GS} = -4 V, chiplevel	T_j = 25 °C		4.6		V
		T_j = 150 °C		4.3		V
$V_{F0} = V_{SD0}$	chiplevel	T_j = 25 °C		3.8		V
		T_j = 150 °C		3.6		V
$r_F = r_{SD}$	chiplevel	T_j = 25 °C		6.4		mΩ
		T_j = 150 °C		5.6		mΩ
t_{rr}	V_{DD} = 600 V, $-I_D$ =240 A, V_{GS} =-4 V, R_{Gon} = 0.5 Ω, di/dt_{off} = 23 kA/µs	T_j = 150 °C		40		µs
Q_{rr}		T_j = 150 °C		6.7		µC
I_{rr}		T_j = 150 °C		337		A
E_{rr}		T_j = 150 °C		2.21		mJ

a)

Characteristics						
Symbol	Conditions		min.	typ.	max.	Unit
Inverse diode						
$V_F = V_{EC}$	I_F = 100 A	T_j = 25 °C		1.40	1.60	V
	chiplevel	T_j = 150 °C		1.80	2.10	V
V_{F0}	chiplevel	T_j = 25 °C		0.95	1.05	V
		T_j = 150 °C		0.80	0.90	V
r_F	chiplevel	T_j = 25 °C		4.5	5.5	mΩ
		T_j = 150 °C		10.0	12	mΩ
C_j	parallel to C_{oss}, f = 1 MHz, V_R = 800 V, T_j = 25 °C			0.42		nF
Q_c	V_R = 800 V, di/dt_{off} = 500 A/µs, T_j = 25 °C			0.33		µC
$R_{th(j-c)}$	per diode				0.24	K/W
$R_{th(c-s)}$	per diode (λ_{grease}=0.81 W/(m*K))			0.076		K/W

b)

Figure 7.5.7 Different datasheet values of inverse diode characteristics: a) SKM350MB120SCH15 (characteristics of the MOSFETs body diode; b) SKM350MB120SCH17 (characteristics of the hybrid inverse SiC SBD)

Forward voltage $V_F = V_{SD}$ of body diode or hybrid inverse diode

Typical or typical and maximum value of drain-source voltage drop on chip-level in reverse direction at specified V_{GS} (0V or slightly negative); forward current I_F and junction temperatures T_j = 25°C/150°C. While the forward voltage of the body diode has a negative temperature coefficient, this is positive for a hybrid integrated Schottky diode in the relevant current and temperature range.
To calculate the forward voltage across the main terminals, the voltage drops across the module lead resistors (bonding wires, terminals, ...) $R_{DD'+SS'}$ (explained under module layout characteristics) must be taken into account; when calculating chip losses, in contrast, this may be neglected. A positive gate-source voltage V_{GS} opens the MOSFET channel in reverse direction, which leads to a massive reduction of the reverse voltage, see diagram "Typ. reverse output characteristic, incl. $R_{DD'+SS'}$ in Figure 7.5.14.

Threshold voltage V_{F0} (V_{SD0}) and forward slope resistance r_F (r_{SD0}) of body diode or hybrid inverse diode

To calculate the inverse diode forward losses, the elements of an equivalent straight line are indicated in the datasheets: $V_F = f(I_F) = V_{F0} + r_F \cdot I_F$. Typical or typical and maximum values of V_{F0} and r_F are given at V_{GE} = 0V for junction temperatures T_j = 25°C/150°C. V_{F0} and r_F values included in the datasheet table refer to chip level.

Reverse recovery time t_{rr}, recovered charge Q_{rr}, peak reverse recovery current I_{RRM} and turn-off energy E_{rr} of the body diode (modules without hybrid inverse Schottky diode).

As with other pin diodes, the current, di/dt, and junction temperature all affect the reverse recovery behaviour of the MOSFET's bipolar body diode. Its dynamical characteristics - indicated in the module - datasheets are determined from a double pulse measurement in accordance with Figure 7.5.6 a).
In the tabular datasheet characteristics, t_{rr}, Q_{rr}, I_{RRM} and E_{rr} are given at maximum operational junction temperature $T_{j(op)}$, characterised by supply voltage V_{DD}, diode current I_F before commutation (in the range of I_{Dnom} of the SiC MOSFET), MOSFET turn-off gate control voltage $V_{GS(off)}$ and current slope di/dt_{off} . The following explanations refer to the times t_9...t_{10} shown in the Figure 7.5.8 with the measuring circuit shown in Figure 7.5.6 a).

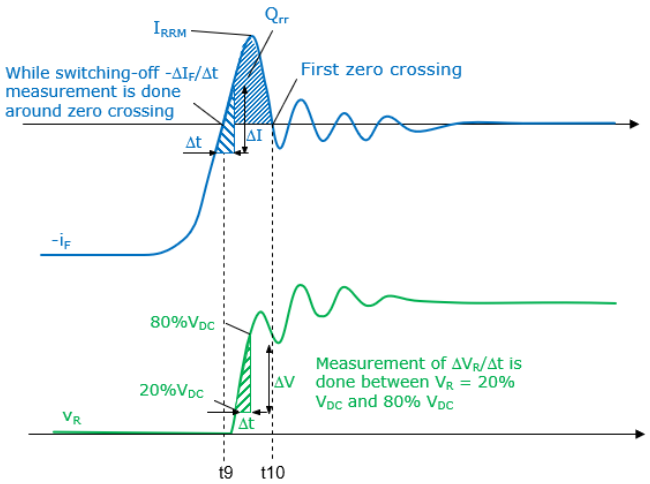


Figure 7.5.8 Dynamical characterisation of SiC MOSFET module's freewheeling diode

The reverse recovery time t_{rr} is the typical time required by the body diode for the transition from a specified forward current value $-I_D$ to reverse state (blocking DC supply voltage). It is measured in the interval from t_9 (zero-crossing of diode current to t_{10} (first zero level of reverse current).

Q_{rr} is the typical value of total recovered charge flowing after switchover from forward current I_F at to reverse blocking state during t_{rr} from the body diode to the outer circuit. It has to be taken up by the complementary MOSFET during turn-on.

$$Q_{rr} = \int_{t9}^{t10} -i_D\,(t)\,dt$$

The current I_{RRM} is the typical peak value of the reverse current after inverse diode switchover from the specified forward current value I_F to reverse state. E_{rr} is the typical turn-off energy of the inverse diode

$$E_{rr} = \int_{t9}^{t10} v_R\,(t)\,\cdot\,-i_D\,(t)\,dt$$

I_{RR}, Q_{rr}, and E_{rr} are highly dependent on temperature, the specification is made at the highest recommended junction operation temperature.

Junction capacitance C_j and stored charge Q_c of hybrid inverse Schottky barrier diode

For SiC MOSFET modules with integrated Schottky barrier inverse diodes (SBD), the switching energy in the body diode is specified as $E_{rr(MOSFET)}$ in the diagrams for the switching energies, see Figure 7.5.16 or Figure 7.5.17 b) below. In contrast, there are no significant switching losses in the SBD [7.54].
When switching, however, the junction capacitance C_j of the diode must also be charged in addition to charging the MOSFET's output capacitance C_{oss}:

$$E_{Cj} = \frac{1}{2}\cdot\left(C_{oss} + C_j\right)\cdot V^2$$

The SBD junction capacitance and the stored charge, specified in the module datasheet, describe its dynamic behaviour sufficiently.

Thermal resistances $R_{th(j-c)}$ and $R_{th(c-s)}$ respective $R_{th(j-s)}$ per hybrid inverse diode switch

The explanations given for the characteristic "Thermal resistances $R_{th(j-c)}$ and $R_{th(j-s)}$ per SiC MOSFET" also apply to hybrid integrated inverse diodes, provided the "SiC MOSFET" is replaced by "inverse diode" and P_T is replaced by P_D.
The datasheet values are given for a specified thermal interface medium. e.g. pre-applied High Performance thermal paste (HPTP), pre-applied phase changer material (HP-PCM) or thermal grease with a specified thermal conductivity λ_{grease}. Usually, $R_{th(j-c)}$ is given as a maximum value but $R_{th(c-s)}$ and $R_{th(j-s)}$ are given as typical values.

7.5.3.3 Module specific characteristics

The characteristic data to be assigned to the complete SiC MOSFET module are also illustrated in the tabular datasheet. Two examples are shown in Figure 7.5.9 (SEMITOP baseplate-less module) and Figure 7.5.10 (SEMITRANS baseplate module).

Characteristics					
Symbol	**Conditions**	**min.**	**typ.**	**max.**	**Unit**
Module					
L_{CE}			6		nH
M_s	to heatsink	1.6		2.3	Nm
w	weight		35		g

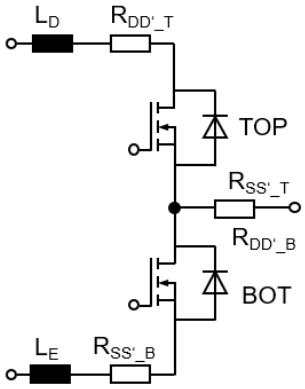
Figure 7.5.9 Module-specific characteristics for SEMITOP baseplate-less SiC MOSFET module SK250MB120CR03TE2

Characteristics						
Symbol	Conditions		min.	typ.	max.	Unit
Module						
L_{DS}				15		nH
$R_{DD'+SS'}$	measured per switch	T_C = 25 °C		0.55		mΩ
		T_C = 125 °C		0.85		mΩ
$R_{th(c-s)1}$	calculated without thermal coupling (λ_{grease}=0.81 W/(m*K))			0.011		K/W
$R_{th(c-s)2}$	including thermal coupling, T_s underneath module (λ_{grease}=0.81 W/(m*K))			0.015		K/W
M_s	to heat sink M6		3		5	Nm
M_t		to terminals M6	2.5		5	Nm
						Nm
w					325	g

Figure 7.5.10 Module-specific characteristics for SEMITRANS SiC MOSFET baseplate module SKM350MB120SCH17

Drain-source commutation inductance L_{DS} (also designated as L_{CE})

Sum of all (parasitic) stray inductances between drain- (TOP) and source (BOT) terminal determined from the inductive voltage drop measured during switching. The partial inductances L_D and L_S depicted in Figure 7.5.11 represent the total inductances of the bond connections and terminals. As Figure 7.5.9 and Figure 7.5.10 shows have modules with multiple solder or Press-fit PCB connections significantly lower parasitic inductances compared to modules with screw terminals.



$L_{DS} = L_D + L_S$

L_D and L_S might be coupled inductances

$R_{DD'-SS'} = \mathrm{Max}(R_{DD'\_T} + R_{SS'\_T};\ R_{DD'\_B} + R_{SS'\_B})$

Figure 7.5.11 Stray inductances and ohmic lead resistances of an IGBT module

Parasitic ohmic terminal-to-terminal lead resistances $R_{DD'+SS'}$

All partial resistances of one half-bridge module are pooled to obtain the terminal resistance $R_{DD'+SS'}$ indicated in the datasheet. Again, the partial resistances $R_{DD'}$ and $R_{SS'}$ depicted in Figure 7.5.11 also represent the sum of resistances of the bond connections and terminals. Because of the temperature dependence of the cooper leads, in the datasheets of module with screw terminals, the ohmic resistance $R_{CC'+EE'}$ is given at two case temperatures, e.g. at T_c =25°C/125°C. Because modules with direct solder or Press-fit PCB connections have very low ohmic terminal-to-terminal lead resistances this information is usually omitted from the datasheet of direct PCB-mountable modules (Figure 7.5.9).

Thermal resistance $R_{th(c-s)1}$ per SiC MOSFET module (modules with baseplate)

$R_{th(c-s)1}$ per module is calculated without thermal coupling of switches by a virtual parallel connection of all $R_{th(c-s)}$ of the module.

$$R_{th(c-s)1} = \left(\frac{n}{R_{th(c-s)T}} + \frac{n}{R_{th(c-s)D}}\right)^{-1}$$

n: number of switches per module
$R_{th(c-s)T}$: thermal resistance case-heatsink per MOSFET switch
$R_{th(c-s)D}$: thermal resistance case-heatsink per inverse diode switch (if available)

This theoretical value could be reached only if the distance between all switches is wider than 3 to 4 times the thickness of the material stack "chip-to-heatsink" (15mm…20mm), which is may be possible in chopper modules but not in halfbridge or 6pack configuration.

Thermal resistance $R_{th(c-s)2}$ per SiC MOSFET module (modules with baseplate)

The value of $R_{th(c-s)2}$ per module - valid for a typical distribution of power dissipation between the switches - includes thermal coupling. Both thermal resistances are specified with thermal interface material (λ = 0.81W/(m·K)) respective Semikron Danfoss pre-applied phase changer material. The reference point T_s is located underneath module.
Since an individual determination of $R_{th(j-c)}$ is not possible for SiC MOSFET baseplate-less modules the thermal resistances $R_{th(j-s)}$ per MOSFET and (if available) per diode switch are given. The thermal resistance is often specified with two different thermal interface materials. The $R_{th(j-s)}$ and $R_{th(c-s)}$ datasheet statement modules are valid only if the modules are mounted according to the mounting instructions using the specified TIM material and layer thickness.

Mechanical data Ms, M_t, w

The following mechanical data is provided in the datasheets:

- Mounting torque M_s of the fixing screws (minimum and maximum values)
- Mounting torque M_t of the terminals (only for modules with screw-terminals, minimum and maximum values)
- Module weight w (typical or maximum value)

Characteristics of an internal temperature sensor R_{ts}, R100, B100/125, tolerance

If available, at SEMITOP SiC MOSFET modules an NTC temperature sensor is positioned next to the chips on the DBC ceramic substrate, representing a temperature that is close to that of the heatsink.
The resistance of this "Negative Temperature Coefficient" sensor falls with rising temperature. In the datasheets, temperature sensor specifications include the internal resistance R_{100} at 100°C, for a measuring tolerance at 100°C and the coefficient B100/125 (typical value with specified tolerance), see Figure 7.5.12. The 100°C resistance value is closer to the interesting operating temperature with a lower tolerance value than the 25°C value R_{25} in that temperature range.

Characteristics					
Symbol	Conditions	min.	typ.	max.	Unit
Temperature Sensor					
R_{100}	T_r = 100 °C		493 ± 5%		Ω
$B_{100/125}$	$R_{(T)}=R_{100}\exp[B_{100/125}(1/T-1/T_{100})]$; T[K];		3550 ±2%		K

Figure 7.5.12 Temperature sensor specific characteristics of SK250MB120CR03TE2

The types of sensors used in specific products, as well as their properties are explained in details in chapter 3.2.8.1. and in the product group specific Technical Explanation, see also Table 7.3.8.

7.5.4 Diagrams

Similar to the sequence in the datasheets, this chapter provides information on the diagrams which generally refer to one SiC MOSFET or freewheeling diode switch or to the module's construction behaviour. Some diagrams presented here are not shown in all of the datasheets, as some are specific to certain product groups. Also, a different sequence is possible, individual diagrams may be missing or additional diagrams may be included.

Typical MOSFET forward output characteristics $I_D = f(V_{DS})$ including $R_{DD'+SS'}$

The diagram in Figure 7.5.13 illustrates the typical output characteristic for T_j = 25°C and 150°C in on-state region using parameter V_{GS}. Shown are the positive temperature coefficient of the drain-source on-state voltage $V_{DS(on)}$ and the decrease of this voltage in line with the increase in gate-source voltage V_{GS}. It In contrast to the tabular data, the diagrams illustrate the voltage drop across the module terminals; the V_{DS} value includes the voltage drops over the parasitic terminal resistances $R_{DD'+SS'}$.

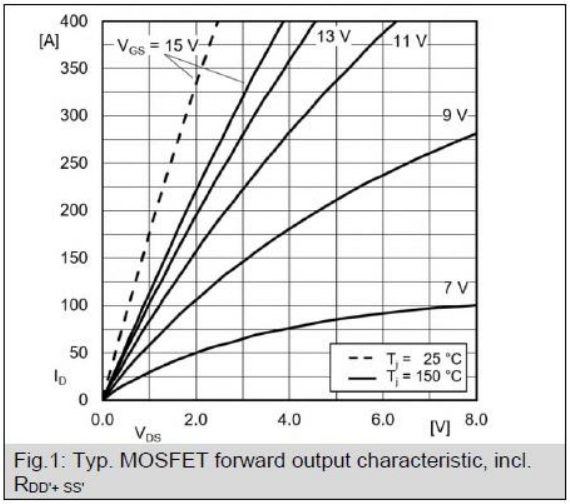


Fig.1: Typ. MOSFET forward output characteristic, incl. $R_{DD'+SS'}$

Figure 7.5.13 Typical MOSFET forward output characteristics $I_D = f(V_{GS})$ including $R_{DD'+SS'}$ of a SiC MOSFET module SK250MB120CR03TE2

Typical reverse output characteristic, incl. $R_{DD'+SS'}$

The diagram in Figure 7.5.14 shows the current-voltage characteristics $V_F = V_{SD} = f(-I_D)$ of body diode or the paralleling of body- and hybrid SBD inverse diode, typical or typical and maximum values of voltage drop in reverse direction across terminals at specified V_{GS} (from positive to slightly negative values); reverse current $-I_D$ and junction temperatures T_j = 25°C/150°C.
While the forward voltage of the body diode has a negative temperature coefficient, this is positive for a hybrid integrated Schottky diode in the relevant current and temperature range [7.55].
A positive gate-source voltage V_{GS} opens the MOSFET channel in reverse operation giving the switch a resistance characteristic similar to that in forward direction, see the left curve(s) in the diagrams "Typ. reverse output characteristic, incl. $R_{DD'+SS'}$ in Figure 7.5.14.

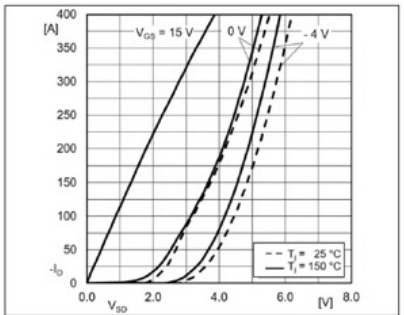


Fig. 1a: Typ. MOSFET reverse output characteristic, incl. $R_{DD'+SS'}$

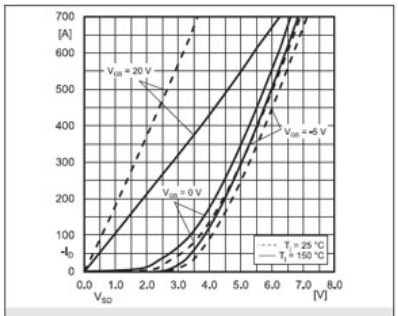


Fig. 2: Typ. reverse output characteristic, incl. $R_{DD'+SS'}$

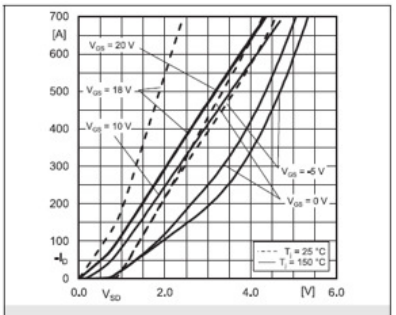


Fig. 2: Typ. reverse output characteristic, incl. $R_{DD'+SS'}$

a) b) c)

Figure 7.5.14 Typical MOSFET reverse output characteristics of three different SiC MOSFET modules: a) SK250MB120CR03TE2; b) SKM350MB120SCH15 [7.52]; c) SKM350MB120SCH17

Drain current I_D derating versus case temperature T_c

The Figure 7.5.15 shows the derating of the maximum continuous drain current I_D (without additional switching losses) which is required if the sink temperature T_s (baseplate-less modules) or case temperatures T_c (baseplate modules) differ from the reference temperatures 25°C, often given as a parameter for the maximum I_D in the datasheet table "Absolute Maximum Ratings". At sink resp. case temperatures above 25°C, the relation is:

$$I_D = \frac{(T_{jmax} - T_s)}{R_{th(j-s)} \cdot V_{DS(on)}} \qquad \text{(Baseplate-less modules)}$$

$$I_D = \frac{(T_{jmax} - T_c)}{R_{th(j-c)} \cdot V_{DS(on)}} \qquad \text{(Baseplate modules)}$$

At case or heatsink temperatures below 25°C, the maximum rated collector current is limited to the limit at 25°C.
In some diagrams for baseplate-less modules, the influence of different thermal interface materials is taken into account. Figure 7.5.15 a) show the rated drain current I_D as a function of the heatsink temperature for thermal paste Wacker P12 (λ_{paste} = 0.8W/(m·K) and for high-performance thermal paste or high-performance phase changer (λ = 2.5W/(m·K). In Figure 7.5.15 b) the rated drain current I_D as a function of the case temperature of a SEMITRANS 3 baseplate module is shown.

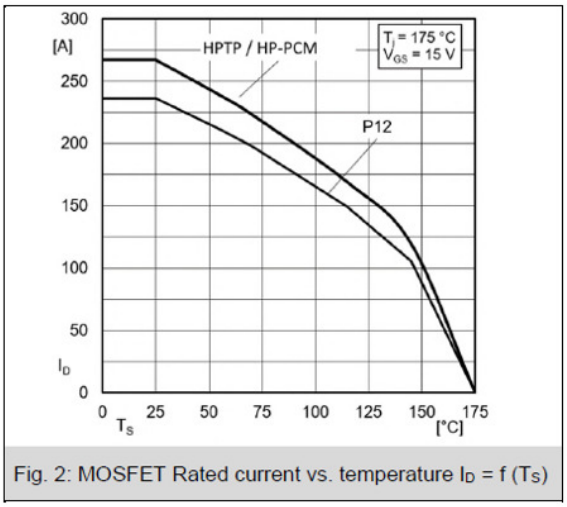


Fig. 2: MOSFET Rated current vs. temperature $I_D = f(T_S)$

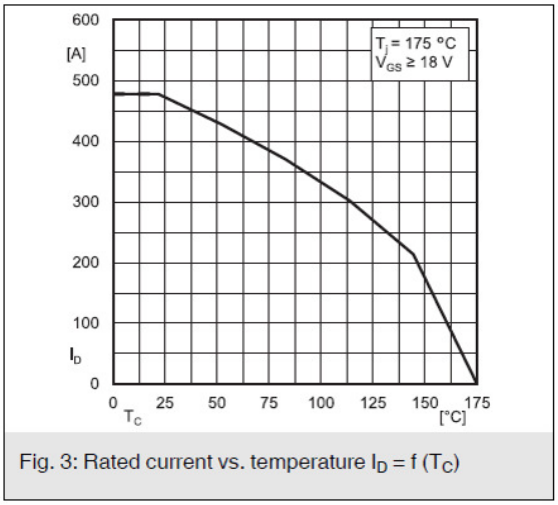


Fig. 3: Rated current vs. temperature $I_D = f(T_C)$

a) b)

Figure 7.5.15 Derating of drain current $I_D = f(T_s)$ or $I_D = f(T_c)$ for modules without and with baseplate: a) versus heatsink temperature T_s: for SK250MB120CR03TE2; b) versus case temperature T_c for SKM350MB120SCH17

Please note, that here the term case temperature T_s (T_c) refers to the heatsink (baseplate) temperature under the hottest chips. The maximum permissible frame temperature of the plastic case is significantly lower.

Typical switching energies E_{on}, E_{off} and E_{rr} as a function of the drain current I_D at two different R_G values

Figure 7.5.16 shows the typical turn-on / turn-off energies E_{on}, E_{off} of the SiC MOSFET as a function of the drain current I_D. Also shown is the drain current depended turn-off energy E_{rr} of the inverse diode used as a freewheeling diode as a function of I_D. The measurements were carried out at two high operating temperatures (T_j =125°C/150°C), a typical operation voltage V_{DD} (e.g. 600V for 1200V MOSFET or 900V for 1700V MOSFET) and the gate-source voltage range, used for the dynamic specifications in the table section of the datasheet. Switching losses and times of the MOSFET are almost independent from the junction temperature an exception is the body diode, because of its bipolar conduction mode.
Some data sheets contain two different diagrams for measurement results with 2 different gate resistors, R_{G1} and R_{G2} (Figure 7.5.16). R_{G1} (the lower values of R_{Gon}/R_{Goff}) are the gate resistors used to determine the switching characteristics listed in the tabular section. These values are applicable for applications with high switching frequencies but currents lower than 50% of the nominal current and/or low DC link voltages. The gate resistors R_{G2} (the higher values of R_{Gon}/R_{Goff}) significantly increases the SiC MOSFET switching losses but degreases the switching losses of the SiC MOSFET body diode. However, if currents in the $I_{D(nom)}$ range or higher are to be switched off, this is only possible with gate resistors similar to R_{G2}, without the SiC MOSFET being destroyed by the resulting switching overvoltage.

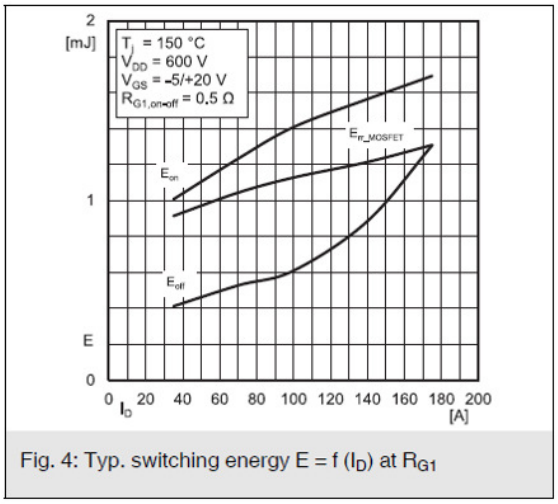


Fig. 4: Typ. switching energy E = f (I_D) at R_{G1}

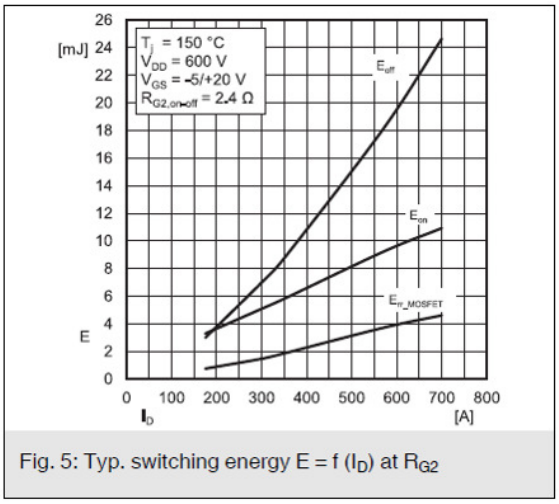


Fig. 5: Typ. switching energy E = f (I_D) at R_{G2}

Figure 7.5.16 Turn-on/turn-off/recovery energy E_{on}, E_{off} and E_{rr} = f(I_D) at different external gate resistances R_{G1} and R_{G2} of a SKM350MB120SCH17 with hybrid integrated SBC inverse diode whose own switching losses are neglected

Typical switching energies E_{on}, E_{off} and E_{rr} versus external gate resistances R_G

Figure 7.5.17 shows - for different external gate resistances R_G - the typical turn-on / turn-off energies E_{on}, E_{off} and E_{rr} of the SiC MOSFET and its body diode at two typical high-current operating points. The measurement was carried out at the highest recommended operating temperature, a typical working voltage V_{CC} (e.g. 600V for 1200V MOSFET or 900V for 1700V MOSFET IGBT and the further conditions under which the typical switching energies are specified in the table section of the datasheet. Different Diagrams are given for different drain current levels I_{D1} and I_{D2} in some cases.

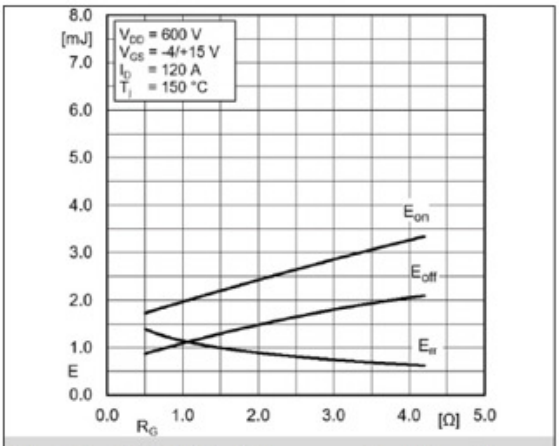


Fig. 4: Typ. MOSFET switching energy E = f (R_G) at I_{D1}

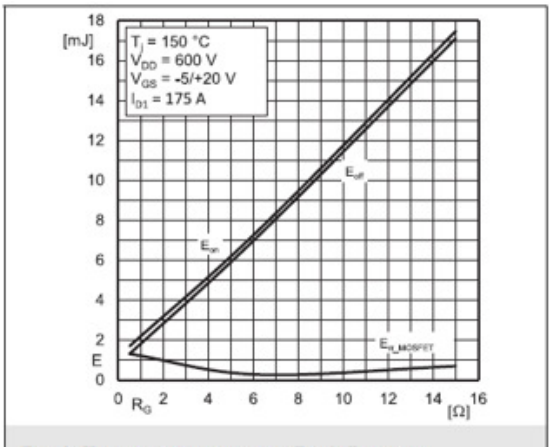


Fig. 6: Typ. switching energy E = f (R_G) at I_{D1}

a) b)

Figure 7.5.17 Turn-on/turn-off/recovery energy E_{on}, E_{off} and E_{rr} = f(R_G) a) SK250MB120CR03TE2; b) SKM350MB120SCH17 with hybrid integrated SBC inverse diode whose own switching losses are neglected (exemplarely for I_{D1})

Typical transfer characteristic I_D = f(V_{GS})

The typical transfer characteristic in Figure 7.5.18 describes the behaviour of the SiC MOSFET in the active operating area at V_{DS} = 20V (linear operation). The drain current is coupled with the gate-source voltage via $I_D = g_{fs} \cdot (V_{GS} - V_{GS(th)})$

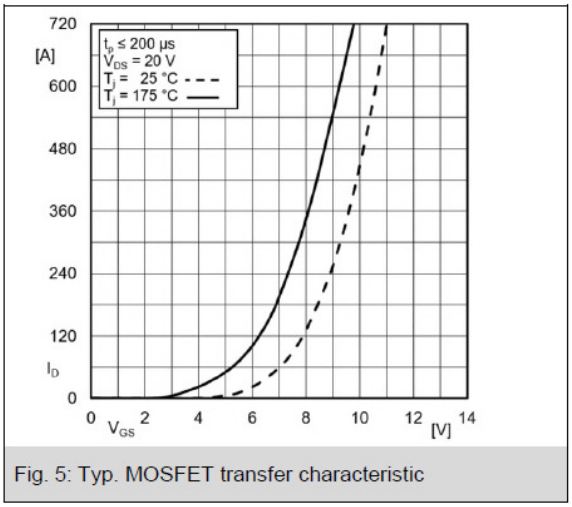


Fig. 5: Typ. MOSFET transfer characteristic

Figure 7.5.18 Typical MOSFET transfer characteristic $I_D = f(V_{GS})$ of a SiC MOSFET module SK250MB120CR03TE2

Typical MOSFET gate charge characteristic $V_{GS} = f(Q_G)$

Figure 7.5.19 shows the typical dependency of the SiC MOSFET gate-source voltage V_{GS} on the gate charge Q_G at a typical working voltage V_{DD} (e.g. 800V for 1200V SiC MOSFET). The gate charge characteristic illustrates the course of V_{GS} between off-state at a conventional negative gate-emitter voltage V_{GS} and on-state at maximum permissible V_{GS}.

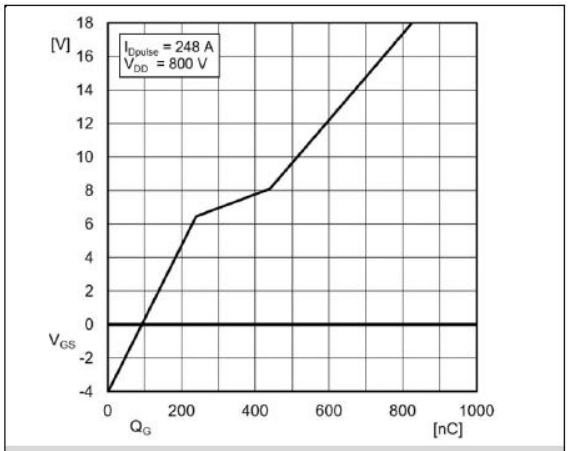


Fig. 6: Typ. MOSFET gate charge characteristic

Figure 7.5.19 MOSFET gate charge characteristic $V_{GS} = f(Q_G)$ of a SiC MOSFET module SK250MB120CR03TE2

Typical dependencies of the switching times $t_{d(on)}$, t_r, $t_{d(off)}$ and t_f on drain current I_D

Figure 7.5.20 shows the switching times $t_{d(on)}$ (turn-on delay time), t_r (rise time), $t_{d(off)}$ (turn-off delay time) and t_f (fall time) as a function of the collector current I_C. The measurements were carried out at two high operating temperatures (T_j =125°C/150°C), a typical operation voltage V_{DD} (600V/900V for 1200V/1700V MOSFET) and the gate-source voltage range, used for the dynamic specifications in the table section of the datasheet.
Some data sheets contain two different diagrams for measurement results with 2 different gate resistors, R_{G1} and R_{G2} (Figure 7.5.20). R_{G1} (the lower values of R_{Gon}/R_{Goff}) are the gate resistors used to determine the switching characteristics listed in the tabular section.

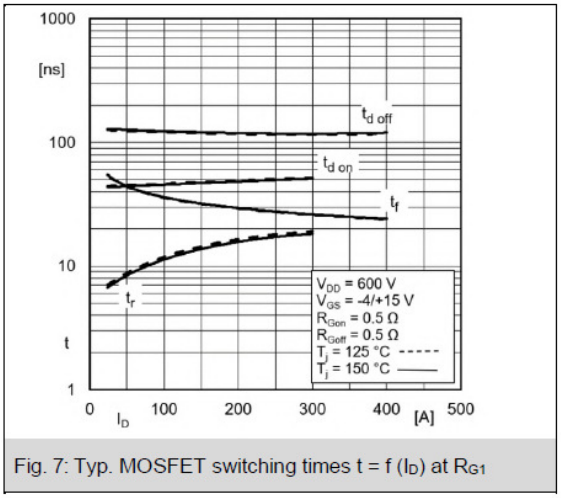


Fig. 7: Typ. MOSFET switching times t = f (I_D) at R_{G1}

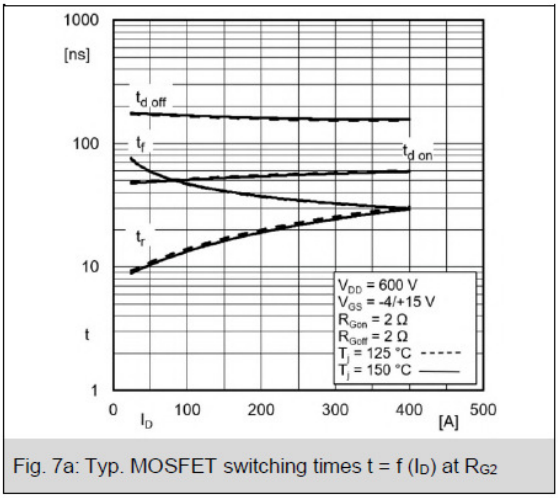


Fig. 7a: Typ. MOSFET switching times t = f (I_D) at R_{G2}

a) b)

Figure 7.5.20 SK250MB120CR03TE2 SiC MOSFET switching times versus collector current at different external gate resistances R_{G1} and R_{G2}

Typical dependencies of the switching times $t_{d(on)}$, t_r, $t_{d(off)}$ and t_f on the external gate resistance R_G

The measurement in Figure 7.5.21 was carried out at the highest recommended operating temperature at a typical working voltage V_{CC} (600V/900V for 1200V/1700V MOSFET) and at different drain currents I_{D1} and I_{D2} as a function of the external gate series resistances R_G.

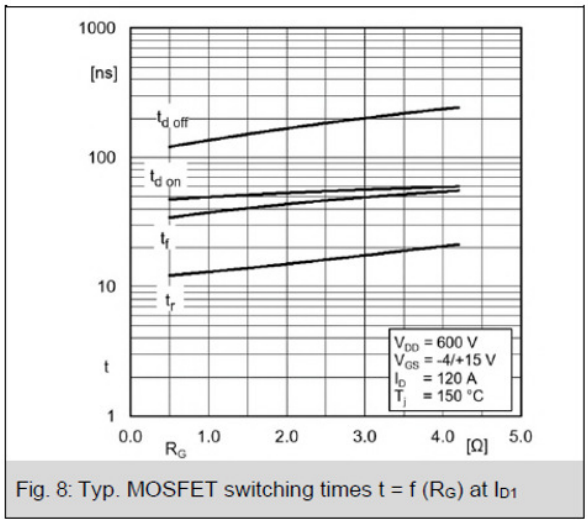


Fig. 8: Typ. MOSFET switching times t = f (R_G) at I_{D1}

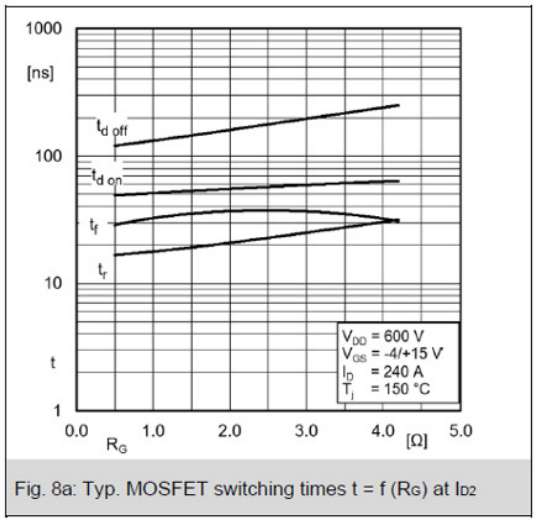


Fig. 8a: Typ. MOSFET switching times t = f (R_G) at I_{D2}

Figure 7.5.21 SK250MB120CR03TE2 SiC MOSFET switching times versus gate resistance R_G at different drain currents I_{D1} and I_{D2} versus external gate resistance

Typical transient thermal impedances $Z_{th(j-s)}$ or $Z_{th(j-c)}$ of IGBT and inverse or freewheeling diode in single-pulse operation as a function of the pulse duration t_p.

The diagrams on Figure 7.5.22 a) shows the thermal impedances $Z_{th(j-s)}$ between MOSFET switch and heatsink of a baseplate-less SiC MOSFET module. The two curves demonstrate the dependence of $Z_{th(j-s)}$ of baseplate-less modules on the thermal conductivity λ of the TIM.

The diagram on Figure 7.5.22 b) shows the thermal impedances $Z_{th(j-c)}$ between switch and module baseplate for MOSFET and inverse diode.

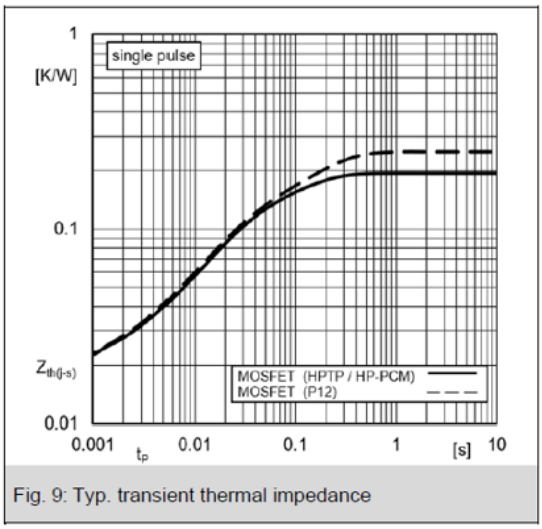


Fig. 9: Typ. transient thermal impedance

a)

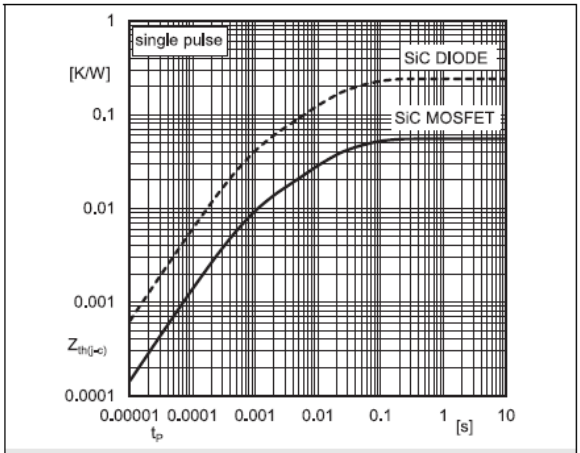


Fig. 14: Transient thermal impedance

b)

Figure 7.5.22 Transient thermal impedances: a) $Z_{th(j-s)}$ per switch of SK250MB120CR03TE2; b) $Z_{th(j-c)}$ for SiC MOSFET and hybrid integrated inverse diode switch of SKM350MB120SCH17

The thermal impedances for single-pulse operation depicted in Figure 7.5.22 characterise the increase in chip temperature during a specified power dissipation pulse in relation to the baseplate temperature ($Z_{th(j-c)}$) or heatsink temperature ($Z_{th(j-s)}$). After the chip temperature has a quasi-static value, $Z_{th(j-c)}$ resp. $Z_{th(j-s)}$ will reach their static end values $R_{th(j-c)}$ resp. $R_{th(j-s)}$, listed in the table section of datasheet too.

Typical peak reverse recovery current I_{rr} of MOSFET body diode versus current slope – di_F/dt of the forward current I_F

Figure 7.5.23 shows typical ratings of the peak reverse recovery current I_{RR} of the MOSFET's body diode, applicable to modules without inverse integrated Schottky diodes. The measurement was carried out at the highest recommended operating temperature at a typical working voltage V_{CC} (600V/900V for 1200V/1700V MOSFET) and at high freewheeling diode forward current I_{SD}.

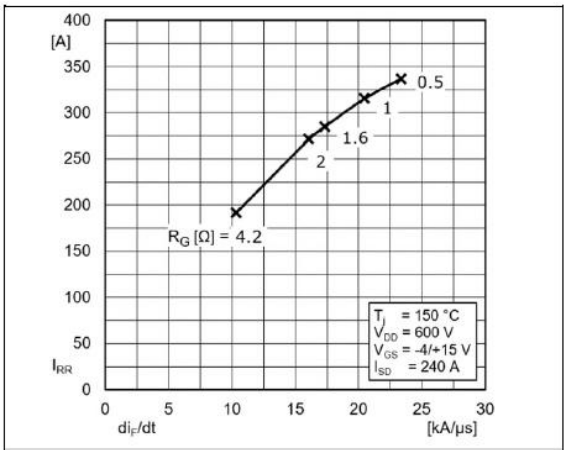


Fig. 10: Typ. body diode peak reverse recovery current $I_{RR} = f(di_F/dt)$

Figure 7.5.23 Peak reverse recovery current I_{rr} of the body diode in a SiC MOSFET SK250MB120CR03TE2

At fixed conditions for V_{GS}, the turn-on speed of the commutating MOSFET (di_D/dt) determines the $-di_F/dt$ of the diode in dependence of the MOSFET gate series resistances R_G. For easy dimensioning, ratings for external R_G (R_{Gon}) of the MOSFET are assigned to the di_F/dt values in this diagram. The peak reverse recovery current of the freewheeling diode increases in proportion to drain current and $-di_F/dt$.

SiC MOSFET Reverse Bias Safe Operating Area (RBSOA)

In the typical case of fast switching of ohmic-inductive load (hard switching applications), the SiC MOSFET module has to reach a virtually rectangular characteristic i = f(v) between DC working voltage V_{DD} and load current I_L, expanded e.g. by the non-ideal properties of freewheeling diode and the inductive overvoltage at the power circuits and module's parasitic inductances.
The diagram in Figure 7.5.24 describes the permitted operating conditions at MOSFET turn-off (RBSOA) at chip level (dashed line) and at the module terminal's level (continuous line).

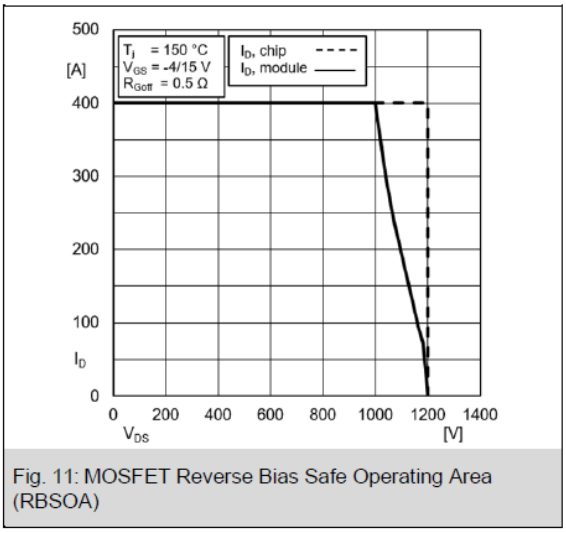


Fig. 11: MOSFET Reverse Bias Safe Operating Area (RBSOA)

Figure 7.5.24 MOSFET RBSOA of SK250MB120CR03TE2

Owing to the voltage induced at the parasitic module inductances L_{DS} during turn-off, the permitted voltage V_{DS} during turn-off decreases in dependence of the collector current and the permissible DC link voltage V_{DD} is reduced for high currents. Under the specified switching conditions (V_{GS}, R_G), the SiC MOSFET module SK250MB120CR03TE2 must not exceed V_{DS} = 1000V (on terminal level) at operation to almost 1.8 times the nominal drain current I_D at T_j = 150°C.
In a real application, this derating is strongly depending on system related parameters, like stray inductance of the DC link and the current commutation slope during the switching transitions, dependent by the gate driver properties. Therefore, in the datasheet specifications, the current commutation slope is defined via a specific gate resistor R_{Goff} and a specific gate voltage range $\pm V_{GS}$. Also, the stray inductance L_s of the commutation circuit and/or the collector current slopes are defined in the "MOSFET characteristics" datasheet table.

Typical characteristic of the internal capacitances versus drain-source voltage

The causes and effects of internal capacitances in power MOSFET have been thoroughly discussed in chapter 2.5.
The ratings given in the datasheet tables "MOSFET characteristics" and in Figure 7.5.25 show the dependency of the low-signal capacitances of a SiC MOSFET in off-state on the drain-source voltage V_{DS}. These are only of minor importance for the module selection, which should rather to be done on the basis of the SiC MOSFET gate charge diagram depicted in Figure 7.5.19.

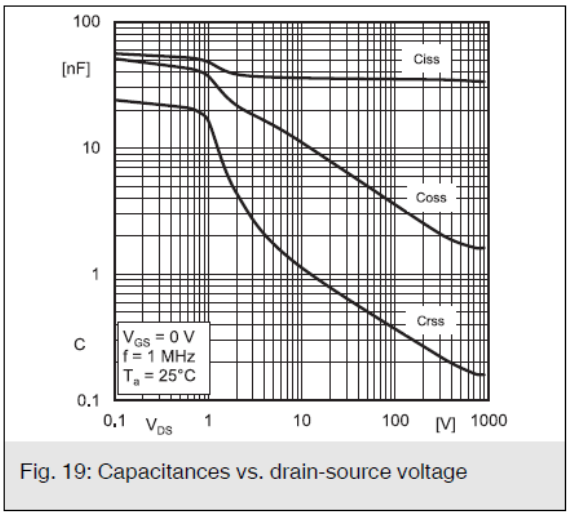


Fig. 19: Capacitances vs. drain-source voltage

Figure 7.5.25 Characteristic of internal capacitances as a function of drain-source voltage for SKM350MB120SCH17

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8 Application Notes for Thyristors and Mains Diodes

8.1 Thyristor, diode and thyristor/diode power module selection

8.1.1 General information

Thyristor/diode modules or discrete thyristors and diodes can be selected on the basis of the data sheet information and the explanations in chapter 7.2.
When selecting for a specific application, especially the following aspects have to be taken into account:

- Blocking behaviour,
- Current capability at operation in continuous duty, with short-time or intermittent load under the achievable cooling conditions (cf. chapter 6),
- Service life and reliability under the aspect of the expected temperature and load cycles (cf. chapter 4),
- Reliability under the aspect of expected cosmic radiation exposure (cf. chapter 4.5.5).

These aspects must be included into considerations for all stationary and short-time operating conditions. The maximum rated values given in the datasheets for blocking voltage, peak current and junction temperature must not be exceeded as a result of stresses under any static or dynamic conditions. The same applies to the limits specified for the case, e.g. vibration and shock resistance, resistance to extreme climatic conditions, insulation voltage in modules and assembly and mounting instructions.
To achieve a high degree of reliability and sufficient service life, the power devices thermal and mechanical behaviour must factor in the intended number of power cycles at which notable temperature cycles occur (see also [8.1]).

8.1.2 Reverse and forward blocking voltage

When selecting diodes and thyristors, it must be considered that the voltage limit values V_{DRM}, V_{RRM}, V_{DSM} and V_{RSM} listed in the data sheets are defined as peak values. For thyristors, these values are specified for an open (not connected) gate terminal.
Even with the highest possible voltage stress (upper mains voltage tolerance limit plus overvoltage), the maximum permissible voltages V_{RSM}, V_{RRM}, V_{DSM} and V_{DRM} must not be exceeded; see explanations to Figure 7.2.6 according to the definitions in IEC 60747-6 [8.2].
For use at very low temperatures, it must be considered that the blocking voltages are specified for temperature ranging from 25°C to T_{jmax}. Due to the positive temperature coefficient of the breakdown voltage, this decreases with T_j by about 0.11%/K. In contrast the reverse currents decrease with temperature T_j by about $0.96^{(Tjmax-Tj)}$, as well as does the risk of unintended trigger.
Expected overvoltage and sensible overvoltage protection measures determine not only the projected service life of the device (e.g. FIT rate as a function of cosmic radiation), but also the voltage headroom required for semiconductor selection. To withstand operational overvoltage, thyristors and diodes are operated at supply voltages V_V, of which the peak value is not higher than the peak reverse voltage divided by a safety factor k. For industrial applications on low-voltage mains supply, k should be selected in the range of 1.5 to 2.5.

$$\sqrt{2} \cdot V_V = V_{DWM} = \frac{V_{DRM}}{k} \quad \text{resp.} \quad \frac{V_{RRM}}{k}$$

A low safety factor is applied when the expected voltage stress is basically known, for example when a rectifier bridge is connected to DC-link via small inductance. For converters in low-voltage supply networks with unknown overvoltage, safety factors of 2 to 2.5 are recommended, depending on the available blocking voltage classes of the diodes and thyristors (Table 8.1.1).
The safety factor considers the rated line input voltage including a tolerance of e.g. +10%) and transient overvoltage, provided these are not reduced by line filters, DC link capacitors and protective devices, e.g. RC snubber networks, varistors or TVS-diodes.

Line Input Voltage V_V [V]	Rectifier Connection	Direct Output Voltage V_{di0} [V]	Peak Voltage $\sqrt{2} \cdot V_V$ [V]	Recommended Blocking Voltages V_{DRM}, V_{RRM} [V]	Safety factor k
125	Line-Neutral	110	177	600	3.39
230	Line-Neutral	202	325	800	2.46
400	Line-Line	540	566	1400	2.47
480	Line-Line	648	679	1600	2.36
500	Line-Line	675	707	1800	2.54
575	Line-Line	776	813	2000	2.46
600	Line-Line	810	848	2000	2.36
660	Line-Line	891	933	2200	2.36
690	Line-Line	932	976	2200	2.25

Table 8.1.1 Recommended blocking voltages for thyristors and rectifier diodes depending on the rated voltage of the supply (Line-Neutral: single-phase circuit; Line-Line: three phase circuit)

In DC-application such as the use of thyristors as crowbars, manufacturers recommend for the DC voltage not to exceed 50% of V_{DRM} (resp. V_{RRM} for rectifier diodes). More detailed information on voltage ratings of power semiconductors for example can be found in [8.3].

8.1.3 Operation in continuous duty, with short-time and intermittent load

To achieve a high degree of reliability and sufficient service life, the performance of thyristor/diode modules must factor in the intended number of power cycles at which notable temperature cycles occur. Furthermore, "serious" dimensioning is generally not based on the thermal capacity of the power devices up to the limit value T_{jmax} in order to leave a safety margin for cases that have not been considered in theory and for module ageing. The methods for thermal dimensioning for different applications and load cases are described in detail in chapter 6.

8.1.4 Operation at higher frequencies

In line applications, the switching losses of diodes and thyristors with about 1...2% of the conducting losses at 50Hz are negligible and are thus covered by the design reserves. For this reason, the data sheets of thyristors or diodes for mains applications do not normally contain any information on switching losses.
If diodes or thyristors for line application are operated at frequencies above 50Hz, the switching losses increase by about 2% per 50Hz. For frequencies above 200Hz, the additional losses must be considered in the dimensioning. For frequencies above 500Hz, diodes and thyristors for mains applications are not suitable. More detailed information on calculation of thyristor switching losses can be found, e.g. in [8.4].

8.2 Parallel and series connection in mains applications

8.2.1 Parallel connection

Different current levels in parallel diode or thyristor branches contribute to an unbalanced distribution of losses and thus account for different temperatures in the paralleled devices. A higher device temperature will finally lead to a reduction of service lifetime. The general target for parallel operation is therefore to reduce the differences between the branches as much as possible to ensure that the devices share the load current as evenly as possible.

- To prevent thermal overload caused by unbalanced current distribution, firstly the following countermeasures are required:
- Mechanically symmetric layout with thyristor modules coupled electrically as symmetrical as possible. Parasitic resistances in the busbars support current symmetry.
- Thermally symmetric layout with thyristor/diode modules good thermal coupling so that temperature differences between the devices stay as small as possible.

For parallel connection of diodes or thyristors in mains application the on-state voltage spread is normally the most critical parameter since it has a large influence on the static current sharing. Forward or on-state voltage binning could be made by the manufacturer, however, this procedure is associated with considerable additional logistical effort and financial expenses. Especially when thyristor/diode modules are considered, which comprise two devices in a half-bridge configuration, a binning would have to be at least two dimensional, which increases the effort beyond the practically acceptable limit. In the medium power range - the preferred field of power modules application - this procedure is therefore not common.

The existence of a multitude of influencing factors on the temperature distribution of parallel chips reduces the statistical probability of occurrence for unfavourable combinations of modules as discussed before. Typical statistical distributions in realistic module productions lots reduces the probability of critical combinations even further. Based on this realistic variation, the application-specific cooling conditions and a current derating in the range of typically 10% to 20%. The established numerical methods must then be used to check whether the static current distribution between the parallel devices meets the requirements.
For thyristors additional concern arises from the trigger characteristic of this devices. In the temporary low-current range, the current unbalance of parallel thyristors can be very high, as this is essentially determined by the thyristor's threshold voltage, which has a strongly negative temperature coefficient. Although this does not result in a thermal overload, the latching current or holding current in one or more parallel thyristors may be undershot. Measurements as described in [8.5] have shown that the resulting values of parallel connected thyristors can be up to 8 times higher than the values for a single thyristor. To prevent an unequal trigger, the following additional countermeasures are required:

- Mechanically and thermally symmetric layout, see above. However, it is advantageous for retrigger of undershot thyristor(s) not to connect the cathode connections of parallel thyristor modules directly but at a central point in order to realise a small balancing resistance. A further measure is using inductances in series with the thyristors in order to achieve even current distribution between paralleled thyristors as shown in Figure 8.2.1 below.
- Appropriate gate trigger with synchronous, steeply rising and high current pulses (min. 110% of the sum of required gate trigger currents of each individual thyristor, continuous sequence of trigger pulses during the whole conduction periods to force a proper retriggering of turned off thyristors). Also, the main cause of different turn-on times are differences in the turn-on delay times between the paralleled thyristors. The higher the gate current, the smaller these differences are.
- Compensation of tolerances and the temperature dependence of the trigger voltages and currents by providing as 'possibly ideal' current feed into each gate via separate gate series resistors.

Owing to the unavoidable variation in trigger delay times, parallel thyristors will never trigger absolute simultaneously. For this reason, in parallel thyristor assemblies, suitable measures are needed to prevent snubber capacitances (cf. chapter 8.4.2) of the remaining thyristor(s) from discharging through the thyristor that triggers first since this could lead to destruction. A measure is using inductances in series with the thyristors in order to achieve even current distribution between paralleled thyristors (Figure 8.2.1).

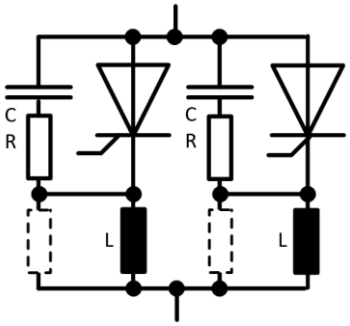


Figure 8.2.1 Single switch snubber circuit for parallel connected thyristors using series inductances

The series inductances L - in combination with the RC snubber - are particularly effective in limiting the peak values, even in the rate of rise of overvoltage. This is very important, especially in converters in six-pulse bridge configuration. At the same time, these series inductances prevent the snubber capacitors of the remaining parallel thyristors from discharging via the thyristor that triggers first. This is why the use of series reactors does not normally require an auxiliary bridge. To attenuate oscillations, a resistor is often connected in parallel to the series inductance. More detailed information on the parallel connection of diodes and thyristors for mains applications can be found in [8.5] to [8.10].

8.2.2 Series connection

To increase the blocking-state voltage, diodes or thyristors with the same blocking voltage may be connected in series. However, a series connection will normally contain components that differ slightly in reverse current, breakdown voltage and dynamic turn-off characteristics.
In most cases (possibly excluding avalanche diodes) homogenous voltage distribution has to be forced:

- for blocking-state symmetry by using parallel resistors,
- for symmetrical commutation by using parallel RC snubbers,
- for symmetrical trigger of thyristors by using suitable, powerful trigger circuits.

Furthermore, a "voltage oversizing" of each series connection "string" is required.
For example, in case of series connected avalanche diode "strings", it is customary to allow a voltage safety margin of 2.4 to 3 between the rated repetitive voltage $n \cdot V_{RRM}$ of the string and the applied peak reverse voltage.
If parallel resistors are used with the diodes or thyristors, they are to be rated so that the current that flows through the resistors is 5…10 times the leakage current at the applied voltage in hot state. Note that this current is factors lower than the I_{DD}, I_{RD} value in the datasheet at maximum blocking voltage.
The dynamic sharing of the reverse voltages during the commutation process is supported by RC snubber circuits in parallel with the individual diodes or thyristors in the series connection, cf. chapter 8.4.2. In practice, the diodes or thyristors will show a spread of reverse recovery charge Q_{rr}, the fastest component having a low Q_{rr} and the slowest component having a high Q_{rr}. It should be noted here that the reverse recovery charge is dependent upon the commutating current, the rate of commutation and the junction temperature.
Owing to the variation in reverse recovery time, the single switch that blocks first is at risk of having to take up a high voltage that is not permissible for a single switch alone. With series connected thyristors, there is an additional risk: directly before firing, the thyristor that goes over into on-state last might have to take up an inadmissibly high forward voltage that would result in uncontrolled "break-over" and may damage the thyristor.
Both risks must be ruled out using a RC snubber circuit. The snubber component values can initially be estimated using the dimensioning guidelines given for single-switch RC snubber circuits, described in chapter 8.4.2.
With ΔQ_{rr} is the maximum difference in reverse recovery charge between the devices and ΔV is the permissible difference in blocking voltage, the required snubber capacitance C can be estimated as $C = \Delta Q_{rr} / \Delta V$. The value of resistance R should be sufficient to overdamp the snubber circuit, see also explanations in chapter 8.4.2.2 and 8.4.2.3 below.
The recommended capacitance, however, is double the value calculated in this way. In addition to this "dynamic voltage distribution", static voltage distribution by means of parallel resistors is needed. These resistors can be selected such that a current roughly the size of the maximum rated reverse current specified in the datasheet for the thyristor or diode flows through each resistor.
The voltage increases over the stationary voltage that occurs when the last thyristor triggers or the first switch blocks can be seen in Figure 8.2.2.

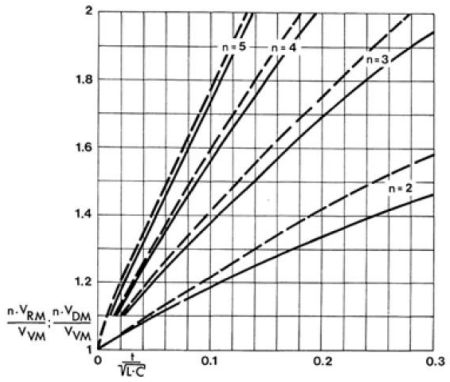


Figure 8.2.2 Time characteristic of the voltages V_{DM} or V_{RM} across the thyristor triggered last (___) and turned off first (- - - -) for n series connected thyristors (V_{VM}: Crest value for total terminal voltage, L: Inductance in the commutation circuit, C: Thyristor snubber capacitance).

More detailed information on the series connection of diodes and thyristors for mains applications can be found in [8.6], [8.10] and [8.11].

8.3 Trigger circuits for thyristors

8.3.1 Requirements for trigger pulses

Trigger pulse amplitude

The gate trigger characteristics, described in [8.12] and chapter 7.2.3 specifies the basic values within which gate-cathode voltage and gate current must lie for safe firing. It also explains why – and under which conditions - the "extreme curves" $v_G(i_G)$ are very far apart and why the maximum gate-cathode voltage required for triggering, may be higher than the steady-state value given in the datasheets.
In the case of insufficient driving voltage or too high a driver output resistance, the temporary counter voltage of the semiconductor may suppress or even temporarily reverse the gate current (Figure 8.3.1). This may damage the thyristor. The driver dimensioning must therefore comply with the power requirements.

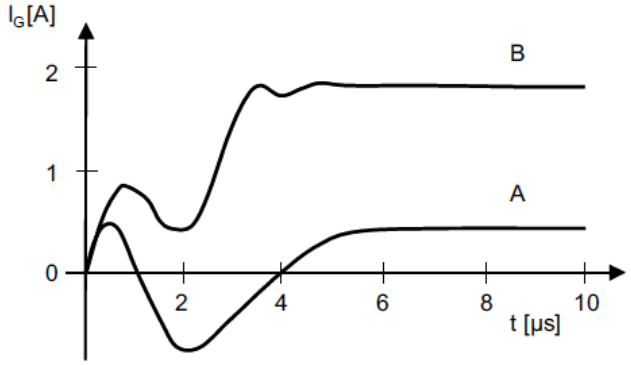


Figure 8.3.1 Gate current versus time: Thyristor triggered by an insufficiently (curve A) and a sufficiently designed (curve B) gate driver

To determine the resultant peak current for a gate driver with known values for short-circuit current ($I_K \sim V_B/R$) and no-load voltage ($V_0 \sim V_B$), the output characteristic determined from these values is entered into the trigger current / trigger voltage diagram (Figure 7.2.22 in chapter 7.2.4) for the type of thyristor to be fired. In Figure 8.3.2 the same diagram is shown in a linear scheme for better understanding.

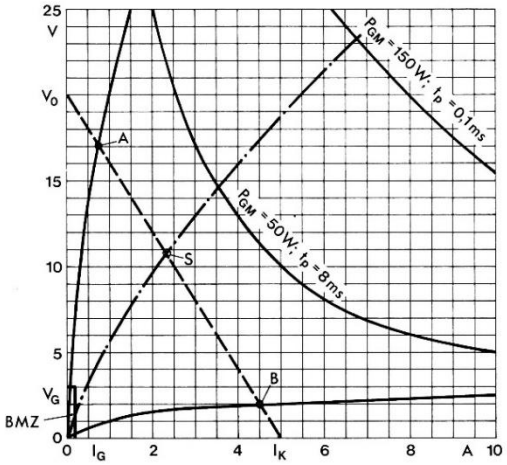


Figure 8.3.2 Gate current (I_G) – gate-cathode voltage (V_{GC}) characteristic of a thyristor in linear scheme and dotted driver output characteristic (load line V_0 = 20V, R_G = 4Ω)

The actual input characteristics for the individual thyristors of the given type lie between the limiting characteristics in the diagram (dash-dotted line). Accordingly, the possible points of intersection with the output characteristic of the driver is between points A and B. The point of intersection of S with the output characteristic of the driver device results from the resulting firing pulse data, e.g. 2.3A; 10.7V.

Trigger pulse shape

Although a 10µs-long gate current pulse is sufficient to trigger a thyristor under laboratory conditions and with resistive load, the real requirements in practice can be significantly higher.

The shape, amplitude and duration of the trigger pulse must be adapted to:

- the specific control characteristics of the thyristor (control characteristics or data sheet values for V_{GD}, V_{GT}, I_{GD}, I_{GT}, $P_{GM}(t_p)$, t_{gd}, t_r),
- the operating temperature range, since I_{GT} increases at low temperatures,
- the progress of the load current rise (reaching I_L, possible current drop below I_H).

Both the critical rate of on-state current $(di/dt)_{cr}$ and trigger characteristics - given in the data sheets (cf. chapters 7.2.2.1 and 7.3) - are validated with trigger pulses according to Figure 8.3.3. The effects of improper gate current pulses or excessive di/dt are described in [8.12], for example.

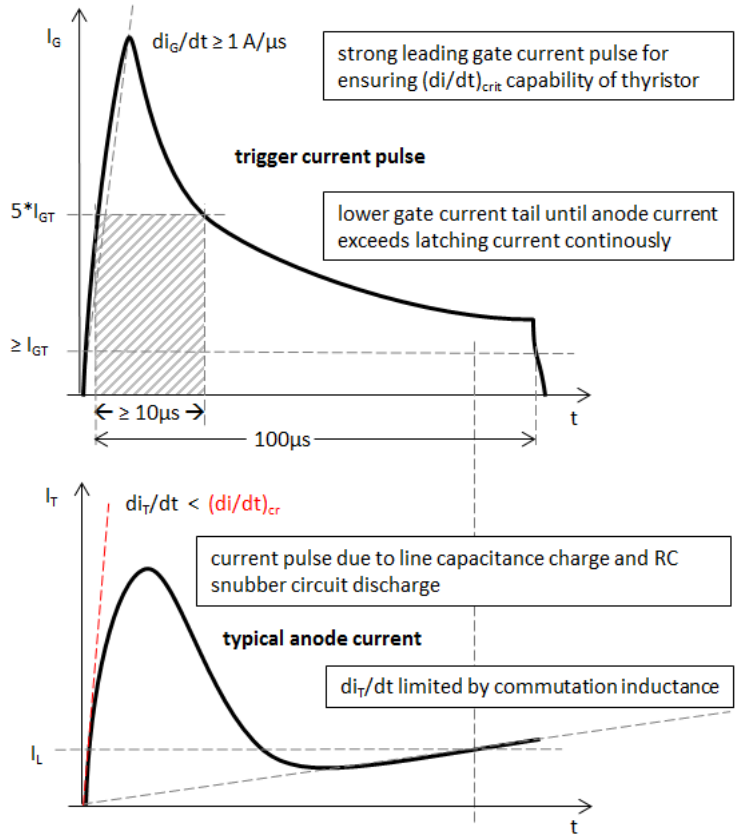


Figure 8.3.3 Recommended trigger current, used to validate Semikron Danfoss thyristors and general course of the load current with inductive load and snubber wiring

As it is expensive in practice to produce high and long trigger pulses, compromise solutions are often used. In general, the trigger pulse should be at least high ($\approx 5 \cdot I_{GT}$) or long ($\geq$ 20µs), but in any case, show a steep increase ($\geq$ 1A/µs) and last at least until reaching I_L. Longer and higher trigger pulses reduce I_{GT} and I_L and increase the thyristor (di/dt)-capability.
In order to trigger thyristors with small and economic trigger transformers using pulse lengths of a few milliseconds, oftentimes a "pulse train" or “picket fence” triggering as shown in Figure 8.3.4 is used, consisting of a 10µs current peak, a short constant current phase and 5…40kHz square wave pulses for the rest of the duty cycle. If a flyback converter is used, these pulses can easily be controlled by means of current control. It is also possible to use a monostable multivibrator or a microcontroller to generate the trigger pulse sequence. Further information can be found in [8.13].

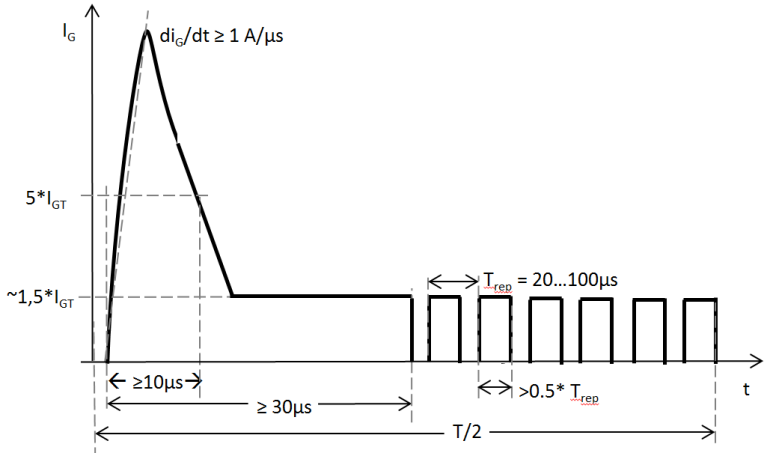


Figure 8.3.4 Gate trigger current for a "pulse train" or "fence" triggering

For rectifiers with reversing voltage and AC controllers with inductive load, each thyristor cannot fire until the instantaneous value of the supply voltage is higher than that of the reverse voltage. In order to achieve safe commutation, trigger pulses of up to 10ms might be required at 50Hz. In fully controlled 3-phase rectifier bridges (B6C) and in the case of continuous current flow the thyristors have current conduction angles of 120°. In the case of discontinuous current or indirect commutation via a freewheeling diode, each current block is divided into two blocks with a 60° current conduction angle. The trigger circuit must therefore deliver double pulses with a distance of 60°. Figure 8.3.5 illustrates this with simulated currents in phase L1 and thyristor V4.

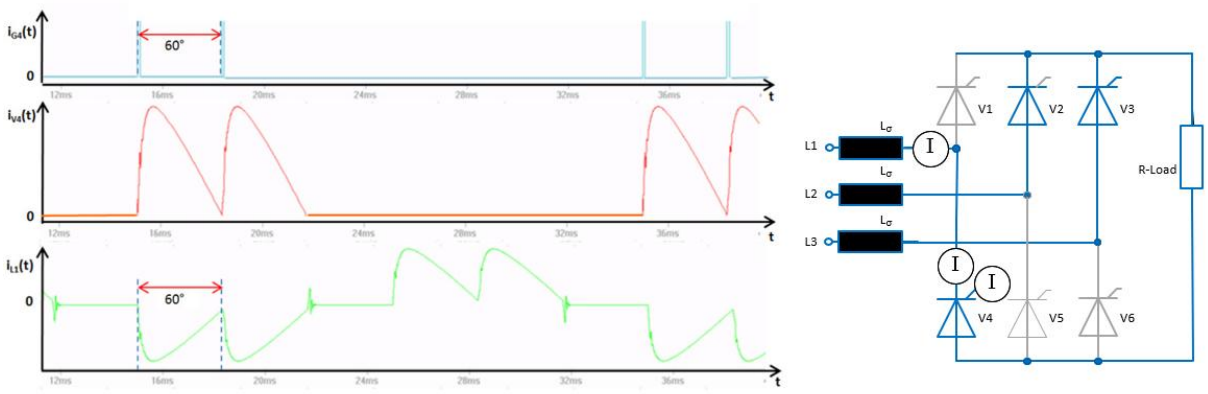


Figure 8.3.5 Current curves in a B6C rectifier bridge with discontinuous output current (example simulation for V4)

8.3.2 Examples of trigger circuits

The trigger circuit has to generate current pulses meeting the datasheet requirements under all operating conditions. This includes the necessity of being synchronised to the mains in order to exclude trigger pulses during the 3rd quadrant reverse blocking state, explained in chapter 2.2.4.2. The pulses that must be blocked can be recognized, for example, by comparing the control signal with the polarity of anode-cathode voltage of each thyristor.
Since the thyristors of a power converter are usually at different potentials, the outputs of the trigger circuits must then be isolated from each other. Pulse transformers are most frequently used for this purpose. These can transmit both the trigger signal and the required control power. Opto-couplers are also used; however, the control power at cathode potential of the thyristor must be generated by a separate power supply or recovered from the anode voltage.
Current and voltage transients can influence the function of the trigger circuit by inductive or capacitive interference or act directly on the control lines of the thyristor and cause unwanted switching. Typical countermeasures are short and twisted control lines, a resistance Rx in the range of about 22 to 220Ω between gate and cathode, and shields between the primary and secondary side in the pulse transformer (or opto-couplers) connected to ground to conduct the current via their coupling capacitance.

8.3.2.1 Trigger circuits with pulse transformers

Figure 8.3.6 shows two examples of conceptual schematics of trigger circuits with pulse transformer.

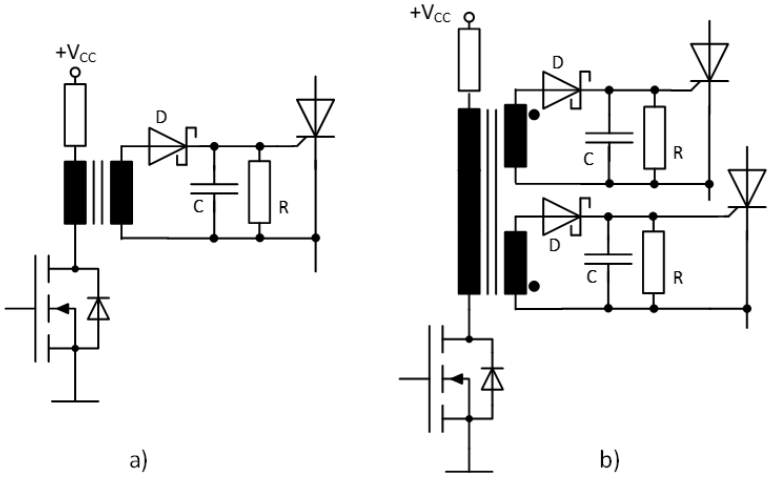


Figure 8.3.6 Conceptual schematics of trigger circuits with pulse transformer: a) triggering a single thyristor; b) triggering two thyristors of a rectifier halfbridge (The shield grounding recommended below is not pictured here.)

The primary voltage V_{CC} and the winding ratio of the transformer must be selected so that the secondary voltage is high enough to supply a sufficient gate current for the thyristor also at dynamical V_{GK} overshot and with negative feedback during the commutating anode current.
The fast diode D in the secondary circuit prevents negative gate current during the commutation swing of the transformer secondary voltage and during dynamical V_{GK}-overshot. Purpose of the RC-element, R_{GK}, C_{GK} is to filter unwanted glitches on the trigger line. A capacitance, C_{GK} of 10 to 47nF is recommended to achieve a discharge time constant $\tau = R_{GK} \cdot C_{GK} \approx 10$ to 20µs (and R_{GK} of 220 to 2200Ω). The power dissipation P_R of R_{GK} at maximum control angle via a half period of line frequency will be:

$$P_R = \frac{V_{GK}^2}{2 \cdot R_{GK}}$$

That means at V_{GK} = 5V and extreme values (max. C_{GK} = 47nF, min. R_{GK} = 220Ω) and $\tau \approx$ 10µs, P_R is about 60mW. At $\tau \approx$ 22µs with $C_{GK} = 10_{nF}$ and R_{GK} = 2200Ω, P_R would be only about 6mW. The amount of power P_R' dissipated with "Pulse Train" thyristor control (cf. Figure 8.3.4) resulting from discharge of C_{GK}:

$$P_{R'} = \frac{C_{GK}}{4} \cdot V_{GK}^2 \cdot \frac{1}{T_{rep}}$$

At V_{GK} = 5V, C_{GK} = 47nF and T_{rep} = 20µs this part would be about 150mW, with C_{GK} = 10nF only about 31mW.
The drive of the pulse transformer can be in either direction, acting as a forward converter or a flyback converter. Figure 8.3.7 shows a flyback converter with trigger pulse curves measured with a thyristor connected. If the primary current has stored enough energy in the transformer when the transistor is switched on, the transistor is then switched off for a defined time. The stored energy now drives the secondary current as trigger current through the gate-cathode path of the thyristor.

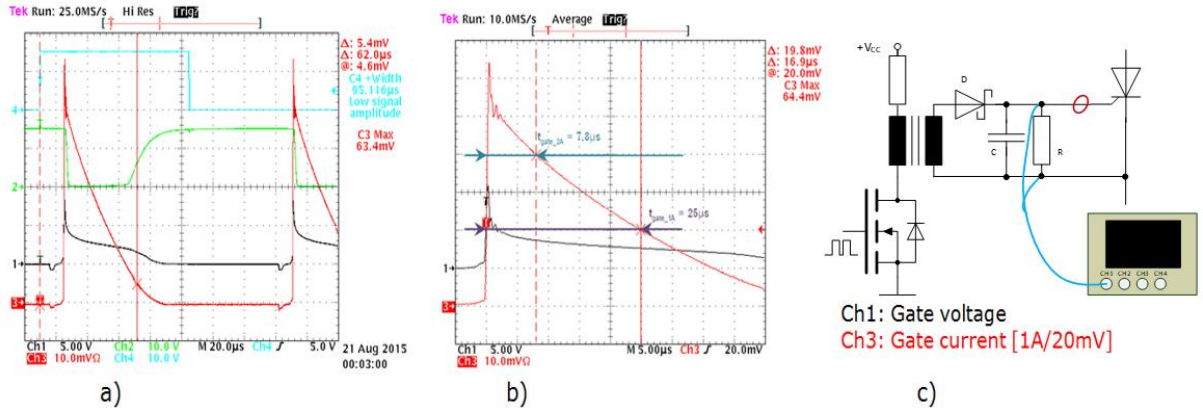


Figure 8.3.7 Gate current and gate-cathode voltage: a) time resolution 20µs/div; b) time resolution 5µs/div; c) measuring circuitry [8.15]

Figure 8.3.8 shows a simplified equivalent circuit diagram of a trigger pulse transformer with usual manufacturer designations

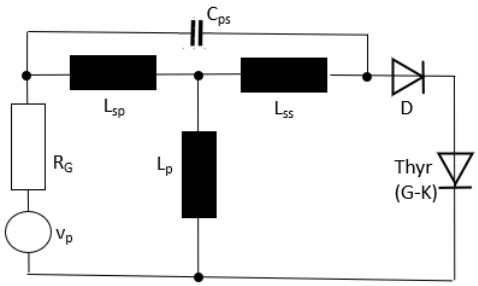


Figure 8.3.8 Simplified equivalent circuit diagram of a trigger pulse transformer with usual manufacturer designations

A typical characteristic for transformer voltage is shown in Figure 8.3.9. The voltage-time area up to the saturation point is $V_0t = t_p \cdot V_{p(av)}$.

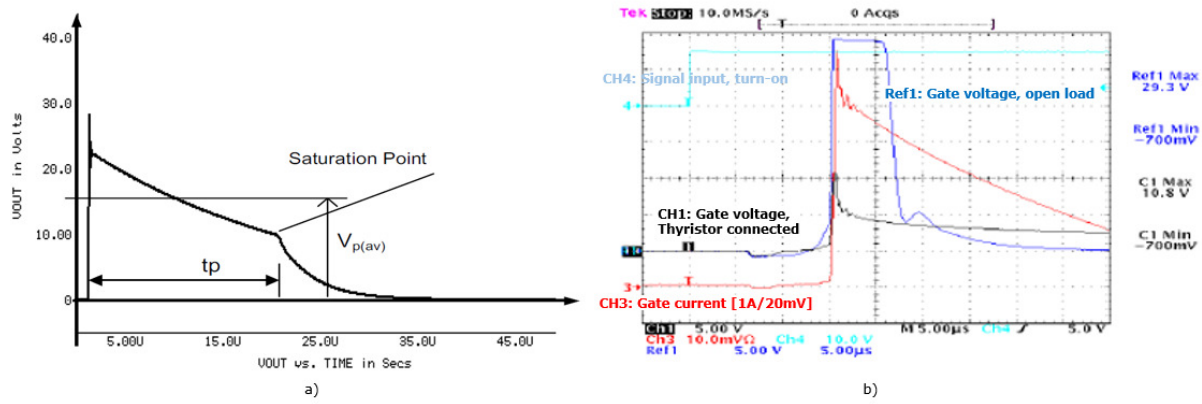


Figure 8.3.9 Output characteristics for a trigger transformer: a) Typical output voltage characteristic (24V supply voltage); b) Time characteristic of drive signal ([8.15])

In the data sheets of trigger pulse transformers, their function and parameters are mostly characterised by the following parameters, extracted from [8.16] and mainly according to [8.17]:
Rated voltage V_{nom}: Secondary-side RMS voltage for which all insulation distances are dimensioned, i.e., 380V, 500V, 750V, 1kV
Test voltage V_p: Insulation test voltage according to the nominal operating voltage V_{nom}. The isolation voltage must correspond to V_{nom}. For 400V mains voltage V_p = 2.5kV is common, while for 690V mains voltage V_p = 4kV is typical (cf. EN 50178). In accordance with the isolation voltage, the transformers must demonstrate the corresponding air and creepage distances between the terminals according to the standard IEC 60664-1.
Turns Ratio: Number of windings primary to secondary and transmission ratio between the windings (1:1, 2:1, 2:1:1)

Ignition current I_{ign}: Primary current peak value, at which the voltage drop across the winding resistance is still insignificant, e.g. < 1V
Primary (magnetising) inductance L_p: Measured at 1kHz and open secondary, dependent on the number of turns and permeability of the core material.
Stray inductance $L_s = L_{sp} + L_{ss}$: Measured at a secondary winding at 10kHz and shorted primary winding; depends on the number of turns and the design of the transformer.
Voltage-time area V_0t: The voltage induced in the secondary winding $V_0 = -L_\sigma \cdot di_p/dt$ decreases after the current increase of a square wave pulse on the primary side during the time t_p, which is inversely proportional to the voltage V_0. Since on the secondary side the voltage amplitude of the pulse is determined by the gate characteristic and by the series resistances in the circuit, V_0t of a trigger transformer defines the width of a single trigger pulse (min. value at the secondary winding at no load until saturation). Typical values are between 180Vµs and 5kVµs. The definition of the pulse width t_p depends on the manufacturer, usually about 50% of the amplitude of the transformer input current.
Rise time of the secondary current t_r: is specified at a defined load resistance R_L i.e. (depending on manufacturer) for 10…90% of the maximum value $\hat{I}_G$. The rise time is proportional to the time constant of stray inductance $L_{sp} + L_{ss}$ and load resistance R (sum of all resistances in the gate circuit).
Winding resistances Rp, Rs: Ohmic resistances R_p (primary winding) and R_s (secondary winding)
Coupling (interwinding) capacitance C_{ps}: Capacitance between primary and secondary winding: can cause unwanted trigger of the thyristor by voltage jumps of the thyristor potential (secondary side) due to the miller effect. Existing shield windings between the primary and secondary windings therefore are to be connected to ground.

8.3.2.2 Trigger circuits with optocouplers

Optocouplers can also be used to isolate the potential of trigger signals. Triggering by optocoupler allows long trigger pulses. Since the required trigger power cannot be transmitted, a separate secondary voltage supply at cathode potential is necessary. If large potential differences must be bridged, a signal transmission via LED transmitter, fibre optic cable and optical receiver can be used for minimising EMI disturbances. The publication [8.14] contains some practical examples from which Figure 8.3.10 and Figure 8.3.11 are obtained.

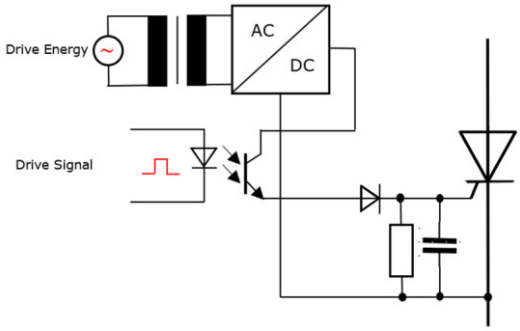


Figure 8.3.10 Thyristor trigger circuit with optocoupler or optical transmitter, fibre cable and receiver

The trigger concept shown in Figure 8.3.11 is mainly used for medium and high voltage applications. The trigger energy is taken from the RC snubber circuit. Safe trigger requires a minimum anode cathode voltage. Such a trigger circuit can also provide optional thyristor status information by adding a feedback signal circuit.

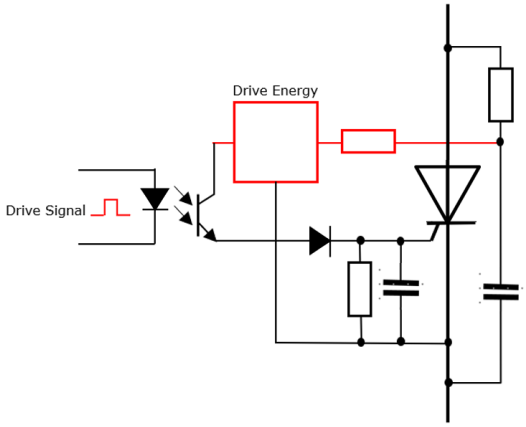


Figure 8.3.11 Thyristor trigger circuit with energy recovery from power circuit via RC snubber

Thyristor trigger circuits products of varying complexity for different requirements are offered as small series by several manufacturers. Information on this is e.g. available in [8.14] and in [8.3.3].

8.4 Protection of rectifier diodes and thyristors

8.4.1 Limitation of current slew rate di_T/dt during turn-on a thyristor

The permissible current slew rate at switching on a thyristor is limited by the maximum rate of rise of on-state current $(di_T/dt)_{cr}$ which the thyristor is able to withstand without being damaged. Its real value depends on the operating frequency, the peak on-state current, the off-state voltage directly before thyristor firing, as well as on the height, width and steepness of the gate pulses, cf. explanations in the chapters 2.2.4 and 7.2.2.1 and in [8.12].
Despite large inductances in the mains supply, steep current slew rates are possible at turn-on of a thyristor, e.g. due to commutation with capacitances within the converter. In such cases, a limitation of di_T/dt is required using a series inductance L_R.

$$L_R \geq \frac{V_{DC}}{(di/dt)_{cr}}$$

$$L_R \geq \sqrt{2} \cdot \frac{V_V}{(di/dt)_{cr}}$$

V_V: RMS supply voltage (line-line)

A linear inductor in series reduces the current density in the triggered area during the current rise. If a saturating choke is used, the high current slew rate occurs only after the step time t_{St} once a larger area of the thyristor is involved in the current conduction.
A low inductance snubber circuit parallel to the thyristor (cf. chapter 8.4.2.2) causes an additional di_T/dt load when switching onto a high voltage instantaneous value due to the discharged capacitor current i_{rc} (Figure 8.4.1). For Semikron Danfoss thyristors, the peak value of this discharge current must not exceed 50A.

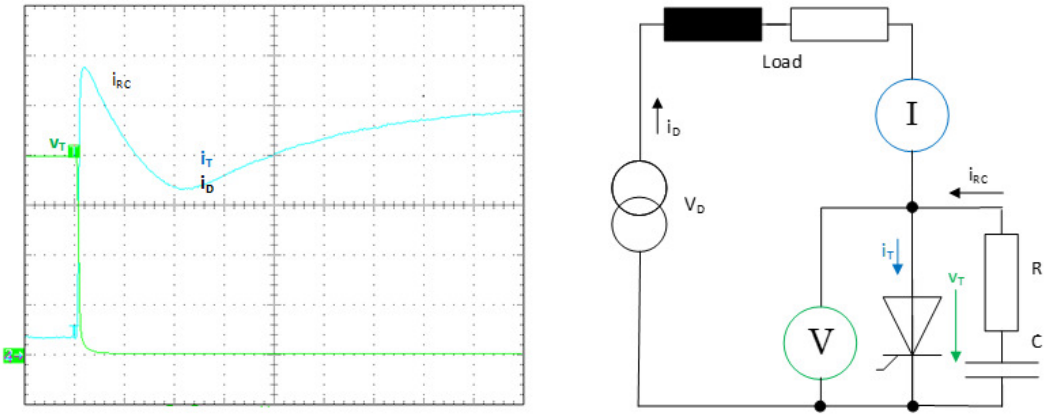


Figure 8.4.1 Discharge current of a snubber circuit parallel to the thyristor when switching on and test circuit

8.4.2 Limitation of overvoltage and voltage slew rate dv_T/dt

8.4.2.1 Sensitivities of diodes und thyristors and possibilities for protection

Diodes and thyristors are sensitive to overvoltage. If the maximum rated voltages given in the datasheet are exceeded, the components might be destroyed. For this reason, the components have to be protected from any excess voltage that might occur in any of the circuits, i.e. the voltage surges have to be reduced to levels which are below the maximum rated values for the given component.
For thyristors, the permissible rate of voltage rise during the transition to the forward blocking state is limited by the maximum rate of rise of the forward-blocking voltage $(dv_T/dt)_{cr}$ which the thyristor can withstand without impermissible triggering. Its real value depends on the value of forward voltage, the shape of their rise, the chip temperature and the output impedance of the trigger circuit, see chapters 2.2.3.2 and 7.2.3.
Snubber circuits with resistors and capacitors (RC snubbers), as well as certain semiconductor components such as varistors or silicon avalanche diodes have proven to be a reliable way of voltage limiting. RC snubbers also limit the voltage slew rate by turning the inductances in the circuit to series resonant circuits, converting the steeply increasing voltage peaks into attenuated oscillations of low amplitude. As a result, the energy of the overvoltage is forced to decrease at low level over an extended period of time, rather than within a brief period at high power.
Varistors and avalanche diodes exploit their non-linear resistance behaviour. Their internal resistances decrease with increasing voltage. Together with the circuit resistors and inductances, they form non-linear voltage dividers that allow low voltages to pass through almost undamped, while higher voltages are strongly damped above a certain value. Here, too, the overvoltage energy is distributed over a longer period of time; it is almost completely absorbed by the damping elements alone.
Components for overvoltage protection can be integrated on the AC side of rectifier bridges, on the DC side or parallel to the individual switches. Their optimal selection is determined by the emergence of overvoltage that need to be protected against:

- Internal overvoltage that occurs during the commutation processes on the power semiconductor. Protective measures are possible only at the DC side respective directly parallel to the individual diodes or thyristors, e.g. by using RC snubbers
- External overvoltage generated, for example, by switching operations on the grid, the triggering of breakers or lightning strikes. Protective measures are possible on both the AC and DC side.

8.4.2.2 Overvoltage and dv_T/dt protection using RC snubbers

Single diode or thyristor protection

The most obvious way of protecting the power semiconductor from overvoltage is to arrange a resistor-capacitors series snubber ("TSE or HSE-network") directly parallel to the individual switches (Figure 8.4.2). This ensures that the component is always protected, regardless where the overvoltage comes from.

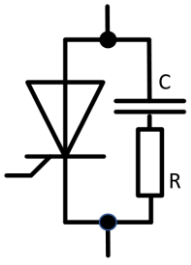


Figure 8.4.2 RC snubber circuit on a single thyristor

In some cases, it is possible or even necessary to use auxiliary diodes in the snubber circuits. For example, using the circuit shown in Figure 8.4.3, the rate of rise of the forward blocking voltage can be ideally attenuated by the components R and C, while for discharge of capacitor C during thyristor triggering an additional resistance R_z is effective which limits the current surge to a harmless level. In reverse direction, R_z is effective too, meaning that in this direction the reduction of surge voltages is not ideal.

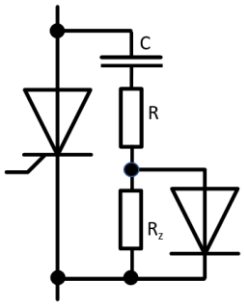


Figure 8.4.3 Single thyristor RC snubber with auxiliary diode

8.4.2.3 Dimensioning of snubber circuits for thyristors and diodes

The rating of a snubber circuit depends (among others) on i_{TM} (i_{FM}) before turn-off, the $-di_T/dt$ ($-di_F/dt$) of the forward current, the reverse current peak I_{RM}, the peak reverse voltage V_{RM}, in relation to V_{RRM} of the device, and, for thyristors, the critical voltage rise time $(dv/dt)_{cr}$ to be observed.
Assuming that approximately half of the energy represented by the reverse recovery charge Q_{rr} is transferred to the circuit as overvoltage, approximate values for the capacitance C and the damping resistance R can be determined as follows:

$$C = \frac{Q_{rr}}{\sqrt{2} \cdot V_V}$$

$$R = (1.5 \ldots 2) \cdot \sqrt{\frac{L_s}{C}}$$

C [µF]: Snubber capacitance
R [Ω]: Snubber resistance
V_V [V]: RMS supply voltage (Line-Line)
Q_{rr} [µC]: Reverse recovery charge
L_s [µH]: Commutation loop inductance

As mentioned in chapter 8.4.1 for Semikron Danfoss thyristors, the current amplitude must not exceed 50A when discharging C via R during trigger. It is therefore possible that R must be increased at the expense of overvoltage attenuation. The power dissipation P_R [W] in the damping resistor R can be determined by the following equation:

$$P_R = \sqrt{2} \cdot V_V \cdot 10^{-6} \cdot Q_{rr} \cdot f + k_1 \cdot C \cdot V_V^2 \cdot f$$

$k_1 = 0$ for diodes in uncontrolled bridge rectifiers
$k_1 = 2 \cdot 10^{-6}$ for thyristors in controlled one- and two-pulse centre tapped circuits, and thyristors and diodes in half-controlled two-pulse bridge circuits
$k_1 = 3 \cdot 10^{-6}$ for thyristors in controlled three- and six-pulse centre tapped circuits as well as fully controlled two-pulse bridge circuits and AC-controllers
$k_1 = 4 \cdot 10^{-6}$ for thyristors and diodes in fully or half-controlled six-pulse bridge circuits

Table 8.4.1 contains the snubber design recommendations for Semikron-Danfoss thyristors and thyristor modules for "common" operating conditions, such as

- Safety factor of V_{RRM} for the peak value of the terminal voltage ≥ 2.2
- Short-circuit voltage of the converter transformer u_K ≥ 5% or mains choke, in which the inductance L of the choke in each phase is such that a short-circuit voltage of at least 5% of the supply voltage V_V results:

$$L \geq 0.05 \cdot \frac{V_V}{2 \cdot \sqrt{3} \cdot \Pi \cdot f \cdot I_V}$$

V_V [V]: RMS supply voltage (line-line)
I_V [A]: RMS phase current
f [Hz]: Mains frequency

Line Input Voltage V_V [V]	Snubber Data	Mean forward current $I_{F(AV)}$, $I_{T(AV)}$ [A]				
		≤25	≤100	≤250	≤500	>500
≤250	C [µF]	0.22	0.22	0.22	0.47	application specific
	R [Ω]	68	33	33	33	
	P_{Rmin} [W]	6	10	10	25	
≤400	C [µF]	0.22	0.22	0.22	0.47	
	R [Ω]	68	47	47	33	
	P_{Rmin} [W]	6	10	10	25	
≤500	C [µF]	0.1	0.1	0.1	0.22	
	R [Ω]	100	68	68	47	
	P_{Rmin} [W]	10	10	10	25	
≤690	C [µF]		0.1	0.1	0.22	
	R [Ω]		100	100	68	
	P_{Rmin} [W]		10	10	50	

P_{Rmin}: Minimum power rating of recommended snubber resistor

Table 8.4.1 Recommended snubber circuits for Semikron Danfoss thyristors

At low possible voltage safety factors or other deviations from the conditions assumed here, the snubber rating may need to be adjusted. In the publications [8.18] to [8.21], suitable calculation options are presented.

Protection of AC controllers by RC snubbers

Since AC controllers consist of two anti-parallel thyristors per phase, both use a common RC-circuit, which limits internal and external overvoltage (Figure 8.4.4).

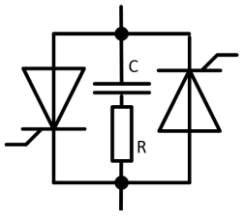


Figure 8.4.4 Common RC snubber circuit of an AC controller

A large commutation dv/dt can occurs here at inductive load and triggering at phase angel α > 0° el. The snubber must limit this below $(dv/dt)_{cr}$ for the still turned off thyristor.
The values of the capacitor C [µF] and the resistor R[Ω] can be roughly determined by means of the following equations:

$$C \approx 700 \cdot \frac{I_V}{V_V^2}$$

$$R \approx \frac{9000}{C \cdot V_V}$$

The power loss P_R [W] in the resistor R is about:

$$P_R \approx 3 \cdot 10^{-6} \cdot C \cdot V_V^2 \cdot f$$

V_V [V]: RMS supply voltage (line-neutral)
I_V [A]: RMS phase current
f [Hz]: Mains frequency

Protection of diode rectifier bridges by RC snubbers

In diode rectifier bridges, single snubbers are normally not economical. Instead, protective circuitry on the AC side is selected (Figure 8.4.5 a) and, if necessary, additional circuitry on the DC side (Figure 8.4.5 b)), since this means that fewer components are needed. For diode rectifier bridges, it is normally sufficient to include a snubber on the DC side only, since two bridge legs are constantly conductive and connect the AC side with the DC side.

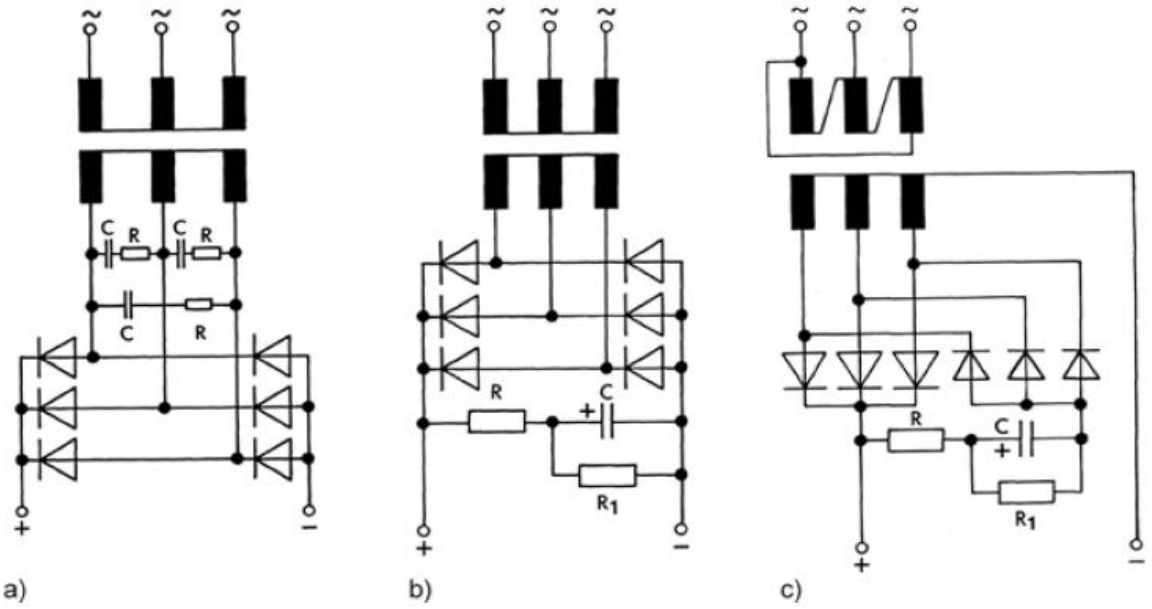


Figure 8.4.5 Snubber circuit for diode rectifier bridges: a) on the AC side; b) on the DC side
c) midpoint connection by adding auxiliary diodes to the bridge circuit

For midpoint rectifier bridges, it often makes sense to use a second identical one-way circuit with low-power auxiliary diodes. Together with the main legs, this results in a bridge circuit where the snubber components can be arranged on the DC side (Figure 8.4.5 c)), see also chapter "DC side snubber circuits" below.

Protection of controlled rectifier bridges by RC snubbers

While in diode rectifier bridges, single-switch snubbers are rather the exception, in thyristor-controlled bridges single-switch snubbers are used as a rule. This is down to the fact that thyristors have to be protected not only from excessive non-permissible surges, but also - and more importantly - from the steep rate of voltage rise (A rate too steep can impermissibly trigger the thyristor).
Further, a thyristor snubber can also be necessary to facilitate thyristor triggering in the case of inductive loads and discontinuous current. This can also be achieved, however, with a DC-side snubber. The use of a single-thyristor snubber is, however, limited because the capacitors discharge through these networks during triggering and thus cause undesired stress with a steep current rise.
In half-controlled rectifier bridges, switch snubbers are used according to the same principles as for fully controlled circuits. In particular, the same resistances and capacitances are to be used for diode snubber circuits as for thyristor snubbers. Under no circumstances are the snubber circuit elements intended for pure diode assemblies sufficient. Diodes in freewheeling paths of controllable converter circuits are to be protected just like the thyristors in the main legs.
In thyristor assemblies for low current densities and high voltages where relatively small capacitance and high-ohmic resistances are sufficient, this di/dt stress is still relatively low, meaning that here a single-switch snubber alone if often enough. This is to be dimensioned like an AC side snubber circuit.
With thyristor circuits intended for higher current densities, however, the capacitances needed to ensure protection from high-energy overvoltage are so high and the optimum resistances so low that a high non-permissible thyristor di_T/dt caused by capacitor discharge during triggering would result. Thus, single-switch snubbers alone cannot provide sufficient protection. In this case, the solution is to use an AC side snubber (if need be, with additional DC side circuitry).
Whether in such cases additional single-switch snubbers dimensioned as described above is necessary depends on the properties of the circuit and the thyristor itself. Due to the considerable critical voltage rise rate of today's thyristors, additional single-switch snubbers are usually not required if an AC-side - and, if required, DC-side - snubber is used.

DC side snubber circuits

For diode rectifier bridges, it is usually sufficient to add a snubber to the DC side if the diode assemblies are not already connected to a low-inductance voltage DC link. The resistors and capacitors are rated according to either the guidelines provided in the first part of chapter 8.4.2.2 or according to the guideline below, depending on whether the surge voltages to be attenuated are on the AC or DC side. If there is any possibility of the rectifier bridge being conductive even when the load is turned off or disconnected, a discharge resistor has to be used.
In rectifier bridges with permanent capacitive load (Voltage source converter), this load will function as an overvoltage snubber, meaning that no additional snubber circuits are needed, if the stray inductance between rectifier bridge and DC-capacitor is sufficiently low. If, on the other hand, there is a ripple filter choke or fuse between the rectifier and capacitive load, a snubber circuit for overvoltage will have to be integrated directly at the rectifier in addition.
In controlled rectifier bridges, an AC-side snubber and single-switch snubbers will normally be integrated, meaning DC snubbers can often be dispensed with. In individual cases, however, they might still be necessary. Sometimes, the single-switch snubbers are not necessary, and one DC and one AC side snubber can be used instead. The best effect is achieved if the following conditions are fulfilled:

$$R + R_L = 2 \cdot \sqrt{\frac{L_L}{C}}$$

$$C = 4 \cdot \frac{L_L}{(R + R_L)^2}$$

C [µF]: Snubber capacitance R [Ω]: Damping resistance
L_L [µH]: total load circuit inductance R_L [Ω]: total load circuit resistance

In many cases, it will suffice to use a smaller capacitor. In this case, R should select such that the aforementioned equation applies approximately. The power dissipation P_R in the damping resistor R can be calculated as follows:

$$P_R = \frac{V_{ALT}^2 \cdot R}{R^2 + \left(\frac{10^6}{2\pi \cdot C \cdot f_{ALT}}\right)^2}$$

V_{ALT} [V]: AC RMS voltage superimposed on the DC output voltage
f_{ALT} [Hz]: Frequency of the superimposed AC voltage

If a discharge resistor R_1 is needed (discharge of C through load is not always guaranteed), R_1 [Ω] is to be rated to

$$R_1 \approx \frac{10^7}{C \cdot f} \text{ with the minimum power dissipation } P_{R1} = \frac{V_D^2}{R_1}$$

f [Hz]: Grid frequency
V_D [V]: DC voltage

8.4.3 Protection from external overvoltage by AC side circuits

External overvoltage is generated, for example, by switching operations on the grid, the triggering of breakers or lightning strikes. Protective measures are possible on both the AC and DC side. In the lower current range, the snubber circuitry described above can often be rated so that it also protects sufficiently against external overvoltage. For high power levels, however, additional snubbing on the AC side makes sense, for which Figure 8.4.6 shows three options that can also be combined. In controlled rectifier bridges, in addition to these occasional non-periodic switching operations, periodic switching operations caused by the thyristor triggering also occur. This is particularly true for diode assemblies which have to work in connection with an AC controller on the primary side of a transformer. For these reasons, particular attention must always be given to the snubber on the AC side.

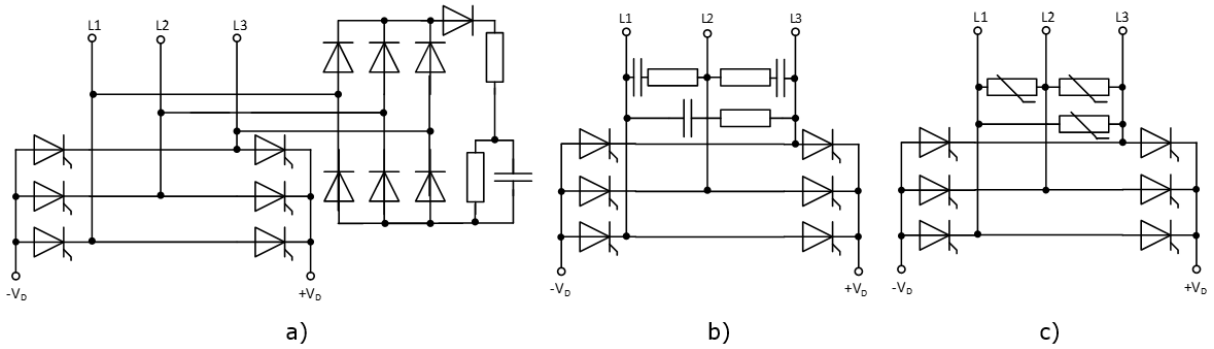


Figure 8.4.6 AC-side overvoltage protection circuits for bridge rectifiers: a) by auxiliary bridge; b) by RC snubbers; c) by varistors (see explanations below)

8.4.4 Overvoltage protection using metal oxide varistors

Varistors are voltage-dependent resistors. The resistance of a varistor decreases as the voltage increases. They can therefore be used to attenuate overvoltage on the AC or DC side or even as single-switch snubbers.

Metal oxide varistors (MOV) consist of zinc oxide with small additions of bismuth, cobalt, manganese and other metal oxides, pressed in pulverised form and then sintered to create a solid disc. The grain boundaries of the conductive zinc oxide grains are responsible for the semiconductor properties of the p-n junction: blocking behaviour at low voltages and non-linear electrical conduction at higher voltages.

Because the current carrying takes place over the entire surface, varistors are more robust than avalanche diodes for overvoltage limitation. Energy is absorbed evenly across the entire body of the device and the resulting heating is distributed evenly over the volume.

The electrical properties are mainly determined by the physical dimensions of the varistor, which is manufactured, for example, in form as disc, block or as an SMD chip. The volume, the varistor voltage by the thickness and the current-carrying capacity by the area perpendicular to the current flow determines the energy dissipation.

General type designation and datasheet specifications for varistors

The type designation normally contains the nominal varistor voltage V_N, suitable as a reference for the selection of varistors. V_N is the voltage drop across a varistor at the 1mA point of its voltage-current characteristic, i.e., at the transition from the leakage current range to the non-linear protection range (Figure 8.4.7). Product datasheets also specify maximum AC and DC operating voltages V_{RMS} and V_{DC}. These values should only be exceeded by transients. The maximum permissible V_{RMS} specified at an ambient temperature T_a must correspond to the highest working voltage given by the application.

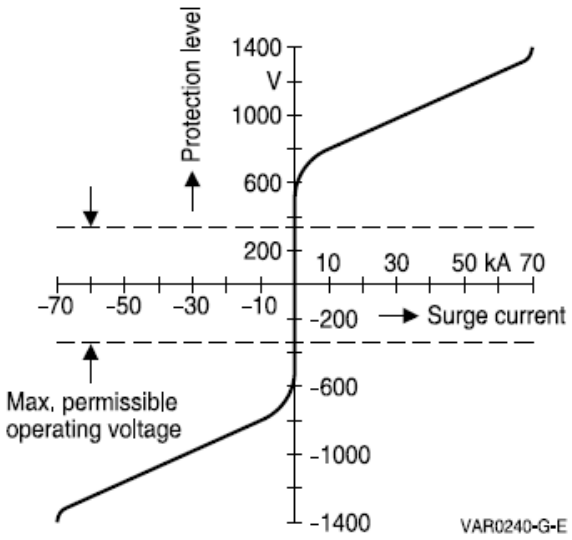


Figure 8.4.7 Typical V/I characteristic curve of a metal oxide varistor SIOV-B60K250 [8.22]

The varistor datasheets contain voltage-current characteristics, showing the maximum protection level as a function of surge current (8/20ms waveform), see Figure 8.4.8.

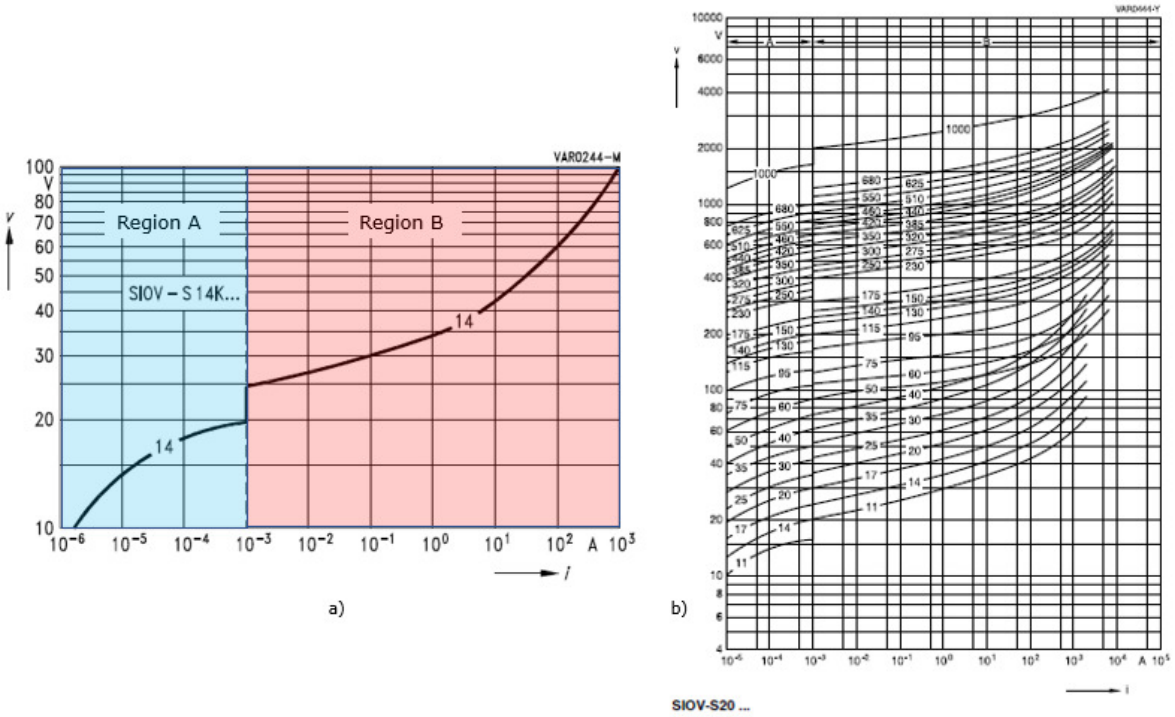


Figure 8.4.8 Voltage–current characteristic of metal oxide varistors: a) general structure; b) V/I characteristics (pulsed) of varistors with 20mm diameter [8.22], [8.23]

The voltage-current characteristics are divided in 2 operating regions A and B. Up to the specified operating voltage - represented by the 1mA limit line between the two areas.
In area A (up to the specified operating voltage) the varistor is high-resistance, in area B (overvoltage) the varistor is in low-resistance mode. For region A, the diagram shows the maximum possible leakage current at a specific operating voltage (lower limit of the tolerance band). For varistor behaviour in low-resistance mode B (overvoltage event), on the other hand, the maximum possible voltage drop across the varistor is important. For this reason, the upper limit of the tolerance band is shown in the V/I diagram for this range, resulting in the discontinuity point in the respective characteristic curves.
Is the varistor selected according to the maximum operating voltage, at nominal operational conditions the resulting power dissipation will be negligible. However, the rated maximum power dissipation P_{max} must be considered if the varistor has not enough time to cool down between a number of pulses occurring within a specified time period.
Short-term current flow – especially when caused by overvoltage – is referred to as surge or transient current. The maximum permissible surge current, and thus for the energy absorption, depend on amplitude, pulse duration, pulse shape and the number of pulses applied during the entire lifetime of the varistor.
The ability of a varistor to withstand a single pulse of defined shape is characterized by the maximum non-repetitive surge current i_{max}, (rise time 8µs/decay time to half value 20µs). If pulses of longer duration or multiple pulses are applied, the surge current must be derated, for example see datasheet value for 5 pulses (rise time 8µs/decay time to half value 20µs per pulse) and Figure 8.4.9.

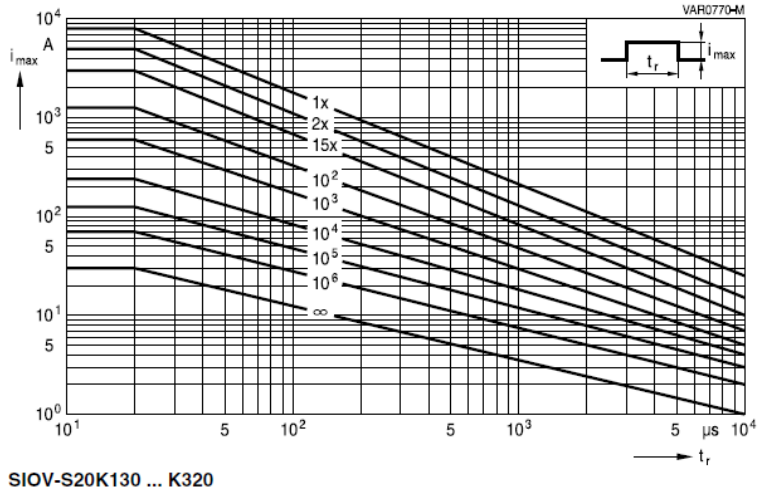


Figure 8.4.9 Maximum surge current i_{max} = f (t_r, pulse train) of varistors with 20mm diameter [8.23]

The derating for a given maximum permissible surge current can be derived from the curves for a type series in repetition numbers. The derating is mainly depending on the varistor size, but also on the rated voltage. At a surge current pulse duration t_0...t_1, the energy absorption of a varistor is correlated with the surge current by

$$W = \int_{t0}^{t1} v(t) \cdot i(t)\, dt$$

v(t): voltage drop across the varistor during current flow [8.22].

In the datasheets, the maximum energy absorption W_{max} is defined for a surge current of 2ms duration. W_{max} can also be calculated from the derating curves with the equation above. It should be noted that the power losses in the varistor at fundamental frequency can normally be neglected. However, one disadvantage of varistors is that they are not able to limit voltage slopes. If the voltage rise has to be limited, an additional RC snubber is required. Further information on the application of varistors can be found, for example, in [8.24].

8.4.5 Overvoltage protection using avalanche or TVS diodes

Avalanche diodes are pin diodes, designed to experience avalanche breakdown at a specified reverse bias voltage. The avalanche breakdown is due to minority carriers being accelerated to such an extent that they cause ionisation in the crystal lattice, generating further charge carriers which in turn lead to further ionisation. This steep increase in reverse current above a certain voltage (breakthrough voltage) is caused by the avalanche effect in the entire space charge zone of the pin junction and does not come from the breakthrough effects on the surface of the silicon element.

The pin junction of avalanche diodes is designed to avoid reverse current concentration and resulting hot spots, so that the diode remains undamaged by the breakdown. Therefore, avalanche diodes can cope with reverse current pulses resulting in power dissipation in the low kilowatt range. Avalanche diodes exhibit a low but significant voltage drop under breakdown conditions. The temperature coefficient of the breakdown voltage is slightly positive.

In contrast to unipolar or bipolar suppressor or TVS diodes (TVS: Transient Voltage Suppressor), Zener diodes are designed for applications with lower voltage.

Avalanche diodes featuring self-protection

In particular, in high-voltage applications, avalanche diodes can be connected in series without the use of snubbers circuits usually required for static and dynamic current distribution. The manufacturer specifies the breakthrough voltage $V_{(BR)}$ as well as the maximum rated reverse current and peak reverse power dissipation P_{RSM} - normally as a function of pulse duration.
A proper selection should be carried out in such a way that the breakdown voltage is significantly higher than the peak value of the operating voltage plus superimposed periodic voltage peaks. The power of the non-periodically occurring overvoltage pulses - if they exceed the breakdown voltage - must be below the permissible surge peak blocking power dissipation for the respective pulse

duration. The breakdown voltage increases with the equivalent junction temperature T_j according to the equation:

$$V_{(BR)1} = V_{(BR)0} \cdot [1 + 1.2 \cdot 10^{-3} \cdot (T_{j1} - T_{j0})]$$

$V_{(BR)0}$: breakthrough voltage at junction temperature T_{j0}

$V_{(BR)1}$: breakthrough voltage at junction temperature T_{j1}

If avalanche diodes are to be used to protect other power semiconductor devices, not only a certain minimum breakdown voltage value but also a maximum value must be maintained. In addition, a certain steepness of the blocking characteristic in the breakdown region must be guaranteed. Some possible applications for avalanche diodes and suppressor diodes are shown in Figure 8.4.10. For protection of AC circuits, bipolar suppressor diodes must be used, featuring semiconductor structures with anti-serial PIN-junctions and thus able to limit overvoltage regardless of polarity.

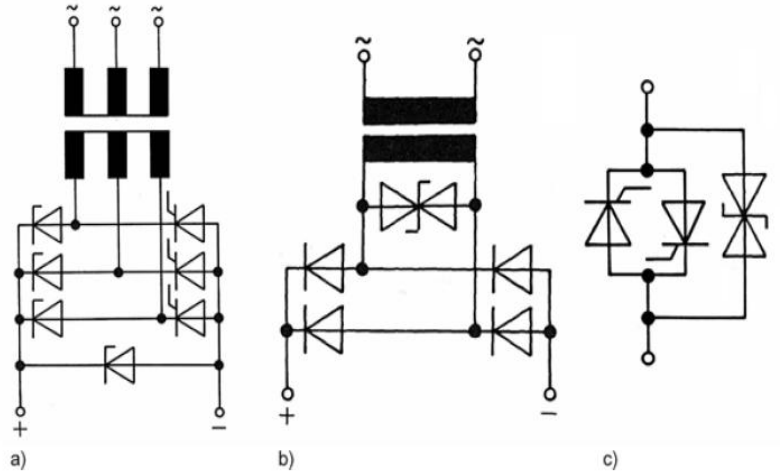


Figure 8.4.10 Circuits with avalanche diodes: a) Half-controlled 3-phase bridge circuit with avalanche rectifier diodes that also protect other semiconductors from overvoltage; b) AC side protection of a single pulse diode bridge featuring a bipolar suppressor diode; c) AC controller snubber featuring a bipolar suppressor diode

Silicon avalanche or suppressor diodes cannot withstand high-energy overvoltage, such as those that occur when transformers are switched off during no-load operation. In such cases, RC snubbers are therefore needed either instead of the avalanche diodes or in addition to them.

8.4.6 Overload and overtemperature protection for rectifier diodes and thyristors

8.4.6.1 Overcurrent and short circuit

The term Overload includes both overload due to excessive current and short circuit.
A typical Overcurrent is only slightly higher than the full load current, but can damage the thyristors or diodes due to excessive heating. The requirement for a protective device is to limit duration and peak value of the overload current.
Short circuits typically result from a catastrophic electrical failure, such as an insulation failure. The peak value of the short-circuit current is determined by grid impedance and voltage and can be a multiple of the full-load current of the system. Normally, heating is so rapid that damage occurs within milliseconds (sine half waves) and cannot be characterised by the RMS current. The requirement for the protective device is to dissipate a large part of the energy converted by the current in the resistive components of the circuit in the event of a fault. Furthermore, the protective device must limit the peak value of the current. The most common causes of short-circuits in converters are:

- Short circuit in the load or the connecting cables between the converter unit and load
- Short-circuit in a rectifier diode or thyristor due to loss of blocking ability (sudden failure)
- Thyristor trigger errors

8.4.6.2 Overload properties of rectifier diodes and thyristors

Diodes and thyristors cannot actively limit or switch off overcurrent. A steep increase in chip temperature associated with excessive load current can cause the temporary loss of controllability and blocking capability. Therefore, certain specified overloads are allowed only at intervals of several seconds and only occasionally with a limited number of periods.

In case of a permissible overload the surge current determined by the grid impedance and mains voltage must be survived. The permissible overload stress for diodes and thyristors in mains applications is described in thyristor or diode module data sheets in figures 7 or 8 "Surge overload current vs. time", which are explained in more detail in chapter 7.2.4 based on Figure 7.2.21.

8.4.6.3 Devices for short circuit protection

Fast acting melting fuses

Melting fuses are protective devices in which the fuse element melts and opens the circuit if the current exceeds a specific value during a period of time. Fast acting melting fuses or "semiconductor fuses" for the protection of power semiconductor devices – with AC voltage ratings up to 1300V and for currents up to 2500A - are intended primarily to provide short-circuit protection. Under certain circumstances, however, the fuse can also provide protection against overload currents. For this purpose, it may be necessary to cover the time until the fuse provides protection with an additional protective device. Figure 8.4.11 shows common basic construction of fast acting melting fuses.

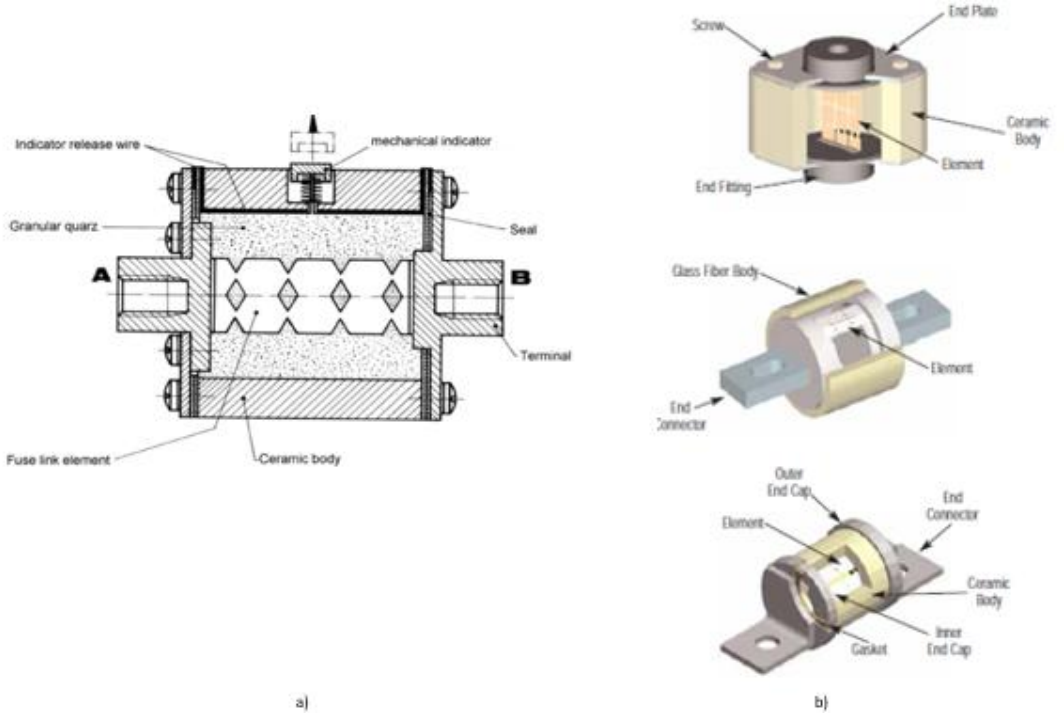


Figure 8.4.11 Fast acting (semiconductor) melting fuses: a) Cross-section; b) Typical Fuse constructions [8.25]

When the fuse melts, the current has reached a given level during the melting time. During the current interruption process, an arc occurs between the terminals of a fuse. This forces the current to zero during the arcing time and finally isolation is established.
For short-circuit protection using fast semiconductor fuses, short circuits are assumed to occur very seldom only. In applications with more frequently load short-circuits, a DC side high-speed circuit breaker, a power circuit breaker and a suppression of gate trigger pulses are needed. This has to be in addition to the fuses also required because of the other short-circuit possibilities mentioned below.

Power circuit breakers

Power circuit breakers are the most common form of overload protection. There are switches with thermal, magnetic and thermo-magnetic tripping. Similar to fuses, their response times are dependent on the overcurrent and lie within the range < 1s; the response time for high overcurrent is shorter. Manufacturers show this ratio in the form of a characteristic that can be then compared with the overcurrent capability (current rating) of the semiconductor component.
Note that the trip current of power circuit breakers and the currents in the current / time curves for safety fuses are always RMS values, while the maximum surge current of the semiconductor components are peak values of sinusoidal half waves. Thus, if comparisons are to be made, these values first must be converted into RMS values.

Throughout the entire possible time period, the trip current of the power circuit breaker has to be lower than the permissible overcurrent of the semiconductor component in the case of error. If this cannot be achieved for the entire period, an additional protective device - normally a semiconductor fuse - must be integrated for the period not covered.

High-speed DC circuit breakers

In rectifier systems where frequent short circuits in the load are to be expected, a fast DC circuit breaker can be installed on the load side to avoid frequent replacement of fuses. Fast fuses as additional protection in case of failure of semiconductor devices are needed and the fast DC circuit breaker must be selected in such a way that in case of a short circuit of the load the circuit breaker is tripped before one of the semiconductor fuses melts (selective protection). Selectivity is given if the time/current characteristic of the fast DC circuit breaker runs below the pre-arcing characteristic of the fuse over the entire range in question.

Suppression of trigger signal

In controllable thyristor circuits, it makes sense to implement overcurrent protection by influencing the gate trigger unit. If a current or a temperature sensor indicates that the limit value has been exceeded, the phase angle is increased, or the trigger pulses are blocked.
The requirement for the use of the gate trigger unit as protection is, of course, that the thyristor controllability is maintained long enough (i.e. the maximum permissible junction temperature is not exceeded) for the protection to take effect. For short-circuit currents that rise steeply within one semi-oscillation, for example, protection via the gate trigger unit is not possible.

8.4.6.4 Protective devices for overtemperature and malfunctions in the cooling system

The destruction of power semiconductors in overload conditions always happens due to excessive non-permissible temperatures, regardless of whether the overload results from overcurrent or malfunctions in the cooling with unintentional change in cooling conditions. As a result, the power semiconductors cannot cope with currents that are normally permissible when cooling is properly ensured. Examples of improper cooling are blocked fan slits, fan breakdown or, in water-cooled systems, malfunction in coolant supply. In general, it makes sense to use devices to protect the semiconductors by components that react to this temperature rise, although their protective function is limited by the thermal time constants in the system.

Bimetal switches

Bimetal switches contain bimetal stripes which, at a certain factory-set temperature, snap from one position to the next, opening or closing a contact in the process. They normally have screw studs with which they are screwed onto the heat sink, establishing the closest possible thermal contact with the semiconductor components as possible.

Temperature-dependent resistors

Temperature-dependent resistors respond to temperature changes quickly, resulting in a minor safety margin between the operating current and the minimum current required to trip the protective device. An additional electronic circuit is needed to convert the change in resistance into a signal that can, for example, trigger a protective device. Temperature-dependent resistors can also be integrated into power modules, for example soldered onto the insulating substrate. Integrated sensors such as these respond far more quickly than the sensors on the heatsink; having said that, these are not enough to detect increases in chip temperature caused by steep overcurrent rising before chip damage occurs. The silicon-based resistors used have either a positive temperature coefficient (PTC) or a negative temperature coefficient (NTC).

Wind vane relays

With enhanced air cooling, wind vane relays which trigger a protective component or influence the driver unit under error conditions can be used to protect the power semiconductors from overload should the fan break down or the fan vents be blocked.

Water flow monitors

In water-cooled systems, flow monitors or flow indicators can be used to monitor the coolant flow.

8.4.7 Short circuit protection by fast acting melting fuses

8.4.7.1 Fuse arrangements and fast acting melting fuse behaviour

Typical arrangements of AC-side semiconductor fuses in power converters are shown in Figure 8.4.12.

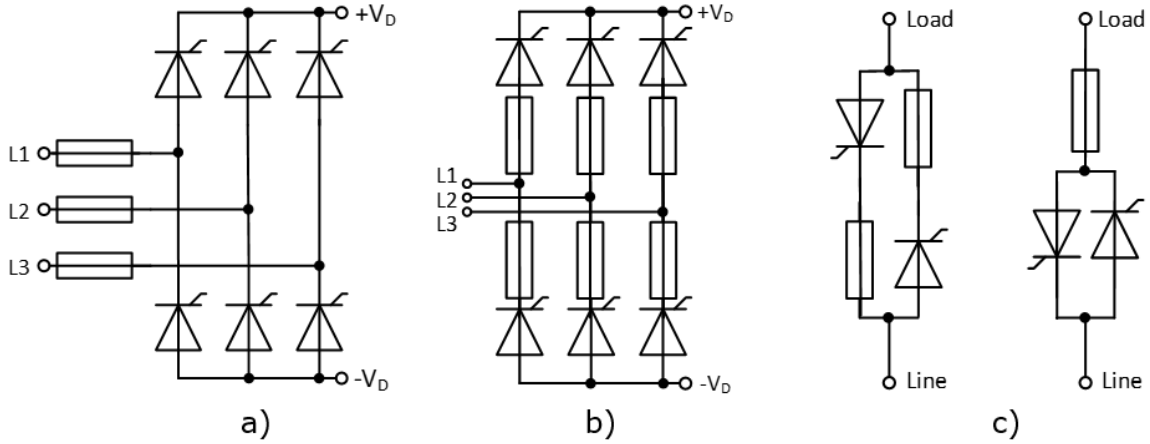


Figure 8.4.12 Arrangements of AC side fuses: a) mains fuses; b) branch fuses; c) fuses in AC-controllers

In rectifier bridge circuits, two power semiconductors each have a common AC terminal. For this reason, they can be protected by a common fuse in the AC supply line (mains fuses, Figure 8.4.12 a). Compared to the branch fuse topology (Figure 8.4.12 b) that has the advantage that fewer fuses are needed and that the switching voltage that occurs when the fuse element melts does not put any load on to the semiconductor components. For very high currents, with mains fuses it also may well be difficult to find a fuse with sufficient rated RMS current and operating i^2t. Figure 8.4.12 c) shows usual fuse arrangements in AC-controller topologies.
If diodes or thyristors are connected in parallel, each semiconductor component is equipped with a fuse. The advantage of this is that if one component or fuse suddenly fails, the device will remain fully functional - with less power accordingly. The internal resistances of the fuses will also compensate somewhat for the differences in the characteristics of the semiconductor components, meaning the current distribution - in short-circuit conditions – will be more homogenous.
In contrast to electromechanical or electronic overcurrent protection devices melting fuses do not have a fixed tripping current, from which the protective effect occurs. The melting time depends on the size of the overcurrent. The value pairs of currents and corresponding melting times are shown in time/current characteristics as shown, for example, in Figure 8.4.18 below.
Depending on the protective function (overcurrent or short-circuit), fast acting fuses for the protection of power semiconductors must belong to one of the operational class gR or aR according to IEC 60269-1 ([8.30]:

- gR class: Fast acting fuses with full-range protection. It protects overload currents as well as short circuit currents.
- aR class: High performance, ultra-fast acting fuses for superior short-circuit protection only.

When the fuse melts, the current has reached a given level during the melting time. During the current interruption process, an arc occurs between the terminals of a fuse. This forces the current to zero during the arcing time and finally isolation is established. The peak arc voltage of the fuse and the permissible peak reverse voltage of the semiconductor should always be coordinated. The melting time plus arcing time is called clearing time, and for long melting times the arcing time is negligible. Figure 8.4.13 illustrates the principal courses of current and voltage during melting of a fuse due to a short circuit.

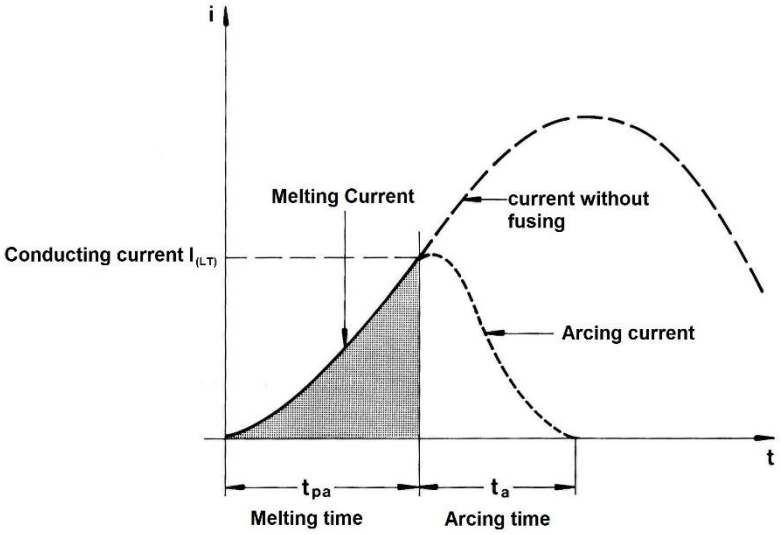


Figure 8.4.13 Current and voltage courses when switching off a short circuit with a fast-acting melting fuse

The meaning of the values entered in Figure 8.4.13 is:
Melting (pre-arcing) current: Current flowing through the fuse during melting process
Let-through (conducting) current $I_{(LT)}$: is the maximum instantaneous current that is reached during fuse operation, if this turn-off prevents the prospective current from reaching its maximum value. A fuse, operating in its current-limiting range, will clear a short circuit before the first peak of the prospective short circuit current. In addition, it will limit the instantaneous peak let-through current to a value substantially less than that obtainable without fuse.
Prospective short circuit current I_{PS} (dashed line in Figure 8.4.13) is the prospective (available) RMS current under short-circuit conditions that would flow in the fault circuit without fuse. Normally I_{PS} is given as symmetrical RMS value, and its value might be needed to determine the precise arcing i²t value.
Arcing current: Current flowing through the fuse during arcing process.
Melting (pre-arcing) time t_{pa}: Time between the onset of a current that is large enough to melt the fusible element and the emergence of the arc
Arcing time t_a: Time that elapses between the generation of the arc and its (final) extinction. During the short-circuit interruption, an *Arcing voltage V_a* is generated between the terminals of a fuse.
The sum of the melting (pre-arcing) time and arcing time *is called (total) Operating (clearing) time t_{op}*. The clearing time is defined between the beginning of the overcurrent and the final opening of the circuit at system voltage.

8.4.7.2 Selected manufacturer's catalogue specifications for fuse selection

The explanations mentioned below refer to fast acting fuses designed to protect power semiconductors. Unfortunately, the terminology and specification of the parameters as well as the dimensioning instructions given in the application documents are very manufacturer-specific, which contradicts a summary presentation at this point.
Further information can be found, for example in the manufacturer's publications [8.26] and [8.27], also for the use of fuses in applications not considered further here, e.g. for DC applications, photovoltaics and electric vehicles.
Since the conditions in practical applications deviate from the test conditions, safety margins and/or an adjustment of the permissible current will be necessary, which the manufacturers provide in the data sheets by means of correction factors, formulas or diagrams.
Many conditions can affect the real current-carrying capacity of a fuse, and to prevent premature ageing, observing explanations below enabling a safe calculation of the rated current.

Rated current I_n and corrective steps for current adjusting

The rated current of the fuse is the RMS current it can carry continuously without degradation or exceeding the applicable temperature rise limits under defined stationary conditions. Please note that the rated current for diodes and thyristors is specified as an average value. At rated RMS current I_n, a fuse can be continually loaded under certain circumstances, i.e., at 20°C ambient

temperature, free air convection and maximum 1.6 A/mm² current density in the connections, I_n is established by testing the fuse under conditions specified in standards, such as IEC 60269-1 [8.30], UL 248-1 [8.31] and UL 248-13 [8.32].
For cyclic overload currents, higher ambient temperatures, smaller wire diameters or higher frequencies the current must be reduced. If fuses are forced cooled, on the other hand, a higher current is possible. Manufacturers give correction factors, conversion equations or diagrams for this. The Table 8.4.2 – derived from information contained in [8.28] - illustrates exemplary factors to be included in the selection of fast acting melting fuses.

Consideration of	Coefficient	Notes
Ambient temperature	A_I	$A_I = \sqrt{\frac{T_{fmax} - T_a}{T_{fmax} - T_0}}$ T_a: ambient temperature T_0: manufacturer's reference temperature T_{fmax}: maximum allowable fuse temperature (typ. 130…150°C)
Forced cooling influence	B_v	Linear increase from 1.0 at v = 0 to typ. 1.25 at v = 5m/s
Cooling by cables & busbars	C_l	Influence of cable/busbar sizes on fuse temperature in relation to the type test conditions. C_l varies depending on the fuse design, typical values 0.8...1.0. For liquid cooled connectors, typical values 1…1.3.
High-frequency, proximity & skin effect	C_{PE}	Influence of significant high frequency current components (>1kHz), on the current distribution within the fuse, caused by the interactions of electromagnetic fields. Depending on the position of the fuse and the return conductor or other current-carrying conductors, resulting in unequal distribution of current between the fuse elements. C_{PE} can vary between 0 (<100Hz) and 0.6 (>10kHz) [Mersen]
Load current fluctuations	A'_2	Influence of variations in the RMS current and duty cycle, e.g by means of a a load classification as either continuous, or cyclic: Continuous (steady state load current during operation, no overloads): At only a few switch-offs per year: $A'_2 \sim 0.95$ For one stop per day or overnight: $A'_2 \sim 0.9$ For ≤ 12 stops per day: $A'_2 \sim 0.8$ Cyclic (variable load current, with repetitive cycles): Further reduction of A'_2 required For long-duration on/off cycles (e.g. each 30 minutes), the fuse cools down during the off-period, resulting in a large temperature swing amplitude: $A'_2 \leq 0.6$
Repetitive cyclic overloads	B'_2	Influence of the maximum repetitive overload on the service lifetime of fuse (see chapter below)
Occasional overload	C_{f3}	Influence of the maximum occasional overload current on the service lifetime of fuse (see chapter below)
Combining these factors, for a fuse with a nominal current rating I_n the practically maximum permissible continuous RMS current $I_{n'}$ is $I_{n'} = I_n \cdot A_I \cdot B_V \cdot C_I \cdot C_{PE} \cdot A'_2$		

Table 8.4.2 Exemplary current correction calculation and descriptions of the respective influences according to [8.28]

Cyclic overload currents

The heating and cooling of the fuse elements due to variable load conditions leads to thermal stress inside the fuses, which can result in mechanical fatigue and premature tripping of the fuse. Manufacturers also give quite complex conversion equations or diagrams for such stresses. A simplified proposal for the correction of the permissible RMS current is as follows:

If the duty cycle time t_s (sum of all conduction intervals $t_1 + t_2 + \ldots$ plus any pauses) is less than a minute, and the maximum overcurrent is no more than 2.5 times the rated current, the following mean load current I_{RMS}, which can be calculated from the equation below, can be expected:

$$I_{RMS} = \frac{I_{RMS1} \cdot t_1 + I_{RMS2} \cdot t_2 + \ldots}{t_s}$$

I_{RMS1}: effective value of current during time t_1 etc.

To check that the fuse is not subject to overload under the load and cooling conditions prevalent in the device, manufacturers recommend measuring the voltage for full load once 5 seconds after turn-on (V_{5s}) and once again 2 hours after turn-on (V_{2h}); it goes without saying that this must be done for exactly the same current. Owing to the temperature dependency of the fuse link resistance, these voltage values provide information on the temperature that the fuse link develops in application. The fuse is not overloaded if the following applies:

$$\frac{V_{2h}}{V_{5s}} \cdot \frac{1 + 0.004 \cdot T_a}{1.14} \leq N$$

T_a: ambient air temperature in °C

N : type-specific constant of the relevant fuse, given by some manufacturers

This formula may differ slightly from one manufacturer to the next.

Short circuit currents

According to [8.28], the transient short circuit current in an AC circuit i is given by the equation

$$i = \sqrt{2} \cdot I \cdot \left\{\sin(\omega t + \theta - \Phi) - \sin(\theta - \emptyset) \cdot e^{-\omega t/\tan\Phi}\right\}$$

I: Prospective short circuit current

ω: Supply angular frequency ($2\pi f$)

θ: phase angle at beginning of short circuit

Φ: power factor angle of the circuit impedance ($tan^{-1}\, \omega L/R$)

The first term in this equation represents the steady-state AC short circuit current, while the second term represents an exponentially decaying transient DC component.

When the short circuit occurs at θ = Φ, the current's transient component is zero and the short circuit current is a symmetrical sine wave. The peak value of short circuit current is $\sqrt{2} \cdot I_p$ (prospective RMS current). If θ ≠ Φ the short-circuit current will have an asymmetrical waveform with an exponentially decaying DC component (Figure 8.4.14).

The maximum value of the first asymmetrical peak current is obtained if the circuit is closed at the voltage zero (θ = 0). It can reach $2 \cdot \sqrt{2}$ times the RMS symmetrical current in a purely inductive circuit, or about 2.5 times in a circuit with an X/R ratio of 10:1.

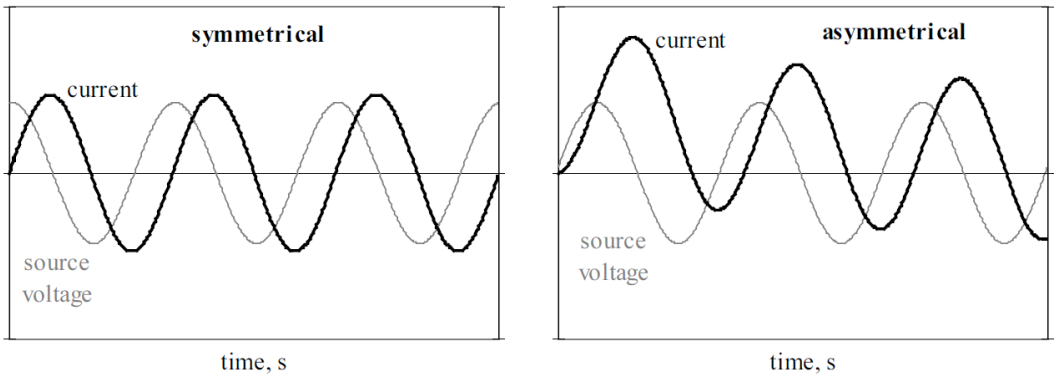


Figure 8.4.14 Symmetrical and asymmetrical short circuit currents in an AC system [8.28]

When a fault occurs in a DC circuit, the prospective short circuit current is the constant final value V_{DC}/R, where V_{DC} is the source voltage and R is the resistance of the circuit. After a fault occurs, the current increases exponentially with a time constant T = L/R, where L is the inductance of the circuit. The instantaneous short circuit current is given by

$$i = \frac{V_{DC}}{R} \cdot \left(1 - e^{-\frac{R \cdot t}{L}}\right)$$

Rated AC voltage V_n

Fast acting semiconductor fuses are usually specified for sinusoidal AC RMS voltage and line frequency between 45Hz and 62Hz. The rated voltage V_n is the maximum permissible open-circuit RMS voltage at which a fuse may be used and still safely interrupt an overcurrent. Exceeding the rated voltage of a fuse will affect its ability to safely clear an overload or short circuit. Also, for non-sinusoidal voltage, neither the RMS nor the crest value of the specified V_n may exceed.
The data sheets often contain several specifications for V_n, valid for different test specifications, e.g. according to IEC 60269-1 (AC-voltage tests at 110% of V_n) [8.30] or to UL 248-13 (AC-voltage tests at 100% of V_n) [8.32].
The rated AC voltage usually applies to frequencies from 45Hz to 1000Hz because the interrupting process at even lower frequencies behaves more like DC. It must at least correspond to the input mains AC voltage.
In rectifier bridge circuits often two fuses are connected in series in the short-circuit circuit, as seen in Figure 8.4.15 below. The mains voltage is divided between the two fuses. As the voltage distribution may not be completely homogeneous, it is advisable to use 60 % of the rated voltage for each fuse.

Peak arc voltage

When the fuse melts, the current has reached a given level during the melting time. During the interruption of a short circuit, an arc occurs between the terminals of a fuse. This forces the current to zero during the arcing time and finally isolation is established. The arc voltage value mainly depends on the recovery voltage and the power factor cos φ. The quicker a fuse opens the higher the peak arc voltage.
The peak arc voltage of the fuse and peak reverse voltage of the semiconductor should always be coordinated. If a commutation error or a component failure occurs, the input and output voltage are added together. In this case, the voltage driving the short circuit is then approximately 1.8 times the AC operating voltage. For this reason, the selected fuses must have correspondingly high rated voltages, and the increased recovery voltage must be considered when determining the operating i²t value. An example at failure of thyristor 2 can be seen in Figure 8.4.15.

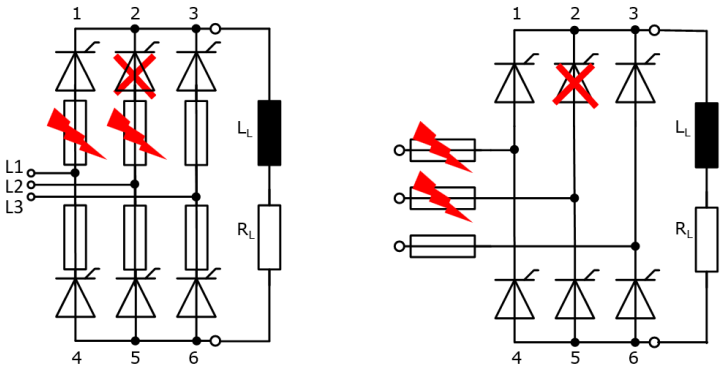


Figure 8.4.15 Arc voltages across the tripped fuses in the case of a short circuit induced by blocking failure of thyristor 2 when thyristors 1 and 5 are conducting

With arm fuses, thyristor 4 is subjected to the sum of the arc voltages from fuse 1 and 2; thyristors 3 and 6 are subjected to the arc voltage from fuse 2 (Figure 8.4.15 a)). If Mains fuses are installed, the arc voltages of the fuses are shorted through the conducting thyristor 1 and short-circuited thyristor 2 as opposed to the remaining thyristors (Figure 8.4.15 b). It should be considered that in the worst-case scenario, the arc voltages of two fuses connected in series may be added in the event of a short circuit. Therefore, the diodes or thyristors to be protected must be suitable for twice the arc voltage.

Melting (pre-arcing) I^2t value $(I^2t)_{pa}$

The value of the integral $I^2t_{pa} = \int_{t_0}^{t_{pa}} I_p^2$ (square of the prospective current over pre-arcing time) depends on the initial temperature and the prospective short-circuit current. It is not time-dependent for pre-arcing (melting) times of less than 10ms.
The lower curve in Figure 8.4.16 shows the dependence of the integral I^2t_{pa} of a typical semiconductor fuse on the RMS prospective current. At very high currents, the melting value I^2t is

roughly constant because the heating rate is so high that heat losses from the fuse are negligible. At lower prospective currents, the melting time is longer, and the heat losses cause the I^2t value required for melting to increase.

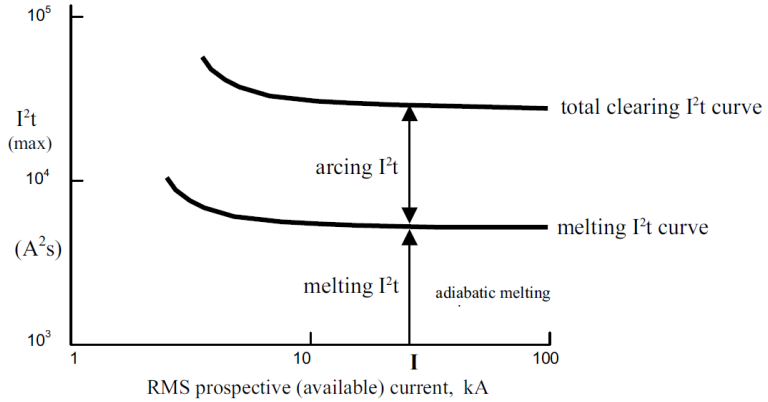


Figure 8.4.16 Principal I^2t characteristics [8.28]

Total clearing (operational) I^2t_{cl} @ rated voltage

As soon as the end of the melting (pre-arcing) time t_{pa} is reached, the arcing time t_a starts. The fuse develops an arc voltage that is higher than the source voltage so that the current drops to zero. The arcing I^2t_a depends on the recovery voltage, the prospective current and the power factor (Figure 8.4.16, upper curve).
During the arcing time, the fuse must dissipate both the energy supplied by the source and the energy ½ L · I², stored in the circuit inductance L. The total energy dissipation by the fuse, or total clearing I^2t, is the sum of the melting (pre-arcing) I^2t_{pa} and arcing $I^2t_a = \int_{t_{pa}}^{t_a} I_p^2 dt$ of the square of the prospective current over arcing time during the arc.
Published data by manufacturers normally give the worst-case total clearing integral I^2t_{cl} under short-circuit conditions at the fuse's rated voltage, 50/60Hz mains frequency, a circuit power factor cos φ = 0.15 and a short-circuit level of 10 to 15 times rated current. When the applied voltage is lower than the fuse's rated voltage, the current-limiting action is more effective, and the total I^2t_{cl} is reduced. The same applies for cos φ > 0.15.
For operation at lower voltage or at different power factor, the manufacturers provide correction factors for I^2t_{cl}, in the form of diagrams; see example in Figure 8.4.17 for I^2t multiplier as a function of AC voltage.

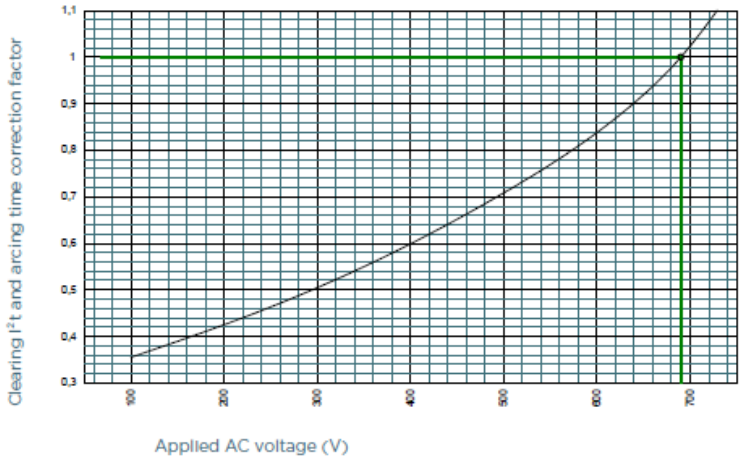


Figure 8.4.17 I^2t voltage multiplier characteristic curves of 690V gR size 71 square body fuses [8.33]

Time-Current characteristics

In contrast to electromechanical or electronic overcurrent protection devices melting fuses do not have a fixed tripping current, from which the protective effect occurs. Thus, the melting time depends on the size of the overcurrent. The value pairs of currents and corresponding melting times are shown in time/current characteristics (Figure 8.4.18).

For a known prospective short-circuit current value, the virtual melting time of a given fuse can be read from the diagram "Time-Current characteristics", a curve of the virtual pre-arcing (melting) time t_{vpa} as a function of the symmetrical RMS prospective short-circuit current I_p under certain conditions, specified in IEC 60269 [8.30]. This normally applies to $T_f \approx 20°C$ initial temperature. In practice, virtual times longer than approximately 100ms are equivalent to real time.
Using I_p and t_v direct from the fuse time-current curve permits calculating its melting integral in A^2s ($I_p^2 \cdot t_v$) for the actual value of prospective current.

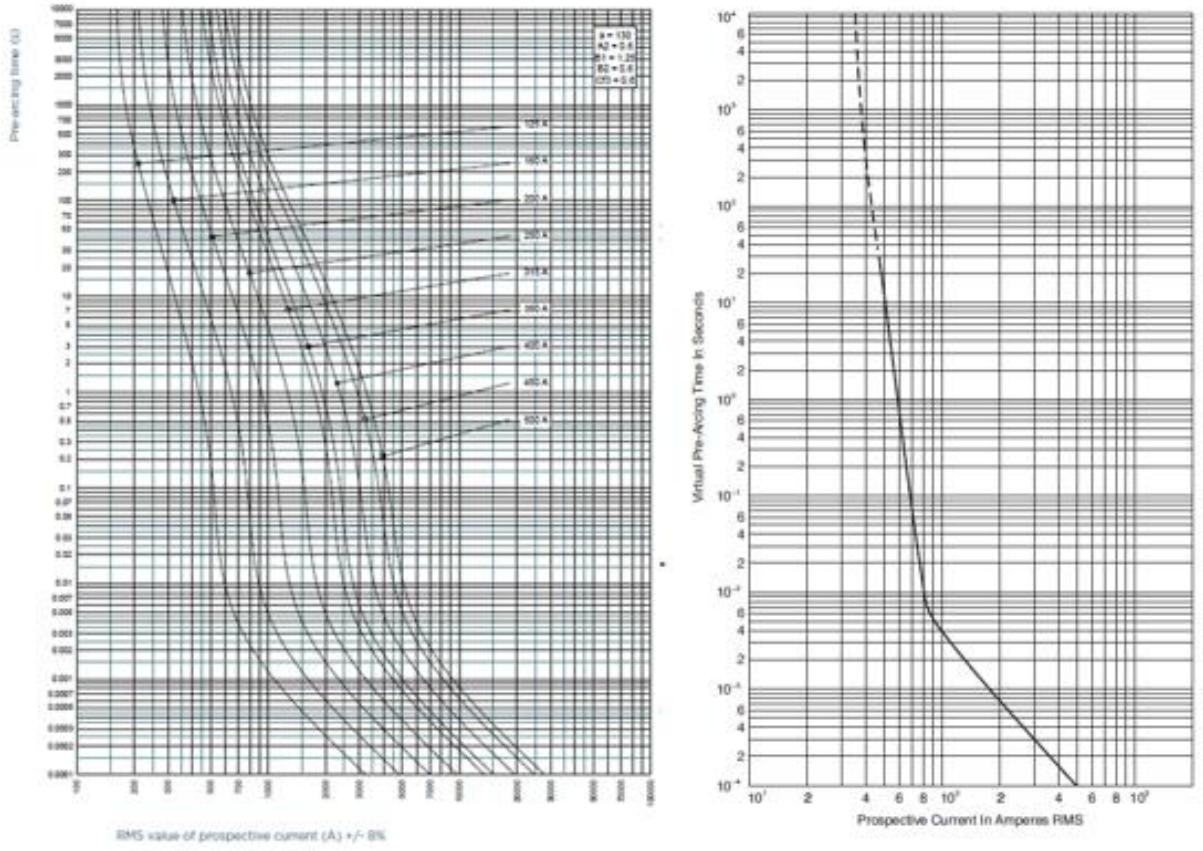


Figure 8.4.18 Time-Current characteristic curves of 690V gR size 71 square body fuses [8.33]

In contrast to the operational class gR fuses with full-range protection, the even faster opening aR class fuses are only able to switch-off short circuits. Therefore, a "forbidden area" is marked in the time-current curves of aR fuses, e.g. by dashed curves or a horizontal line. This means that the fuse is not suitable to interrupt currents that lead to melting times in this range.
For high short-circuit currents that cause melting at times on the order of the main frequency cycle, the melting time is strongly influenced by the current waveform (symmetrical or non-symmetrical). In these cases, the time-current characteristic is of limited value and system protection must be coordinated using I^2t values, because the standard time-current curve is only valid for symmetrical sine waves.

Cut-off (Let-thru) current characteristic

The ability to limit current within defined boundaries is one of the most important advantages of modern semiconductor fuses. Especially fuses of operation class gR can limit and interrupt a faulty circuit in less than half a cycle and before the fault current has enough time to reach its maximum value.
As illustrated in Figure 8.4.13 above, the cut-off or let-thru current i_p is the current flowing through a fuse while the fuse is interrupting a fault within its current-limiting range.
This current value is shown in the fuse data sheets as a diagram of instantaneous peak value I_p as a function of the prospective, symmetrical RMS fault current (Figure 8.4.19).

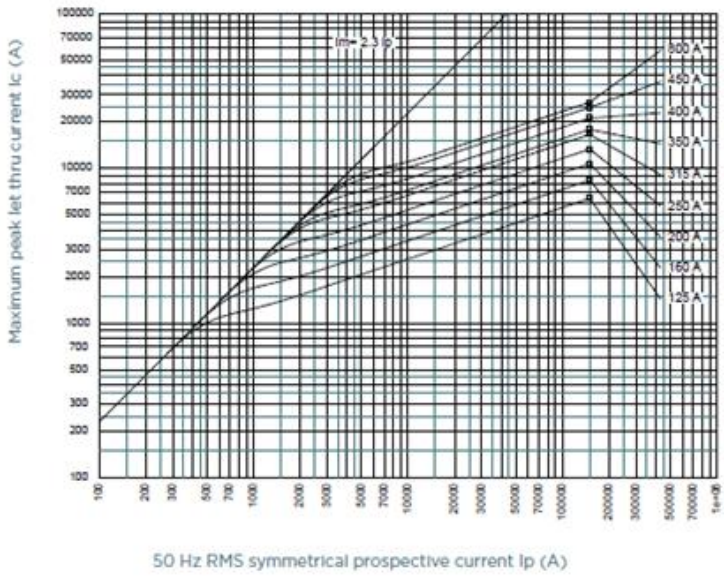


Figure 8.4.19 Cut-off (Let-thru) current characteristic curves of 690V gR size 71 square body fuses [8.33]

The steeper sloping line (Maximum prospective current) represents the highest peak current possible in the circuit without a fuse. The ratio between the available peak current value and the RMS value of prospective current I_P depends on the applied voltage, the short-circuit closing angle and the circuits cos φ. It can assume values between $\sqrt{2}$ and $2 \cdot \sqrt{2}$ at cos φ between 0.15 and 1. Diagrams of the manufacturers usually refer to cos φ = 0.15 or a factor of about 2.3 between the peak value of available current and the RMS value of prospective current.
The flatter sloping line is the characteristic curve of the fuse. It shows the peak let-thru currents to which the fault current is limited by the fuse depending on the prospective fault current I_P and the certain magnitude of I_P, relative to the fuse's I_n is needed before the current-limiting effect will take place. Further information can be found, for example, in [8.29].

Rated breaking current (Interrupting rating)

During the arcing period, the fuse absorbs a large amount of energy. The rated braking current value defines a fuse's ability to safely interrupt and clear short-circuits as the "the highest current at rated voltage that an overcurrent protective device is intended to interrupt under standard test conditions". This rating is much larger than the fuses rated current I_n and mostly identical for fuses of one size. For more detailed information please refer to [8.28].

Power dissipation (Watt Losses) @ rated current

The rated power dissipation within a fuse is given in the data sheet tables under certain conditions.

8.4.7.3 Simplified approach for a fuse selection

For the protection of thyristors or diodes, their permitted overload current value must be higher than the fuse's peak let-through (cut-off) current at the end of the respective overload time, specified by the application.
Using the example of 3 thyristor modules SKKT273/16E in a B6 rectifier bridge application with 320A input current and a permissible overload of 480A for 10 minutes, the initial selection of suitable mains fuses is briefly described below. For exact dimensioning, please refer to the previous chapters. For the example, a square body fuse with I_n = 350A from the 690V gR size 71 series from Mersen [8.33] has been preselected, the suitability of which must be checked. The first verification step shown in Figure 8.4.20 is carried out using the time-current characteristic curves for the fuse described based on Figure 8.4.18.

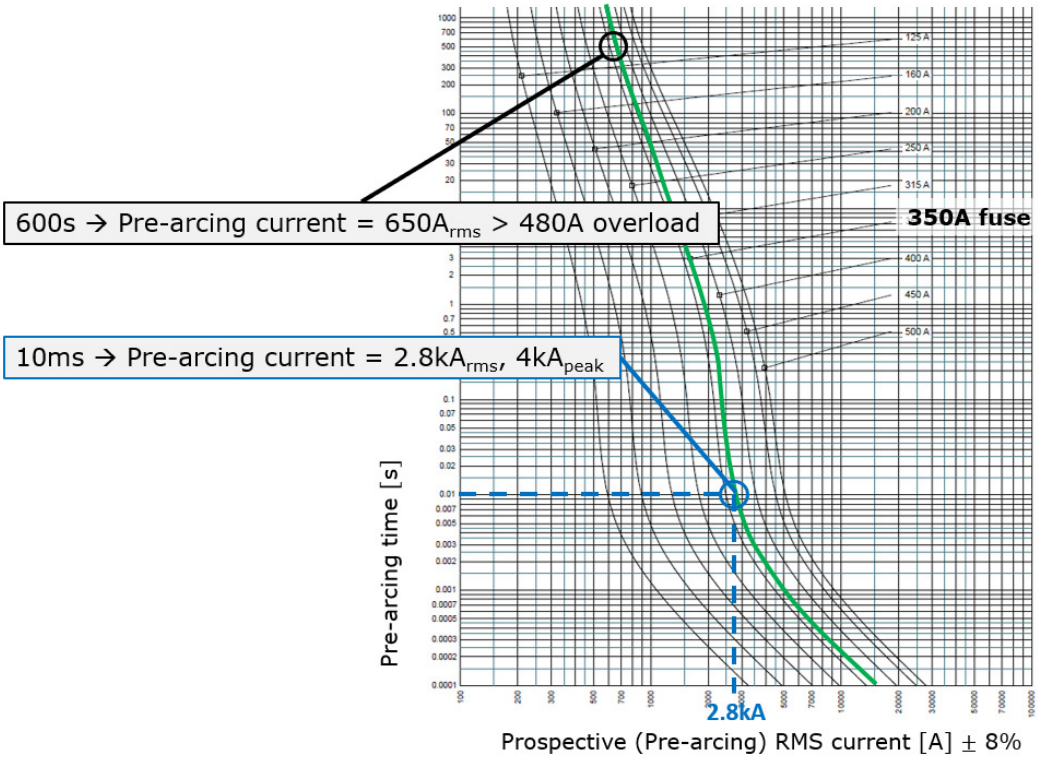


Figure 8.4.20 Determination of the Pre-arcing current (fuse starts to melt)

Results:

- *The fuse must not melt at the permissible RMS overload current of 450A for 10 minutes. → For 600s the pre-arcing current must be larger than 450A.*
- *For the conduction half period of 10ms, the pre-arcing RMS current is 2.8kA → peak value 4kA.*

The next step is to calculate the maximum peak let-through (cut-off) current, described based on Figure 8.4.19. For the example, Figure 8.4.21 Illustrates the procedure.

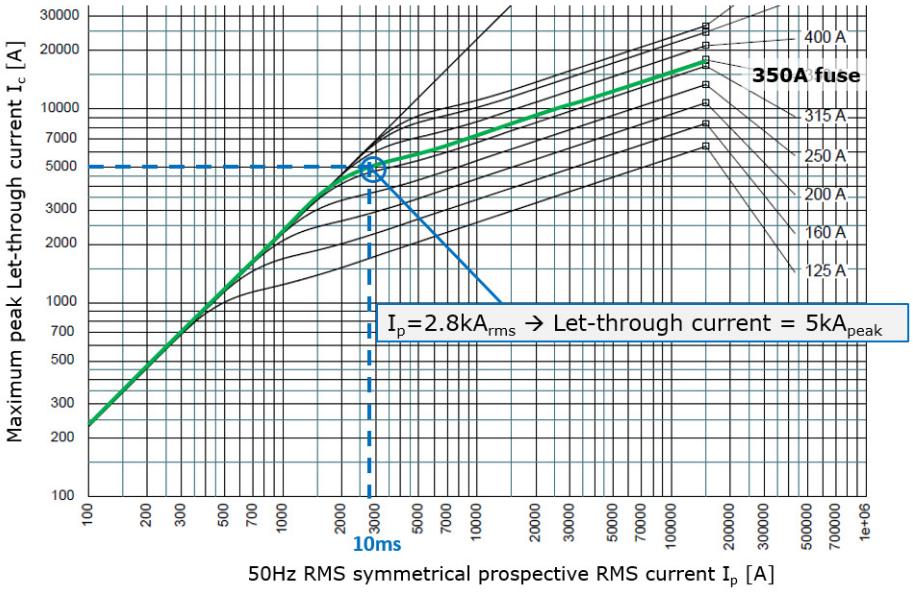


Figure 8.4.21 Determination of the maximum peak Let-thru (cut-off)) current

Result:

- *For the value 2.8kA of the 50Hz RMS symmetrical prospective RMS current I_p and 10ms conduction time, the maximum peak Let-thru current I_c of the selected 350A fuse is approx. 5kA.*

The next step is to check whether the fuse can adequately protect the thyristor. From the diagram "Surge overload current vs. time" included the diode or thyristor data sheet, the permissible peak value of the current can be determined as a function of the overload duration, see Figure 7.2.21 in chapter 7.2.4 and related explanations. Depending on the fault case, the curve for $V_R = 0.5 \cdot V_{RRM}$ (with DC-link at rectifier bridge output) or $V_R = 0 \cdot V_{RRM}$ (AC controller applications) may be used: The surge overload current value $I_{T(OV)}$ – permitted for the applied thyristors or diodes - must be higher than the fuse's peak let-through (cut-off) current at the end of the respective overload time, also specified by the application. For the example, Figure 8.4.22 illustrates the checking procedure for the case that DC voltage is still present after the short circuit, which is divided between both semiconductors of a halfbridge.

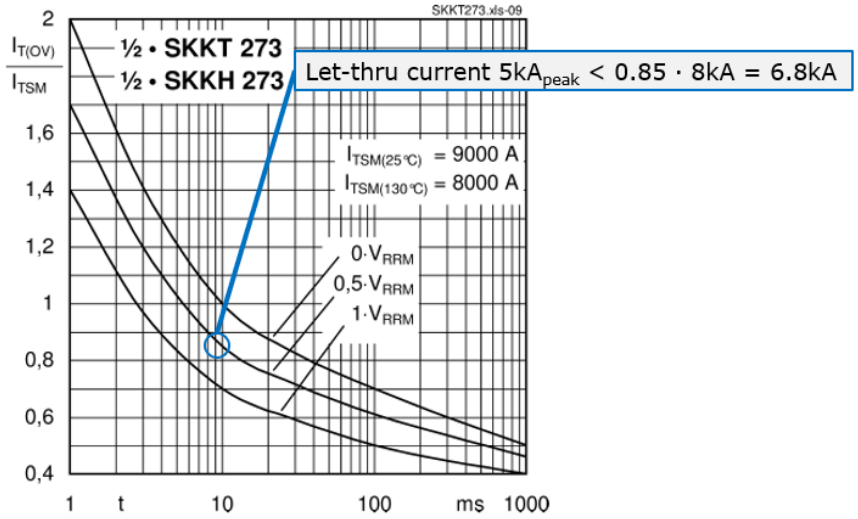


Figure 8.4.22 Checking the protective function of the selected fuse using the surge overload characteristic of the thyristor

Result:

- *The 350A fuse's maximum peak Let-through (cut-off) current I_c of 5kA is lower than the permissible overload current of the thyristors inside the module SKKT273/16. Therefore, the selected mains fuses will probably be able to protect the B6 rectifier bridge.*

The same procedure should be done for 1ms pre-arcing time current (here the peak let-through current is relevant) and for 100ms pre-arcing time (here both currents, peak value of pre-arcing rms current and peak let-though current) should be checked.

8.4.7.4 Protecting DC Circuits

Fuse specifications for DC and AC applications are different and the AC data cannot simply be converted to DC data. Under short-circuit conditions in a DC circuit, the rate of rise (di/dt) of the current depends on the time constant (L/R) of the circuit. Typical time constants are in the range of less than 10ms (DC link) to about 100ms (DC traction motor), normally resulting in a lower rate of rise of the current (di/dt) under short-circuit conditions compared to an AC short-circuit.
Because of the lower di/dt, the fuse takes longer to melt compared to AC conditions, which also results in a longer arcing time. These conditions, as well as the lack of natural current zero crossings, make it more difficult for the interruption of DC faults compared to AC faults. As the L/R time constant in a circuit increase, the DC voltage capability of the fuse decreases. Roughly estimated only 0.5…0.8 times the rated voltage is permissible as maximum DC supply voltage, depending on the fuse type.
The arc energy generated in a DC circuit also varies with the current. For a given L/R, there is a maximum breaking current, a minimum breaking current and a current that causes the maximum arc energy. Some manufacturers publish characteristic curves V_{DC} vs. L/R for the maximum arc energy of the fuse. The minimum breaking currents for DC applications are usually published separately or to obtain on request. Information that is more detailed are included for example in the manufacturer's Technical Explanations, for example in [8.28].

8.5 References

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9 Application Notes for IGBT and SiC MOSFET Modules

9.1 Selection of IGBT and SiC MOSFET modules

The decision for an IGBT or SiC MOSFET module depends on a number of specification points. Criteria for the selection include:

- Which ranges of electrical variables need to be covered (DC link voltage, output current, output power, switching frequency, power factor)
- Topology and control method
- Semiconductor material (Si, Si+SiC SBD, full SiC)
- PCB mounting or AC busbar connection
- Module housing (R_{th}, insulation)
- Robustness (SOA, short circuit capability, humidity robustness)
- Efficiency
- Cost

The following sections deal with selected questions whose answers are necessary for the successful selection of power modules with IGBT or SiC MOSFET. Corresponding information for diodes and thyristors is already contained in chapter 8.1.
The selection of power modules for a specific application must take into account their

- Voltage carrying capacity (reverse voltage, insulation voltage)
- Current carrying capacity, taking into account
  - the forward current
  - the switching frequency
  - the power factor range

in all stationary and short-term operating cases (e.g. overload).
In no stationary or dynamic operating case may the load cause the limit values for reverse voltage, peak current, chip temperature and maximum permissible operating point curve specified in the data sheets to be exceeded. The same applies to the limits of the module housing (e.g. insulation voltage, vibration resistance, climate resistance - see climatic classes given in the technical explanations of the product families, mounting instructions).
In the interest of high reliability and sufficient lifetime, the utilization of the modules must also take into account the intended number of switching cycles during which significant temperature changes occur (see chapters 6.1and chapter 4).
As already explained in the previous sections, many properties of the power modules change with temperature. Furthermore, dimensioning for "normal operating cases" is not based on the thermal load of the semiconductors up to the limit value T_{jmax} in order to retain a margin for overload cases and to be able to fall back on the static and dynamic characteristic values guaranteed in the data sheets for T_{jmax} - 25K.

9.1.1 Preselection and estimation

The decision for a power module must fulfil both the technical and commercial requirements. A rough pre-categorization is already made on the basis of the maximum DC link voltage and the maximum output current. The commutation voltage should be a maximum of 2/3...3/4 of the reverse voltage class in order to reliably turn-off overcurrent. Depending on the switching frequency and cooling, the specified output current will be in the range of 60...80% of the nominal module current.
The voltage class, the degree of pollution and the overvoltage category place requirements on the clearances and creepage distances of the insulation coordination and therefore also the respective height of the module housing. The level of the output current determines whether it can be reliably routed via a printed circuit board or whether a module with busbars must be used.
One of the main criteria when deciding on the semiconductor material is efficiency. The use of SiC leads to lower overall losses at the same switching frequency, which means that the cooling effort can be reduced. Alternatively, the switching frequency can be increased in order to take advantage of the lower filtering effort and the associated weight and cost savings while maintaining the same cooling effort. The topology is particularly relevant to the question of 2-level or 3-level. Are the high costs of a full SiC MOSFET 2-level topology compared to a 3-level topology with Si IGBT compensated for by the savings in circuitry (drivers)?

The following example provides an introduction to the preselection of modules. A 3-phase inverter with 100kW output power should not exceed a sink temperature of T_s = 100°C at a cooling temperature T_a = 40°C and an efficiency of 99%. What thermal resistance $R_{th(s-a)}$ is required for this?
Figure 9.1.1 shows the respective formulas and the curves. With increasing efficiency and permitted sink temperature, the cooling requirement decreases ($R_{th(s-a)}$ increases). For the above specification, a thermal resistance $R_{th(s-a)}$ = 0.06K/W is required.

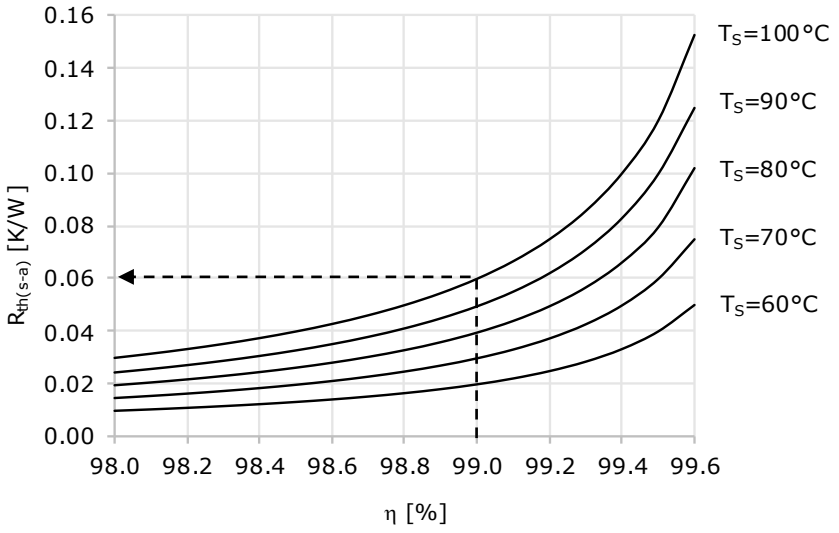
Formulas	Thermal resistance as function of efficiency and sink temperature
$R_{th(s-a)} = \frac{T_s - T_a}{P_{loss}}$ $P_{loss} = P_{out}\left(\frac{1}{\eta} - 1\right)$ $R_{th(s-a)} = \frac{T_s - T_a}{P_{out}\left(\frac{1}{\eta} - 1\right)}$ $T_a = 40°C$ $P_{out} = 100kW$ Parameter: • T_s • η	

Figure 9.1.1 Required $R_{th(s-a)}$ as a function of the efficiency and the maximum T_s

Table 9.1.1 shows the different options for the semiconductor materials used.

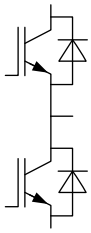
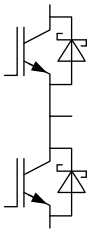
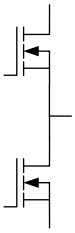
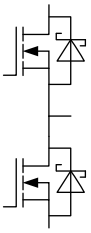
Si (Standard)	Si+SiC SBD (Hybrid)	SiC MOSFET	SiC MOSFET + SiC SBD
			
Si-IGBT ⇄ Si-Diode	Si-IGBT ⇄ SiC SBD	SiC-MOS ⇄ Body Diode	SiC-MOS ⇄ Body Diode||SiC SBD

Table 9.1.1 Commutation partners IGBT/MOSFET and diode in Si and SiC versions

The commutation partners Si-IGBT and Si-diode are standard. The hybrid solution, in which the Si diode is replaced by a SiC SBD, has the following advantages:

- Negligible switching losses of the SiC SBD compared to the Si diode
- Reduction in IGBT turn-on losses due to the almost non-existent storage charge of the SiC SBD

At the same switching the resulting reduced switching losses lead to

- an increase in efficiency
- reduced system temperatures (junction, driver, heat sink)

Alternatively, the cooling effort could be reduced in order to save costs.
Figure 9.1.2 shows measured switching losses (E_{on}+E_{off}) for above mentioned commutation partners.

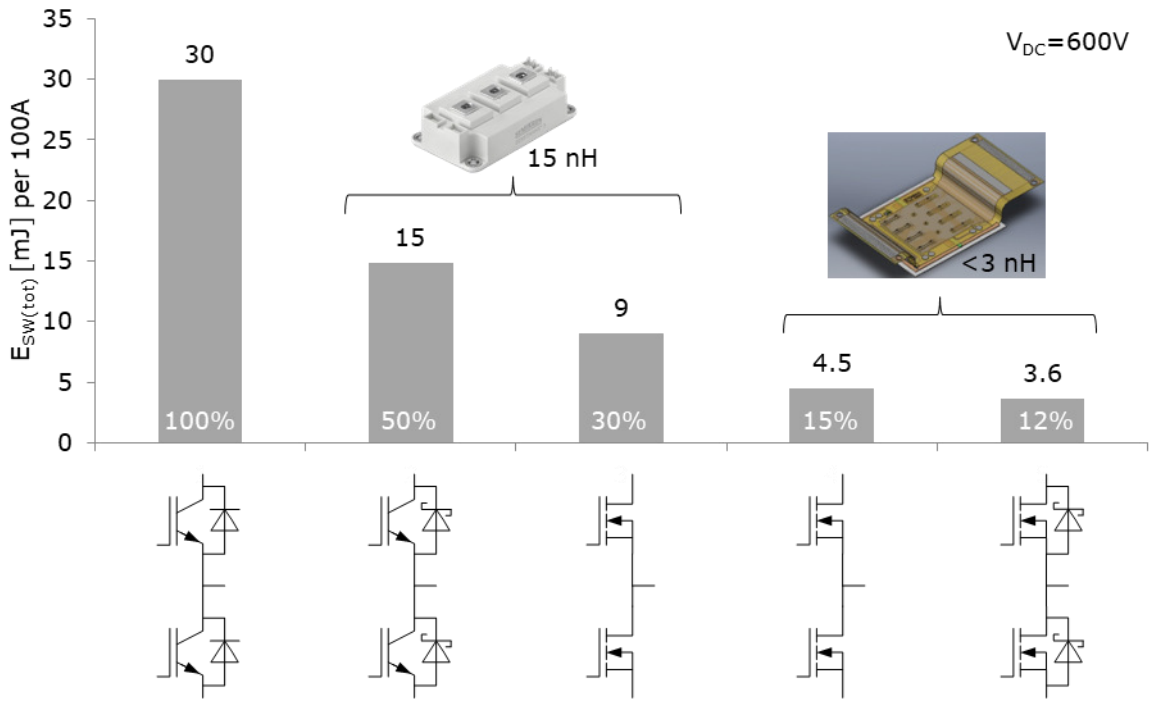


Figure 9.1.2 Comparison of Switching Losses of 1200V Devices

Power modules are available on the market in various circuit configurations in order to create a variety of compact applications. The focus is on a low-inductance design to enable short commutation paths. The realisation of a halfbridge (GB) with two single switches (GA) is only recommended if there is no equivalent halfbridge with two switches in one housing.
Table 9.1.2 and Table 9.1.3 show representatives of standard modules for the implementation of typical 2-level and 3-level topologies.

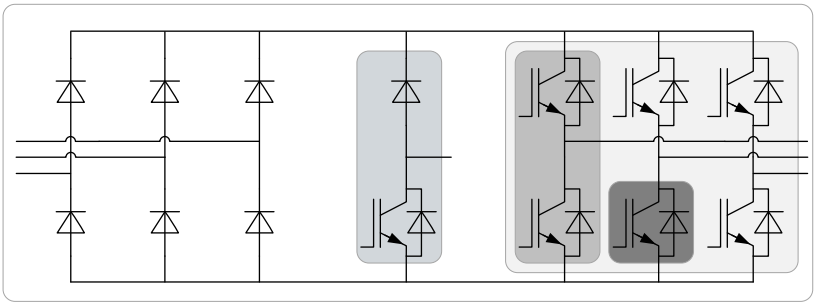
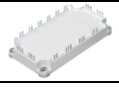
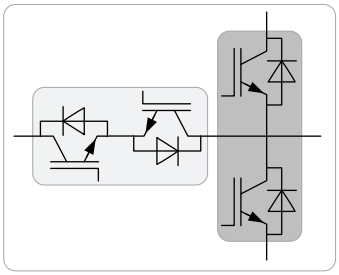
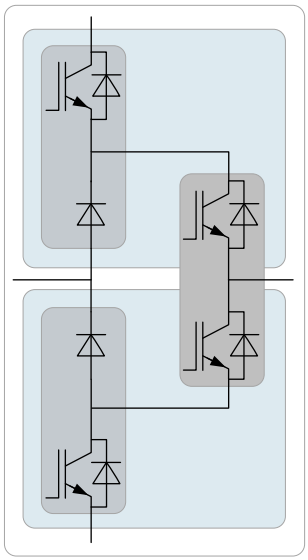
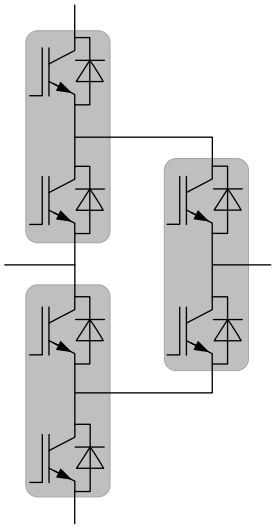
2-Level topologies				
				
All-in-One	3-phase inverter	Buck/Boost	Halfbridge	Single switch
NAB/CIB	AC/GD	GAR/GAL	GB	GA
				
				
				

Table 9.1.2 Typical power electronic topologies - input rectifier, brake chopper and 3-phase inverter as well as their respective realisation with standard halfbridges

3-Level topologies		
TNPC	**NPC**	**ANPC**
		

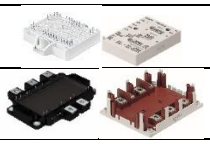
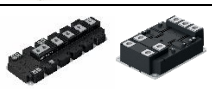
All-in-one	GM	GAR/GAL	TOP/BOT	GB
				
				
				

Table 9.1.3 Typical 3-level topologies TNPC, NPC and ANPC and their respective realisation with standard halfbridges (GB, GM, GAR, GAL), split-NPC (TOP/BOT) or all-in-one modules

Semiconductor chips are optimized for different switching frequencies. Figure 9.1.3 shows a basic simplified representation of a technology curve. The switching losses (E_{off} / E_{rr}) are plotted against the conduction losses ($V_{CE(sat)}$ / V_F).

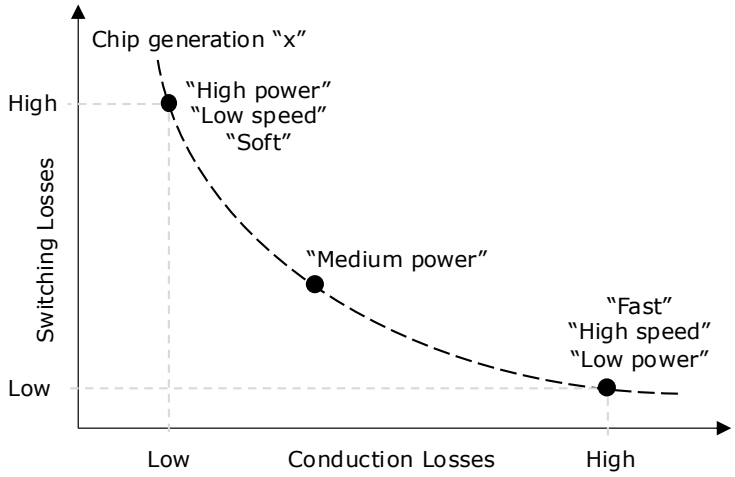


Figure 9.1.3 Simplified technology curve of a chip generation with differently optimized chip variants

Switches with low switching losses are selected for high-frequency applications. Depending on the respective technology curve, low switching losses are accompanied by increased conduction losses and vice versa. For applications with a low switching frequency (e.g. wind application f_{sw} = 2kHz, high output currents), it makes sense to use chips that are optimized for low conduction losses, as these will account for the majority of the switching losses.

Table 9.1.4 shows modules with different chip optimization, the rated current I_C and the internal module inductance. The figure of merit $I_C \cdot L_{CE}$ is an indicator of the corresponding chip technology. The larger the slower, the smaller the faster the chip should/can be switched. The values given are only intended as a guide within the same chip technology. They do not represent a fixed value for a corresponding chip optimization. Even the smallest module with the lowest inductance does not always use the fastest chip. This is due to the switching frequency in the application. If the switching frequency of an application is below 10kHz, then a T4 chip can also be used instead of an F4 chip, even if there is no problem with overvoltage.
Which chip is used in an application depends on the ratio of switching and conduction losses.

Description	Module	I_C [A]	L_{CE} [nH]	$I_C \cdot L_{CE}$ [nVs]
SK200TMLI12**F4**TE2		200	14	2800
SEMiX155GD12**T4**		150	20	3000
SKiiP39GB12**E4**V1		400	15	6000
SKiiP2414GB12**E4**		2400	4.5	10800
SKM1400GB12**P4**		1400	10	14000

Table 9.1.4 IGBT modules with different chip optimisation

The explanations mentioned above are based on IGBT4/1200V chip technology (Table 9.1.5). In principle, they can also be transferred to other chip technologies and voltage classes.

IGBT4/1200V	High Speed	Low Power	Medium Power	High Power
Indication	…12**F**4	…12**T**4	…12**E**4	…12**P**4
Switching speed (di/dt) switching frequency	fastest			slowest
figure of merit $I_C \cdot L_{CE}$	lowest			highest

Table 9.1.5 Identification of IGBT chip optimisation and properties with regard to switching speed, switching frequency, figure of merit $I_C \cdot L_{CE}$

Table 9.1.6 summarizes the frequency range, the output power and the chip variants recommended for these applications as examples. The associated product line lists potential module families that are suitable for these operating conditions.

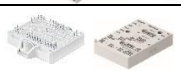
Application	Switching frequency	Output Power per unit	Chip variant	Product line
Solar – string	15…20kHz	…250kW…	S7/L7	
Solar – central	<10kHz	…500kW…MW	E4/P4	
Wind	<5kHz	500kW…MW	E4/P4	
UPS	18…27…kHz	…50kW…	F4/T4	
Drive	<10kHz	kW…MW	T4/E4/P4	

Table 9.1.6 IGBT chip variants and product lines for selected applications and their application area of use (f_{sw}, P_{out})

9.1.2 Consideration of selected criteria

9.1.2.1 Blocking voltage

As the majority of power modules operate on a DC link that is fed from an AC grid via single-phase or three-phase rectifier bridges (see Table 9.1.2), the blocking voltages of the IGBT and MOSFET modules for general-purpose use (e.g. 600V, 1200V, 1700V) are matched to common grid voltage levels.
In the first selection step, a rough selection is therefore first made from the mains voltage (control angle 0° for controlled rectifiers) V_N or open-circuit DC voltage V_{CC} (V_{DD}) in the DC link as shown in Table 9.1.7 as follows:

V_N [V]	Rectification	V_{CC}, V_{DD} [V]	V_{DSS}, V_{CES} [V]
125	B2	110	200
200...246	B2	180...221	500, 600
400...480	B6	540...648	1200
575...690	B6	777...932	1700

Table 9.1.7 Mains voltage levels, ideal open-circuit DC voltages and recommendations for the selection of IGBT or MOSFET modules

It must then be checked whether in the case of the highest voltage load, i.e.

- rectified value of the highest steady-state input voltage (nominal voltage + mains voltage tolerance) or output voltage of an active mains rectifier (see section 9.1.2.3) or PFC boost converter
- transient mains overvoltage, unless dissipated in mains filters, DC link capacitors and DC side circuits (suppressor diodes, snubbers, varistors)
- DC link voltage peaks due to oscillations between the inductances and capacitances of the power supply, e.g. line filters, chokes, capacitors) in certain operating cases
- Limiting voltage of a DC link chopper, if available,
- Turn-off overvoltage (using IGBT as an example) $V_{CC} + \Delta V$ with

$$\Delta V \approx L_\sigma \cdot \frac{0.8\, I_{max}}{t_f(I_{C(max)})}$$

L_σ: Sum of all parasitic inductances in the commutation circuit
I_{max}: Highest collector current to be switched off (usually with active short circuit turn-off)
$t_f(I_{C(max)})$: Fall time of collector current at $I_{C(max)}$

the blocking voltage is not exceeded.
In most data sheets, the limit values V_{CES} or V_{DSS} are specified as chip limit values and not as module limit values. The internal module inductance L_{CE} or L_{DS} (e.g. 20...30nH), which is also included in most data sheets, is part of L_σ.
This means that the highest voltage $V_{CE(max,T)}$ or $V_{DS(max,T)}$ occurring at the module terminals must be limited to e.g.

$$V_{CE(max,T)} \leq V_{CES} - L_{CE} \cdot \frac{0.8 \cdot I_{C(max)}}{t_f(I_{C(max)})}$$

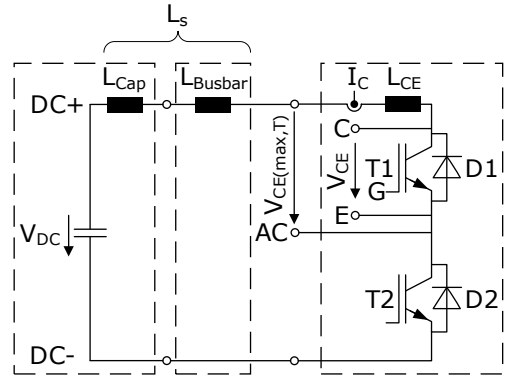
i.e. for the DC link voltage including all possible stationary or transient overvoltage, e.g.

$$V_{CC(max)} \leq V_{CES} - L_\sigma \cdot \frac{0.8 \cdot I_{C(max)}}{t_f(I_{C(max)})}$$

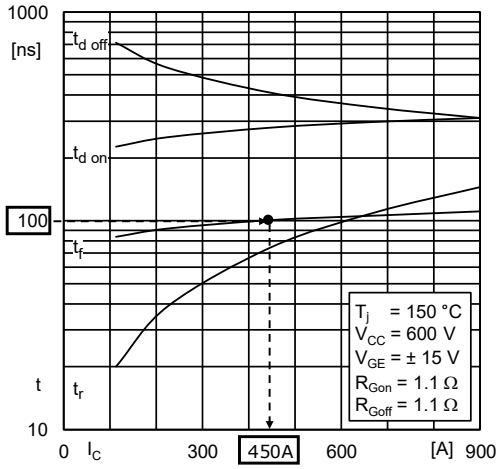
must be observed, see chapters 7.3 and 7.5.

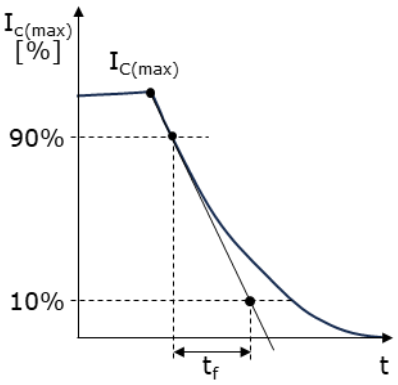
Table 9.1.8 shows the determination of the maximum terminal voltage based on the datasheet parameters of the SEMiX453GB12M7p module. The current slope is determined between 10% and 90% of the collector current. The diagram for the switching times can be used to determine the associated fall time (in the example t_f = 100ns) for the respective collector current (450A in the example). The maximum voltage to the terminals can be calculated using the additional data sheet information on the module inductance L_{CE} = 20nH and the DC link setup used for the measurement (L_S = 25nH).

SEMiX453GB12M7p



SEMiX453GB12M7p datasheet values:
L_{CE} = 20nH
L_S = 25nH





$$\frac{di}{dt} = \frac{(90\% - 10\%) \cdot I_{C(max)}}{t_f} = \frac{0.8 \cdot I_{C(max)}}{t_f}$$

$$\frac{di}{dt} = \frac{(90\% - 10\%) \cdot I_{C(max)}}{t_f} = \frac{0.8 \cdot 450A}{100ns} = 3.6\frac{kA}{us}$$

$$V_{CE(max,T)} \leq V_{CES} - (L_S + L_{CE}) \cdot \frac{di}{dt}$$
$$\leq 1200V - (25nH + 20nH) \cdot 3.6\frac{kA}{\mu s}$$
$$= \mathbf{1038V}$$

Table 9.1.8 Determining the maximum terminal voltage using the example SEMiX453GB12M7p

For IGBT modules, the voltage applied to the chips can be approximately verified by performing measurements between the terminals C_x and E_x (Figure 9.1.4). Further investigations can be found in [9.1] and [9.2].

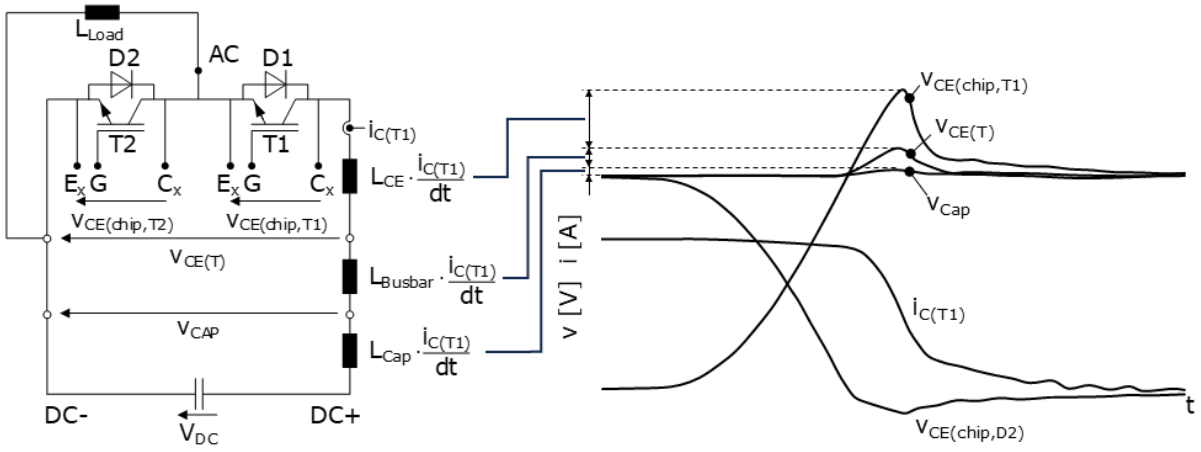


Figure 9.1.4 Measurement determination of the overvoltage during IGBT T1 turn-off

Figure 9.1.5 shows the dependence of the overvoltage peak on the turn-off current I_C, the DC link voltage V_{DC} and the DC link inductance L_S at a junction temperature T_j = 25°C and $R_{G(off)}$ = 1.1Ω. The lower voltage rise at higher currents is characteristic. Here the chip exhibits a kind of clamping behaviour.

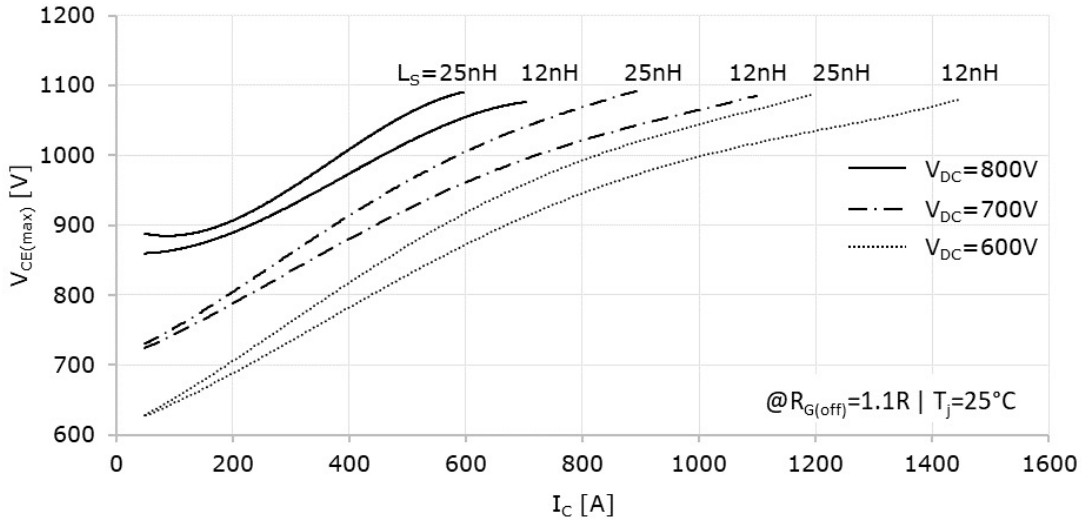


Figure 9.1.5 Dependence of the overvoltage peak $V_{CE(max)}$, parameter I_C, V_{DC}, L_S (SEMiX453GB12M7p)

For V_{DC} = 600V and three different turn-off currents $I_{C(off)}$, the increasing clamping behaviour is shown in Figure 9.1.6. The overvoltage curve flattens out as the turn-off current increases.

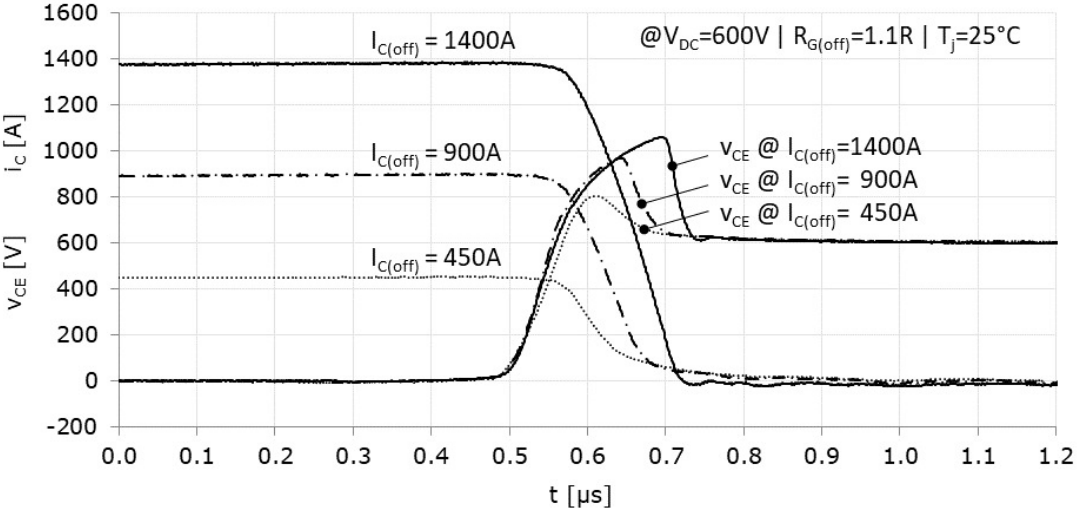


Figure 9.1.6 Time curves of turn-off current i_C and voltage v_{CE} (SEMiX453GB12M7p)

Figure 9.1.7 shows the dependence of the di/dt_{off} on the DC link voltage V_{DC}. The three curves are almost congruent. This means that the overvoltage is almost independent of the DC link voltage.

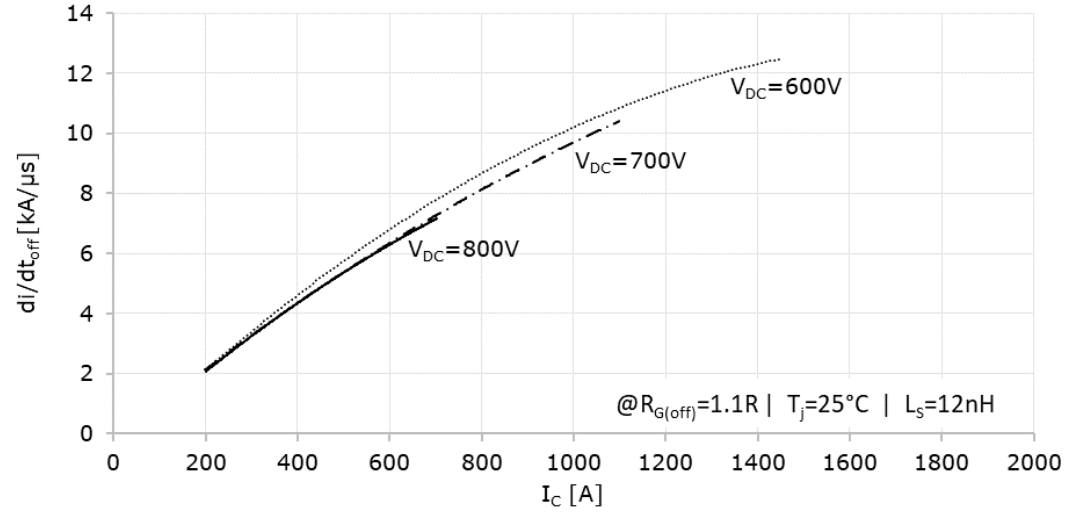


Figure 9.1.7 Collector current dependence of the di/dt_{off}, parameter V_{DC} (SEMIX453GB12M7p)

Figure 9.1.8 shows the influence of the turn-off resistance $R_{G(off)}$ on the overvoltage peak for 25°C and 150°C. The overvoltage increases from nominal values up to approx. 6R and then decreases again. The M7 chip therefore shows similar behaviour to the IGBT4. In addition, it must be taken into account that the di/dt increases as the temperature falls and therefore the overvoltage increases.

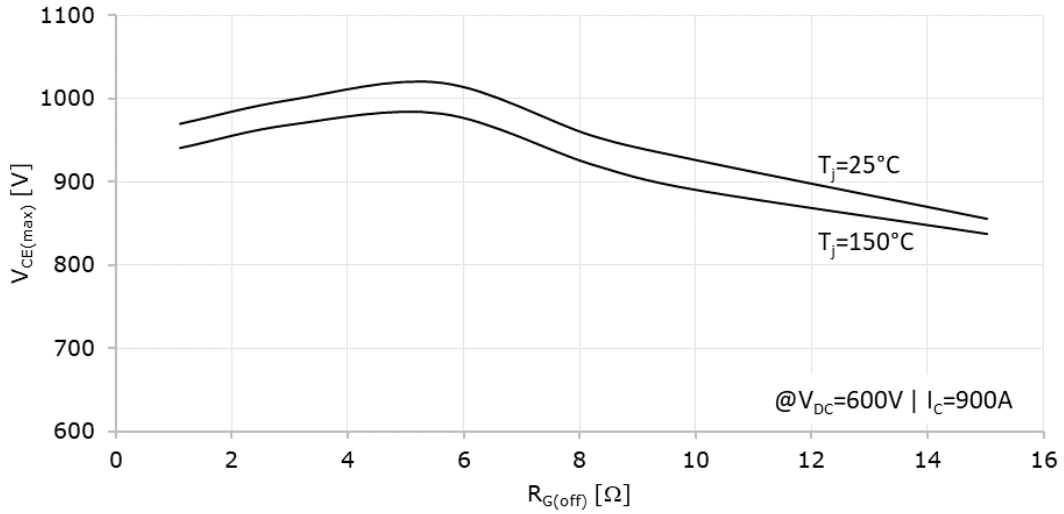


Figure 9.1.8 Overvoltage peak as a function of the $R_{G(off)}$, parameter T_j (SEMiX453GB12M7p)

One positive aspect can be seen by an increased stray inductance, it decreases the turn-on energy E_{on} because of an higher voltage drop $L_S \cdot di/dt$. Furthermore is the di/dt lower, which reduces the diode losses E_{rr}, so that the overall switching losses $E_{sw}=E_{on}+E_{off}+E_{rr}$ are smaller.

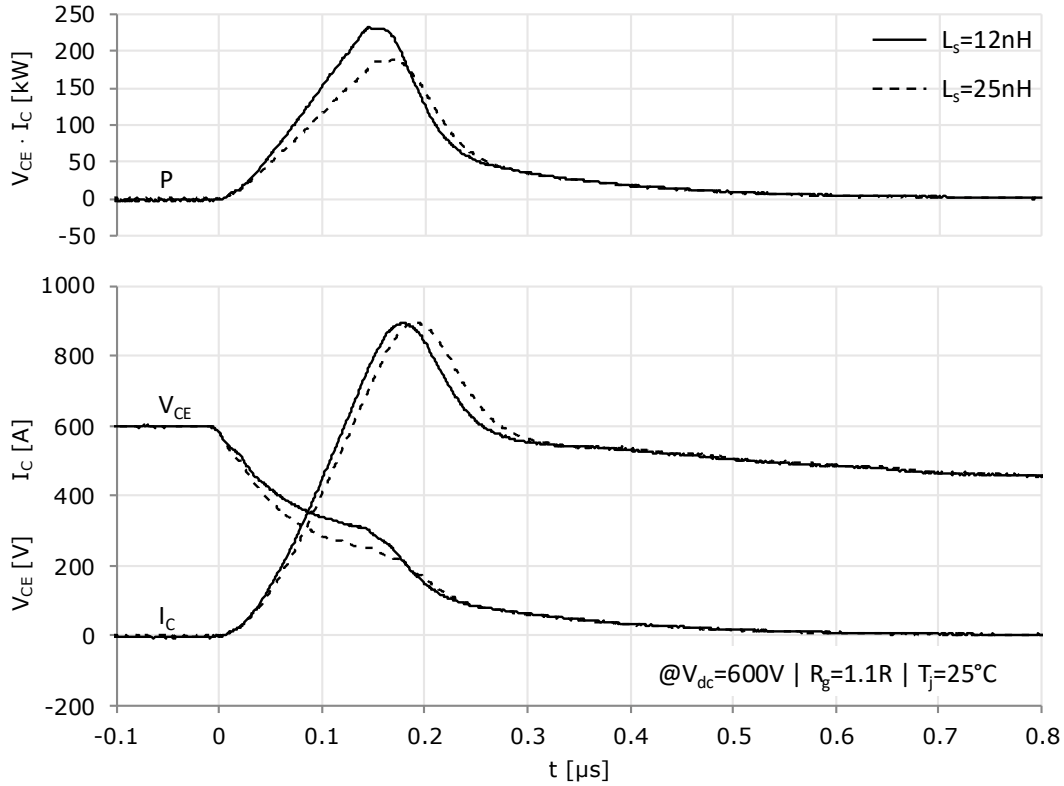


Figure 9.1.9 Curves of I_C, V_{CE} and P during turn-on with different stray inductances in the commutation loop

9.1.2.2 On-state current

The maximum permissible forward direct currents I_C (collector direct current) or I_D (drain direct current) listed as limit values in the data sheets, at which the maximum permissible chip temperature is reached, are formally calculated for the stationary fully controlled transistor according to.

$$I_c = \frac{T_{j(max)} - T_C}{V_{CE(sat)} \cdot R_{th(j-c)}}$$

$$I_D = \sqrt{\frac{T_{j(max)} - T_C}{r_{DS(on)} \cdot R_{th(j-c)}}}$$

for housing temperatures T_c = 25°C and 80°C for modules with base plate or T_s = 25°C and 70°C for modules without base plate, see also explanation of the data sheet specifications in chapters 7.3.2 and 7.5.2.
For modules without a base plate, T_s replaces T_c and $R_{th(j-s)}$ replaces $R_{th(j-c)}$. For $R_{DS(on)}$ and $V_{CE(sat)}$, the maximum values at the maximum permissible chip temperature T_{jmax} are used. These specifications are only suitable for rough orientation, as in real operation, in addition to the conduction losses, switching and (low) blocking losses also occur, the housing temperature will differ and the static end values of $R_{DS(on)}$ or $V_{CE(sat)}$ are not reached during the entire turn-on period.
Details about the IGBT chip current I_{cnom}, the periodic collector current peak value I_{CRM} and the module terminals current $I_{t(RMS)}$ are explained in Chapter 7.3.2.1 and 7.3.2.3.

Analogous to the transistor limit values, the current limit values of the freewheeling diodes are defined as inverse diode forward current I_F, diode chip current $I_{F(nom)}$ and periodic peak value of the inverse diode forward current I_{FRM}.
The (non-periodic) surge current limit I_{FSM} is important for the selection of protective measures when operating inverse diodes as mains rectifiers. It defines the permissible level of a forward current surge in the form of a 50Hz sinusoidal half-wave oscillation which the diode can withstand without damage in the event of a fault (short circuit) if it occurs only rarely during the diode's service life.
Values for different half-wave periods and for several consecutive half-waves can be determined from the limiting overload characteristics (see chapter 7.3.2.2).
The achievable output current of a power electronic circuit in practice is basically limited by the total power loss balance (forward, reverse and switching losses) of the transistors and freewheeling diodes in the power modules and the possible heat dissipation from the chips via the module and the cooling device into the cooling medium:

- The maximum permissible chip temperature of the IGBT, diodes or MOSFET must not be exceeded in any stationary or dynamic operating case (with the exception of short circuit shutdown, which is only permitted a limited number of times)
- The temperature gradients caused by load and temperature changes must not lead to wear-related destruction of the module before the end of the expected module lifetime, see chapter 4.

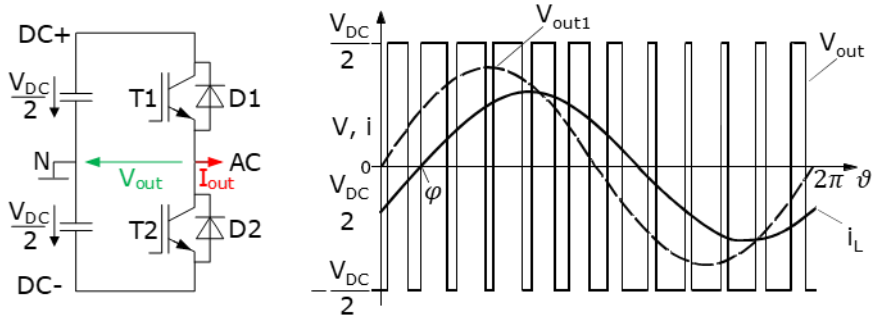
Further limits exist, for example, in

- the switching capacity of the transistors during operation and in the event of possible overloads up to the highest current to be switched off, i.e. in the limits of the permissible operating ranges of the transistors
- the necessary selectivity of active and passive overcurrent protection measures
- switching overvoltage that depend on the current to be switched off

9.1.2.3 Stress conditions of freewheeling diodes in rectifier and inverter mode

In order to be able to feed energy back to the grid, drive converters are often rated for 4-quadrant operation, which means they consist of 2 topologically identical converters at the line side (LSC: Line Side Converter) and at the machine side (MSC: Machine Side Converter). Depending on the direction of current flow (rectifier or inverter mode), the freewheeling diodes of the two converters are under different stresses as regards resultant power dissipation for the same power transmitted. In inverter mode, the average energy flow is directed from the DC link to the AC side, i.e. the AC side supplies a consumer, e.g. a three-phase motor or a power system. On the other hand, the

average energy flow in rectifier mode is directed from the AC side to the DC link. In this case, the converter works as a pulse rectifier connected to an AC mains or generator. Although the power performance in both cases is the same, the power semiconductors are subject to different power losses essentially due to the opposite phase shift between the voltage and current fundamental frequency on the AC side that occurs in rectifier or inverter mode. This can be explained using to the basic circuit in Figure 9.1.10.



If $v_{out}>0$ and $i_L>0$: current flow through T1
If $v_{out}<0$ and $i_L>0$: current flow through D2
If $v_{out}>0$ and $i_L<0$: current flow through D1
If $v_{out}<0$ and $i_L<0$: current flow through T2

Figure 9.1.10 Basic circuit of a converter phase with IGBT and freewheeling diodes

Consequently, the IGBT and freewheeling diode on-state power losses occurring at a given RMS current value are dependent on the cos φ between voltage and current fundamental frequency, as well as on the modulation factor m of the converter (this determines duty cycles).
In inverter mode the following applies: $0 \leq m \cdot \cos \varphi \leq 1$. Power dissipation in semiconductors reaches its limits if $m \cdot \cos \varphi = 1$. In this case, maximum on-state losses and, therefore, total losses in the IGBT have been reached, whereas losses in the freewheeling diodes are at their minimum.
In rectifier mode the following applies: $0 \geq m \cdot \cos \varphi \geq -1$. Power dissipation in semiconductors reaches its limits if $m \cdot \cos \varphi = -1$. In this case, minimum on-state losses and, therefore, total losses in the IGBT have been reached, whereas losses in the freewheeling diodes are at their maximum. Applied to the characteristics in Figure 9.1.10, this situation would be given if the pulse rectifier converts pure active power from the line – referred to the fundamental component – and the neutral point of the line is connected to the centre point of the DC link voltage. Figure 9.1.11 graphically illustrates these interrelations in an example.

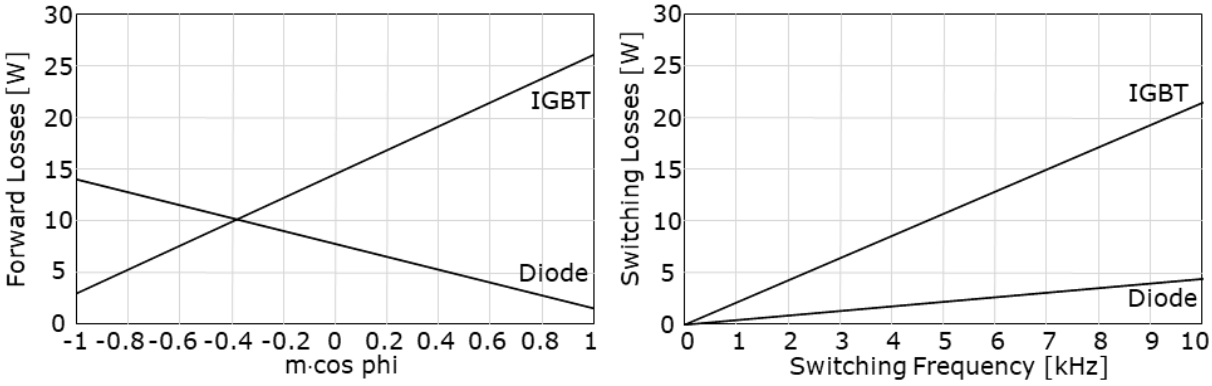


Figure 9.1.11 Switching and forward on-state losses of IGBT and freewheeling diode in a frequency converter (IGBT 1200V / 50A; V_{DC}=540V; $I_{L,RMS}$=25A; T_j=125°C)

At given DC link voltage and RMS AC current values, the switching losses of the components are merely linearly dependent on the switching frequency (Figure 9.1.11). Most available IGBT and MOSFET modules with integrated freewheeling diodes are dimensioned for use in inverters in reference to the power losses that can be dissipated at rated current (e.g. cos φ = 0.6...1). Due to their reduced on-state and total losses, diodes have been designed for a far lower dissipation of power losses than for IGBT (ratio IGBT : Diode ≈ 2...3:1). When dimensioning a converter for use as a pulse rectifier, the diode load must be taken into particular consideration.

9.1.2.4 Switching frequency

Figure 9.1.12 shows the measured turn-on and turn-off behaviour of a power MOSFET and an IGBT module for one specific operating point. Apart from the characteristics for v_{DS} or v_{CE} and i_D or i_C, the instantaneous power dissipation values p(t) have been determined by multiplying instantaneous current and voltage values; the integral of p(t) reflects the total MOSFET and IGBT losses over the entire period. The total losses in the power module are composed of the losses of all transistors and freewheeling diodes contained in the module.

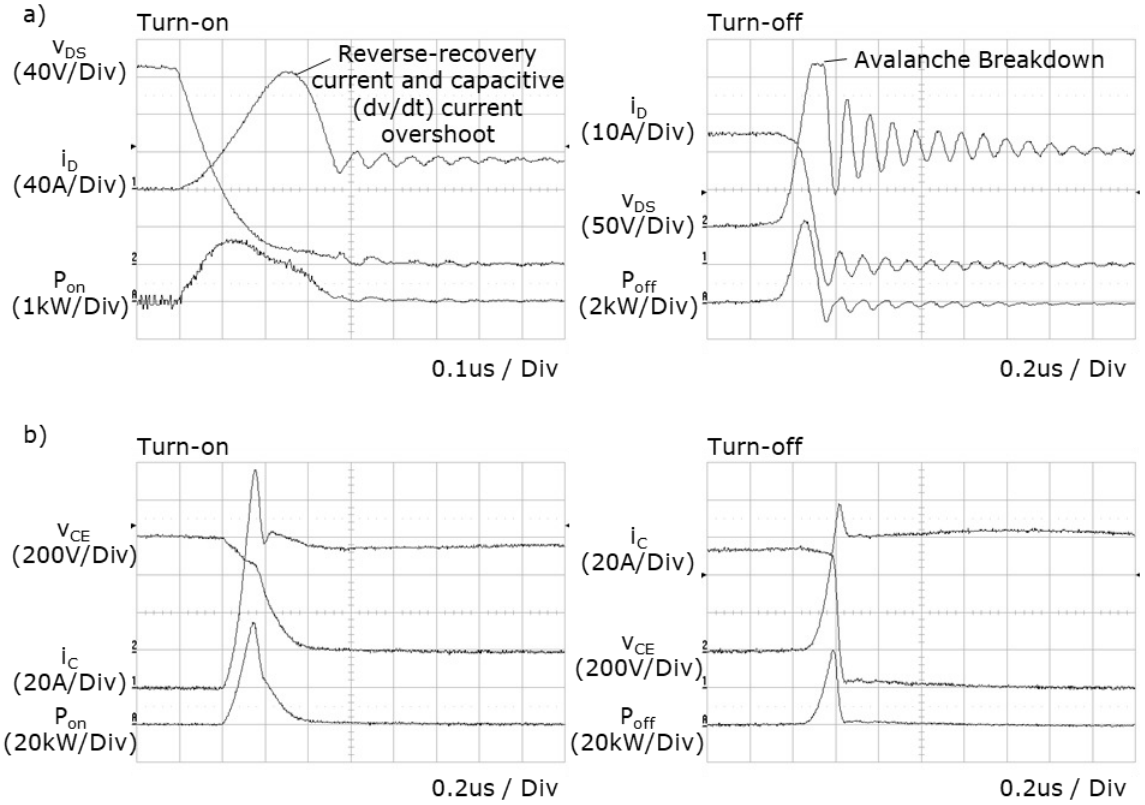


Figure 9.1.12 Measured switching processes (hard turn-on and turn-off under ohmic-inductive load): a) Power MOSFET module; b) IGBT module

A qualitative explanation of current and voltage characteristics is given in chapters 2.4 and 2.5. Since switching losses increase in proportion to the frequency, they limit the switching frequency, although this can still be increased by oversizing the power module.

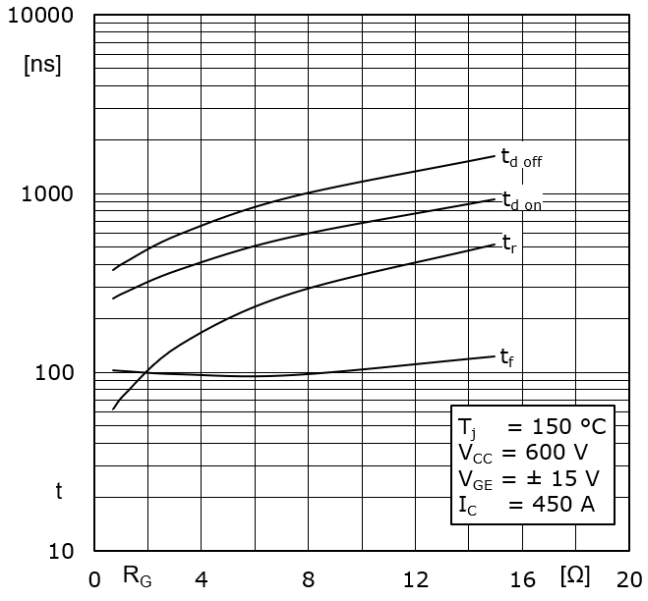


Figure 9.1.13 Switching times of an IGBT7 as a function of the external gate resistor R_G

Other limitations may be set by the transistor turn-on and turn-off delay times $t_{d(on)}$, $t_{d(off)}$, the reverse recovery times of the freewheeling diodes, the driver control power which increases proportionate to the frequency, as well as by the minimum turn-on, turn-off or deadtimes necessary for driver, interlocking, measuring, protection and monitoring functions. If switching losses are to be shifted to passive networks (snubbers) or overvoltage are to be limited by snubbers, the recharge time of such networks required after low-loss switching has to be considered as deadtime.
Switching times of MOSFET and IGBT power modules are within the range of some ns to some 100ns. While the switching times of MOSFET and older IGBT can be influenced within relatively wide limits by control parameters, many new Trench IGBT provide this option for turn-on to a limited extent only and for turn-off barely at all (cf. Figure 9.1.13), unless drastic increases in switching losses – owing to very high gate resistances – are accepted.

Figure 9.1.14 shows the influence of the negative gate voltage on the delay times $t_{d(on)}$ and $t_{d(off)}$. As the gate voltage decreases (-8V → -15V), $t_{d(off)}$ decreases and $t_{d(on)}$ increases. For this reason, the deadtime must be adjusted.
The negative gate voltage has no influence on the losses E_{on}, E_{off}, E_{rr}, because switching on depends on the voltage difference between the gate threshold voltage $V_{GS(th)}$ and the positive driver voltage V_{p+}. Switching off can hardly be influenced by the gate voltage and the gate resistor.

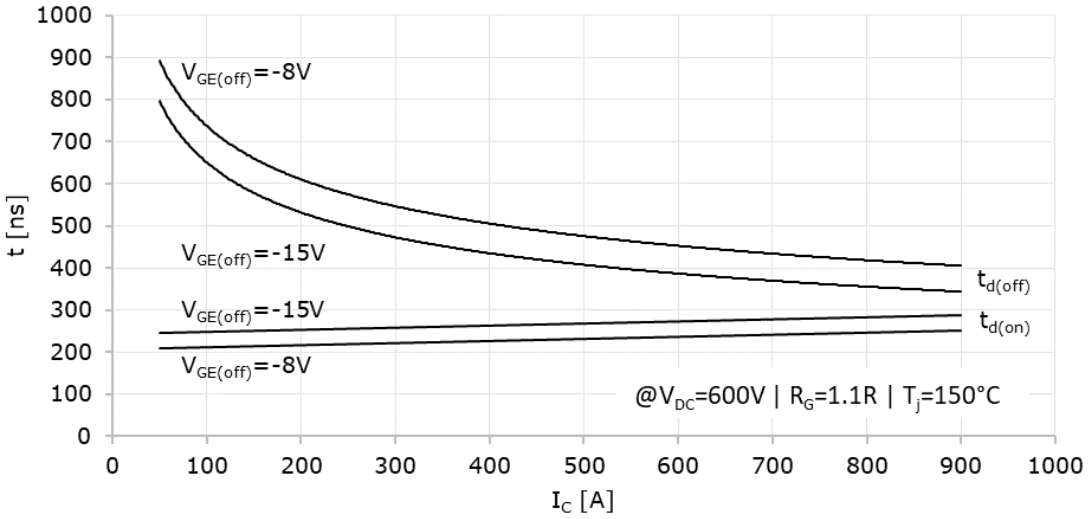


Figure 9.1.14 Influence of negative gate voltage on the delay times $t_{d(on)}$, $t_{d(off)}$ (SEMiX453GB12M7p)

Figure 9.1.15 shows the dependencies of the distortion times $t_{d(on)}$, $t_{d(off)}$ as a function of the junction temperature. As the junction temperature decreases, the times become shorter. The difference between the two remains almost constant.

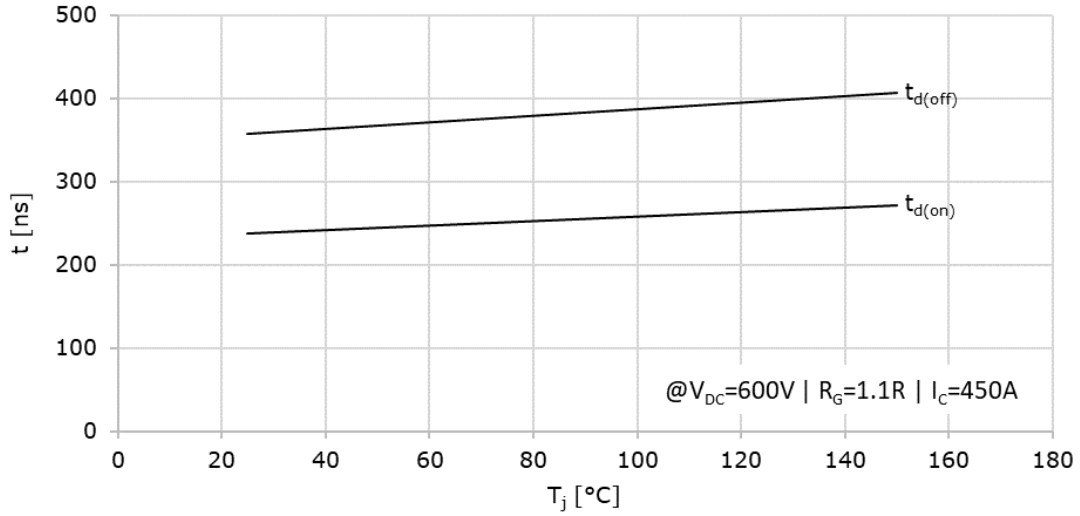


Figure 9.1.15 Dependence of the delay times on the junction temperature (SEMiX453GB12M7p)

As transistor switching time decreases, the influence of parasitic inductances and the real properties of the freewheeling diodes (t_{rr}, Q_{rr}) end to become limiting factors for the switching frequency in case of hard switching and higher operating voltages. This is because, for example,

- the turn-off velocity, limited by the permissible switching overvoltage, and
- the turn-on velocity, limited by the permissible peak current (load current + reverse recovery current of the freewheeling diode depending on di/dt)

often determine the maximum values of the feasible switching speed.
Moreover, transistor dv/dt and di/dt values, which are prone to be too steep within the high power range, might cause electromagnetic interference and dv/dt-dependent insulation problems under certain loads (machines). For this reason, an optimum compromise between the requirements resulting from the application (e.g. frequency out of range of audibility), switching times / losses, power dissipation and EMC features has to be looked for when determining switching frequency and (if possible) switching times.

Today, the following guideline values for switching frequencies in standard modules apply:

For hard switching:	MOSFET modules	low-voltage (various Si MOSFET)	up to 250 kHz
		high-voltage (SiC MOSFET)	up to 100 kHz
	IGBT modules	650 V	up to 30 kHz
		1200 V	up to 20 kHz
		1700 V	up to 10 kHz
		3300 V	up to 3 kHz
For soft switching:	MOSFET modules	low-voltage (various Si MOSFET)	up to 500 kHz
		high-voltage (SiC MOSFET)	up to 250 kHz
	IGBT modules		up to 150 kHz

9.2 Layout, parasitic elements, EMC

Power circuits used to connect power semiconductors and passive components (L, C etc.) are designed in printed circuit board technology, or by means of cables or solid copper or aluminium bars, depending on the currents and voltages to be switched.
Apart from the general specifications to be met, for example with regard to creepage and clearance distances, current density or heat dissipation, the short switching times within the nano to microsecond range call for a power design which also lives up to the requirements related to high-frequency applications. In this context, commutation circuits are of particular importance, because their parasitic inductive and capacitive characteristics have a crucial influence on the overall system behaviour.

9.2.1 Stray inductances and capacitances

To analyse the individual effects of parasitic inductances and capacitances and their interdependence in converters, it suffices to examine one commutation circuit.
Figure 9.2.1 shows the commutation circuit of an IGBT converter with parasitic elements, consisting of DC link voltage V_{DC} (corresponds to commutation voltage V_K) and two IGBT switches with driver and antiparallel freewheeling diodes. The commutation voltage is impressed by the DC link capacitance C_{DC}. The impressed current i_L flows out of the commutation circuit.

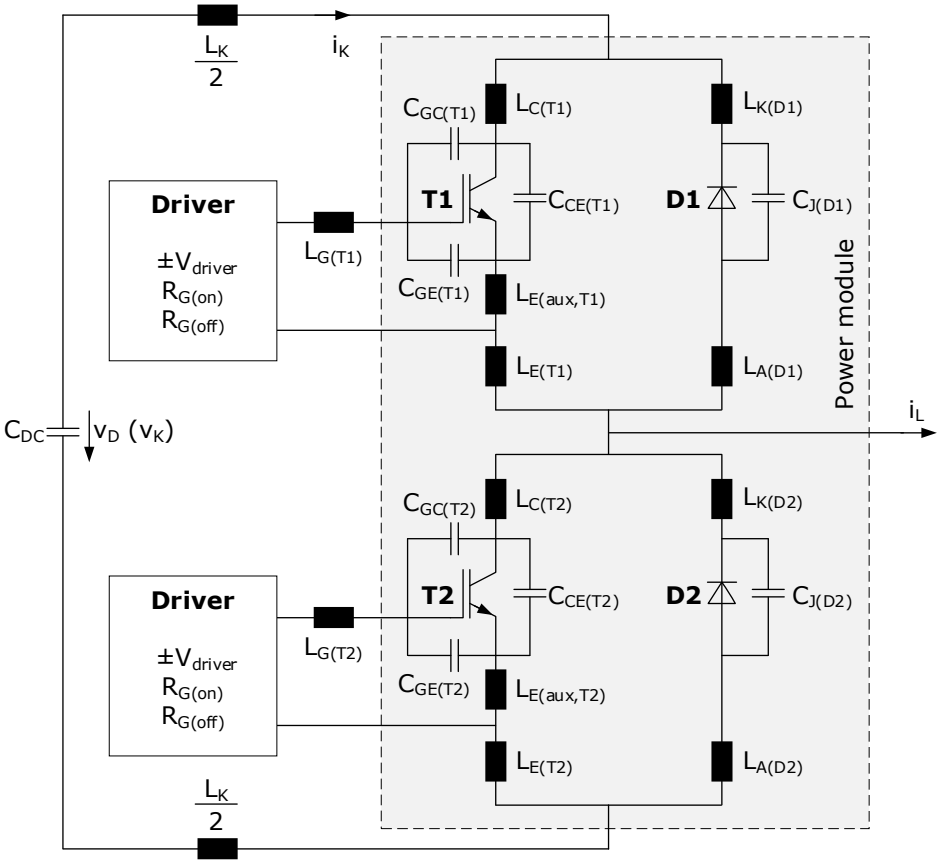


Figure 9.2.1 Commutation circuit with parasitic inductive and capacitive elements

9.2.2 The effects of parasitic elements/counter-measures

9.2.2.1 Total commutation circuit inductance

In the commutation circuit with T1 and D2, the total commutation circuit inductance $L_{T1\text{-}D2}$ is the sum of

$$L_{T1-D2} = 2\frac{L_K}{2} + L_{C(T1)} + L_{E(aux,T1)} + L_{E(T1)} + L_{K(D2)} + L_{A(D2)}$$

In the same way, the sum of

$$L_{D1-T2} = 2\frac{L_K}{2} + L_{C(T2)} + L_{E(aux,T2)} + L_{E(T2)} + L_{K(D1)} + L_{A(D1)}$$

is effective in the commutation circuit with D1 and T2.
During active turn-on of T1 or T2, the total commutation inductance becomes effective as turn-on relief, which will reduce turn-on power dissipation in T1 or T2 (cf. chapter 9.8).
However, during active turn-off of T1 and T2, as well as during reverse-recovery di/dt of D1 and D2, switching overvoltage is generated in the transistors and diodes due to high di/dt caused by the commutation circuit inductances. This increases turn-off power dissipation and voltage stress in the power semiconductors.
This effect is especially critical with regards to short circuits and overload (cf. chapter 9.6).
Moreover, undesired high-frequency oscillations in the range of some MHz may be generated in connection with parasitic capacitances. In hard-switching converters, it is therefore vital that inductances in the commutation circuit be reduced to a minimum.
With the exception of the components $\frac{L_K}{2}$ (DC link connection), these are module-internal inductances over which the user has no influence.
In this respect, it is up to the manufacturers of power modules to keep on working on the minimisation of internal inductances by improving module assembly technologies (cf. chapter 2.4 and 2.5).
Semikron Danfoss datasheets indicate the internal inductances effective at the module output terminals (Example: SEMiX453GB12M7p L_{CE}=20nH).

If several modules are involved in a commutation circuit (single-switch module, 3-level topologies, cf. chapter 9.7), the modules must be connected with as little inductance as possible when implementing an inverter phase or a commutation circuit.
Particularly important here is that the DC link busbars are low-inductive. This applies to the busbars between the DC link capacitors, as well as to the connection of the power modules to the DC link. In relation to this, laminated busbar systems (tightly parallelled plate systems) adapted to the specific converter layout have become widely accepted in practice, achieving busbar inductances of up to 20...50nH.
The effect of the remaining inductances $2\frac{L_K}{2}$ on the power semiconductors can still be reduced by connecting C-, RC- or RCD-circuits directly to the DC link terminals of the power modules (cf. chapter 9.6.2.3). In most cases, a simple C-circuit with film capacitors within the range of 0.1...2µF is connected. In low-voltage high-current applications, attenuated RC-circuits are preferred.

9.2.2.2 Emitter / source inductances

The elements $L_{E(aux,T1)}$ or $L_{E(aux,T2)}$ of the emitter / source inductances are effective in the power circuit, as well as in the driver circuit of the transistors. Due to the fast di/dt of the transistor current, voltages will be induced that will have the effect of inverse feedback in the driver circuit (emitter / source inverse feedback). This, however, will decelerate the charging process of the gate-emitter capacitance during turn-on or the discharging process of the gate-emitter capacitance during turn-off, resulting in increased switching times and switching losses. The inverse feedback effect of the emitter may be utilised to limit the collector current di/dt in the case of short circuits near the modules. To minimise the inductances $L_{E(aux,T1)}$ and $L_{E(aux,T2)}$, power modules are equipped with separate emitter control terminals.
If several BOTTOM driver stages of a converter are supplied by a common operating voltage with negative DC link reference, the parasitic inductances between the ground connectors of the drivers and the negative potential of the DC link may cause undesired oscillations in the ground loops. This problem can be solved by way of HF stabilisation of the driver operating voltage near to the output stage or, in high-power converters, by way of separate supply voltage potentials for the BOTTOM driver stages.

9.2.2.3 Inductances $L_{G(T1)}$ and $L_{G(T2)}$

The inductances $L_{G(T1)}$ and $L_{G(T2)}$ designate the inductance of the supply line between driver and transistor. Apart from increasing the impedance of the driver circuit, they may cause unwelcome oscillations with the input capacitance of the transistor. This may be remedied by using a short, low-inductance connection between driver and transistor. Increasing the gate series resistance may dampen oscillations; this, however, will unintentionally cause an increase in transistor switching losses at the same time. For more details refer to [9.9].

9.2.2.4 Chip capacitances

The capacitances C_{xx} in Figure 9.2.1 stand for the intrinsic capacitances in the power semiconductors (voltage-dependent, non-linear) and cannot be influenced by the user. They indicate the minimum value for commutation capacitance C_K and, generally speaking, cause a reduction in power dissipation during turn-off (cf. chapter 1 and chapter 9.8.).
Additional power dissipation is generated during active turn-on due to the recharge process of the commutation capacitances; in high-frequency MOSFET applications (...>100kHz...), in particular, these losses must be taken into account.
$C_{GC(T1)}$ and $C_{GC(T1)}$ result in the Miller effect, as well as dynamic dv/dt-feedback to the gate that slows down the switching process.
The circuit must be designed such as to prevent strong capacitive coupling between the inductive supply leads to gate and collector / drain as well as to gate and emitter / source outside the module, which is likely to cause additional high-frequency parasitic oscillations. This aspect is becoming increasingly important in fast high-voltage power SiC MOSFET applications.

9.2.3 EMI and mains interference

9.2.3.1 Energy processes in converters

The processes that take place in a converter system will always produce unwelcome interference due to the switching of the power semiconductors, on the one hand (Figure 9.2.2), and welcome energy transmission with corresponding signal processing, on the other hand.

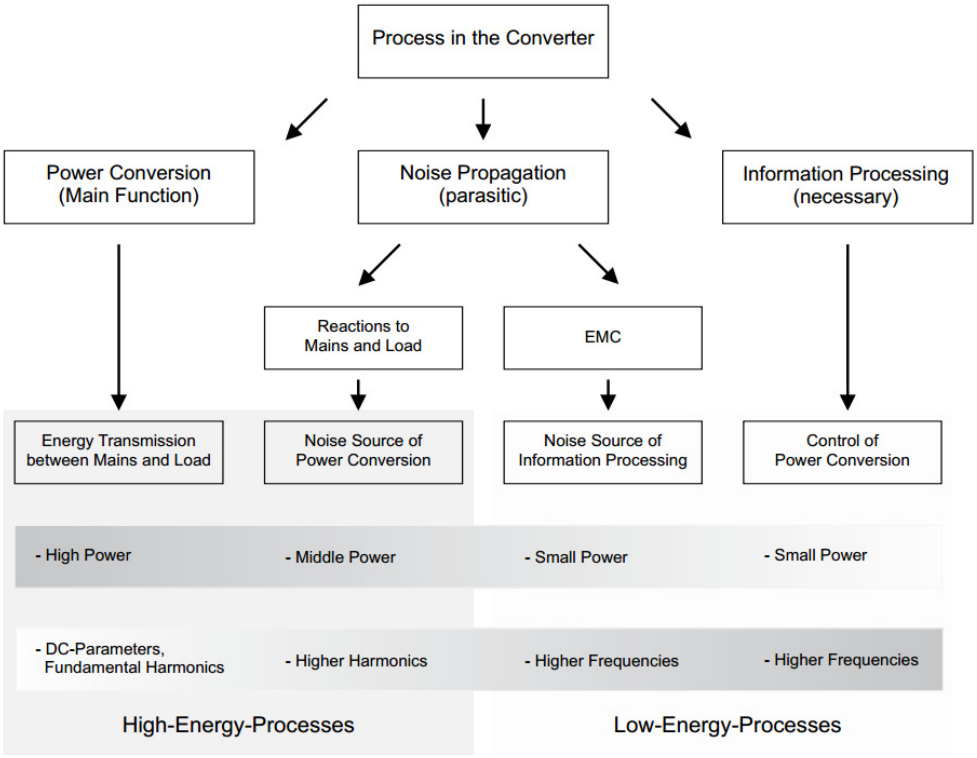


Figure 9.2.2 Energy processes in converters [9.4]

These processes can be divided up into high-energy processes, which may cause interference in the mains and the load within a frequency range between fundamental frequency and about 9kHz, and low-energy processes above 9kHz up to about 30MHz, where noise emission and, consequently, non-conducted current flow will start to be propagated. In the low-frequency range, these effects are called converter mains feedback, which are normally characterised by discrete harmonic current oscillations up to about 2kHz. At higher frequencies, these oscillations are called radio interference voltages or radio interference and are given as interference voltage spectra in dB/mV for reasons of selective measurement. Terms such as zero current, leakage current or asymmetrical interference voltage only differ with respect to their assignment to different frequency ranges and with regards to the frequency dependency of the switching parameters. Since this frequency dependency is continuous, as is the transition to radio interference, the frequency transition range is inevitably very wide.

9.2.3.2 Causes of interference currents

Electromagnetic interference is caused mainly by the switching operation mode of power semiconductors. Causes of interference may be explained by the equivalent commutation circuit in Figure 9.2.3. In the case of inductive commutation, switch S1 will switch over to conducting switch S2. In a hard switching process ($L_K = L_{K(min)}$, $C_K = C_{K(min)}$), the current is initially commutated with a di/dt that is given by the semiconductor characteristics of switch 1. Commutation is finalised by the reverse-recovery di/dt of switch 2, which determines voltage commutation and, consequently, dv/dt along with the current-carrying inductance and the effective capacitances C_K. The effective capacitances comprise all capacitances C_Σ which are effective towards the neutral potential. In addition to the impedances of the commutation voltage connections to the neutral potential, parallel impedances of the commutation capacitances will become effective. At the beginning of the commutation process, the di/dt of switch 1 will cause a symmetrical current flow i_{dm} (differential mode) within the commutation voltage capacitance and the parallel network 1. The dv/dt at the end of the commutation process caused by the reverse-recovery di/dt of switch 2 and the inductance L, which serves as a supply current, conducts the currents i_{cm} (common mode) asymmetrically via the ground line through the parallel lines to the commutation capacitances C_K. Transition to soft turn-on induced by an increase in L_K (ZCS, chapter 9.8) reduces the di/dt, thus minimising symmetrical current interference. At the same time, the increased inductances L_K are effective in the asymmetrical interference current circuit. At the beginning of the commutation process, dv/dt is determined by the switching characteristics of S1. The voltage leap at the end of

the commutation process is determined by the reverse recovery current behaviour of switch S2. Transition to soft switching in ZCS mode reduces symmetrical current interference and changes the frequency range of asymmetrical currents, without reducing them considerably; also see chapter 9.8.

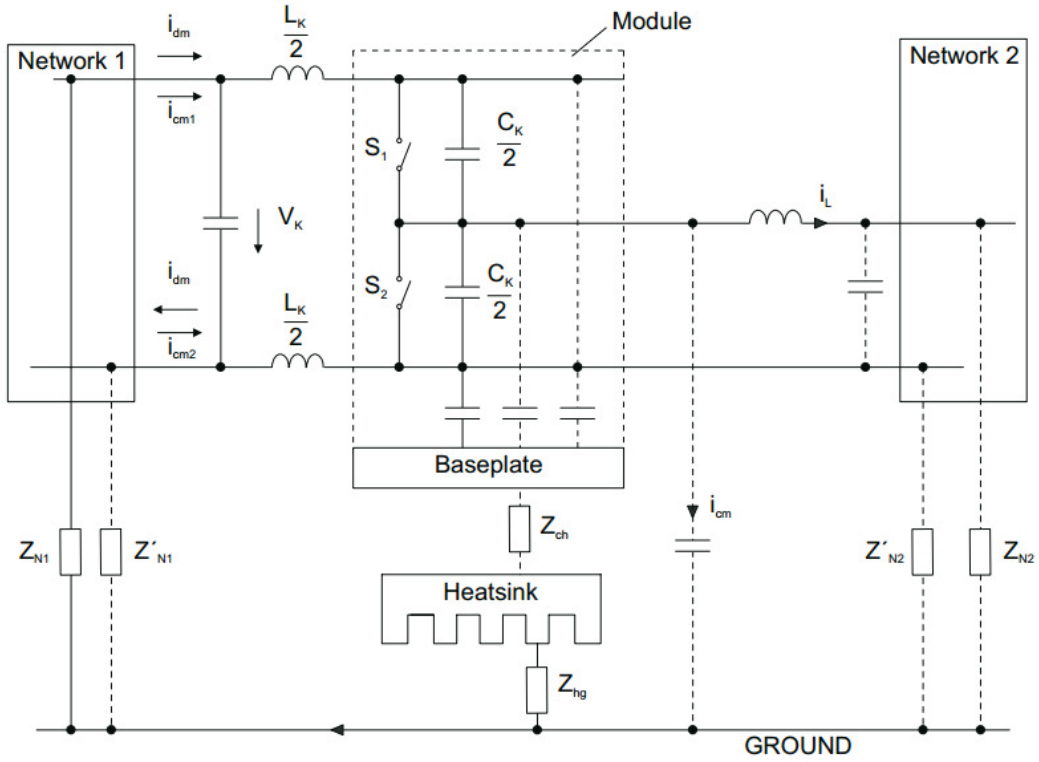


Figure 9.2.3 Equivalent commutation circuit with noise propagation paths [9.4]

Capacitive commutation begins when switch S1 is actively switched off.
In hard switching processes ($C_K = C_{K(min)}$), the asymmetrical interference current is determined by the impedances towards the neutral potential which are effective parallel to the commutation capacitances, and by the semiconductor characteristics of switch S1. The current commutation which is triggered after voltage commutation, and, consequently, the symmetrical interference current is determined by the turn-off behaviour of S1 and the turn-on behaviour of S2.

An increase in C_K calls for the use of a zero-voltage switch with soft turn-off behaviour (chapter 9.8). The turn-off process starts with the first stage of current commutation at a di/dt determined by switch S1 at a reduced voltage. The delayed dv/dt will reduce the asymmetrical currents during voltage commutation. Passive turn-on of S2 determines the di/dt during the second stage of current commutation. Asymmetrical current interference will be reduced by soft switching in ZVS mode without changing symmetrical currents noticeably. Nevertheless, the increased capacitances C_K will diminish the symmetrical interference current in network 1 in relation to the capacitive current divider. Soft switching converter circuits (resonant, quasi-resonant) with turn-on or turn-off phase-shift control will reduce asymmetrical and symmetrical interference currents when using zero-voltage switches or zero-current switches. In converter circuits with auxiliary commutation arms, where ZVS and ZCS are switched alternately, interference currents will not be reduced considerably in comparison to hard switching circuits, since both high di/dt and dv/dt are involved in the total system within one switching cycle; see chapter 9.8.

9.2.3.3 Other causes of electromagnetic interference (EMI)

The cyclic operating mode of power semiconductors with steep switching edges, as well as the current and voltage frequency shares involved here are discussed as one of the main causes of electromagnetic interference in chapter 9.2.3.2. This, however, by no means constitutes a detailed description of the EMI behaviour of power electronic systems.
In [9.6], for example, further component-related oscillation effects are identified as reasons for electromagnetic interference beyond the circuit-related effects (parasitic frequencies in the range of 100Hz - 30MHz), which can be summarised as follows:

LC oscillations:

(1) Oscillations that occur when switching individual power semiconductors (IGBT, MOSFET, diode)
   Cause:
   - excitation of resonant circuits consisting of the non-linear intrinsic semiconductor capacitances and the parasitic circuit environment (L, C)

   Interference frequency range: 10 - 100MHz
   Counter-measure:
   - circuit layout optimisation
   - reduction of switching speed
   - limitation by external circuits

(2) Oscillations in paralleled or series-connected IGBT / MOSFET or diode chips in modules or press-packs:
   Cause:
   - variations in parameter tolerances among the chips
   - asymmetries in the parallel / series circuit layout (also applicable to series or parallel connection of discrete components and modules)

   Interference frequency range: 10 - 30MHz
   Counter-measure:
   - circuit layout optimisation (balancing)
   - use of suitable gate series resistors
   - chip optimisation
   - reduction of switching speed
   - limitation by external circuits

Oscillations during charge carrier transit time:

(1) PETT oscillations (Plasma Extraction Transit Time)
   Cause:
   - occur in the tail current phase of the turn-off process of bipolar components (IGBT, soft-recovery diode)
   - the space charge zone collides with a pile of (free) charge carriers which form the tail current
   - PETT oscillations occur in the form of radiated electromagnetic interference

   Interference frequency range: 200 - 800MHz
   Counter-measure:
   - avoid LC circuits with resonant frequencies in the PETT oscillation range in
   - the module design

(2) IMPATT oscillations (Impact Ionisation (Avalanche) Transit Time)
   Cause:
   - dynamic process during diode turn-off
   - the electrical field encounters the residual pile of (free) charge carriers
   - the diode changes dynamically to avalanche state (electron impact ionisation)
   - IMPATT oscillations occur in the form high-energy radiated electromagnetic interference

   Interference frequency range: 200 - 900MHz
   Counter-measure:
   - optimisation of chip design

9.2.3.4 Turn-on time diode

In order to reach the "soft" switching characteristics described in chapter 2.3.4.2, the charge carriers must be granted sufficient time to reach the state of quasi-static charge carrier distribution. This is not the case for very short conduction times. Figure 9.2.4 shows switching processes with a very short diode turn-on time with an inductive load. It is taken into account that the actual on-time of the diode is approx. 1µs shorter, as the short pulse suppression of the driver and turn-off delay time $t_{d(off)}$ of the IGBT are deducted from the time duration $t_{off,IGBT}$. Oscillations with high amplitude can be seen in the current (green) with a very short duty cycle. The interference level (pink) is only a relative measure, measured with a conductor loop above the module.

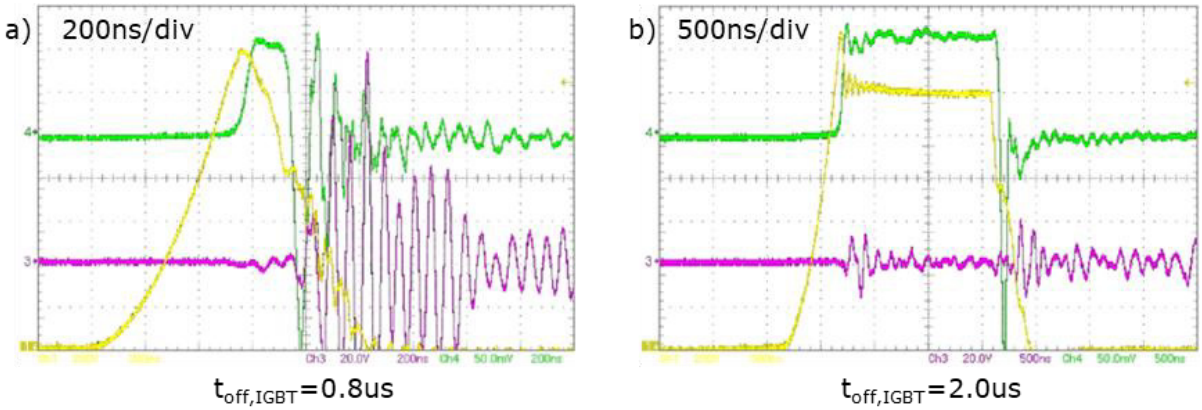


Figure 9.2.4 a) Turn-off at high interference level (pink) at V_{CC}=1200V (V_{AK} -yellow) and I_F=400A (green); b) Turn-off at "normal" interference level (pink)

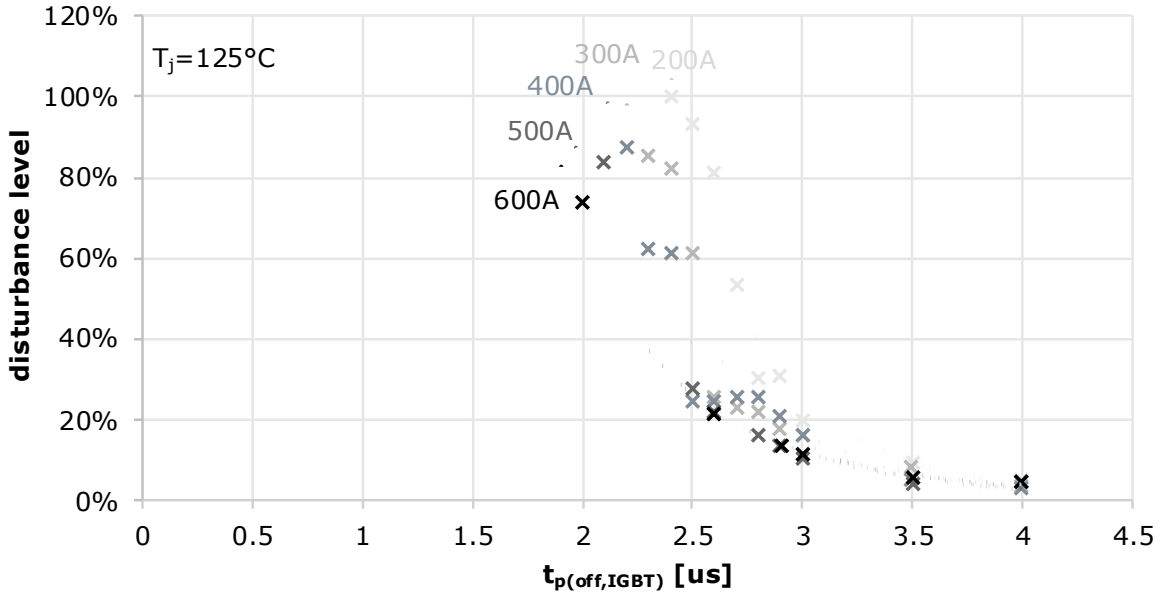


Figure 9.2.5 Relative interference level related to the maximum value at 200A and 125°C for IGBT turn-off signals of different durations as a function of current and temperature

These high-frequency oscillations may influence signals and logic devices and impair safe and reliable operation. For this reason, Semikron Danfoss recommend suppressing switching signals for less than 3µs for 1200V IGBT and < 5 µs for 1700V.

9.2.3.5 Low-inductance structure of the commutation circuit

A low-inductance design of the commutation circuit aims to reduce the high-frequency oscillations in the switching process. This includes the reduced snappy behaviour of the diode when switching off and the reduced overvoltage at the IGBT/MOSFET.
A low-inductance design is achieved by a large overlap of the potentials involved in the commutation circuit. In a 2-level circuit, these are the DC+ and DC- potentials. In a 3-level circuit, these are DC+ and N as well as N and DC-, as these potentials are involved in the commutation circuit.
Further measures to minimize the oscillation behaviour are the snubber capacitors described in chapter 9.6. For measures at system level, please refer to [9.7] and [9.8], among others.

9.3 Parallel connection

9.3.1 Objectives and areas of application

The chapters below are designated for IGBT with freewheeling diode. They may also, however, be applied to MOSFET, provided the connection/terminal designations are modified accordingly. Parallel connections are always needed when the performance of an individual component is insufficient. Paralleling begins at the microscopic level with some hundred thousand of individual IGBT cells, continues on the module level in the parallel chip connections and on the circuit level in the parallel connection of modules and entire inverter units. (Figure 9.3.1).

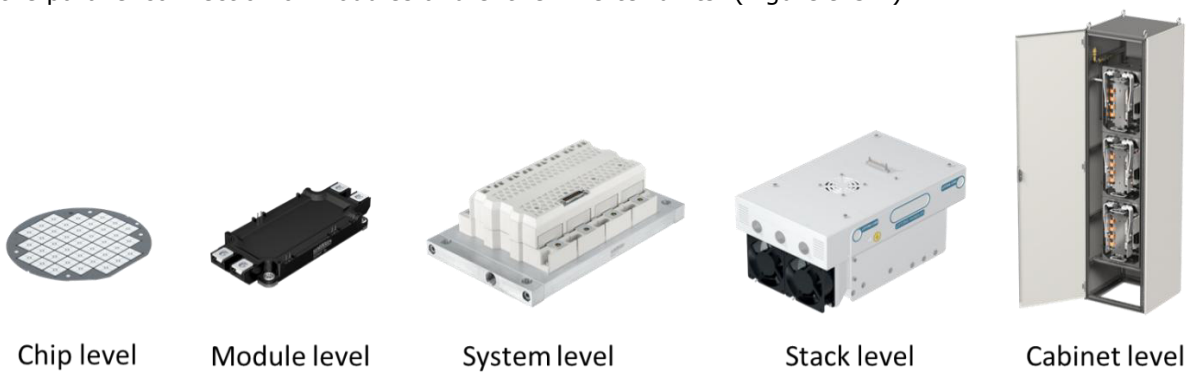


Figure 9.3.1 Levels of parallel connection

Parallel connection of components is a common concept to realize required output currents with components of lower rated current classes compared to a single high current component. The parallel connection pursues the goal of symmetrical current distribution between the parallel-connected paths in the conducting (static) as well as switching on and off (dynamic) state. Compared to a single switch, the parallel connection of several components achieves a better heat spread at the expense of the installation volume. From an economic point of view, the use of a higher number of smaller modules in the high volume can speak in favour of a parallel connection instead of a single device.

9.3.2 Static, dynamic current symmetry and derating

Maximum utilization of the switch resulting from the parallel connection is only achieved with ideal static and dynamic balancing of the current (see Figure 9.3.2.).

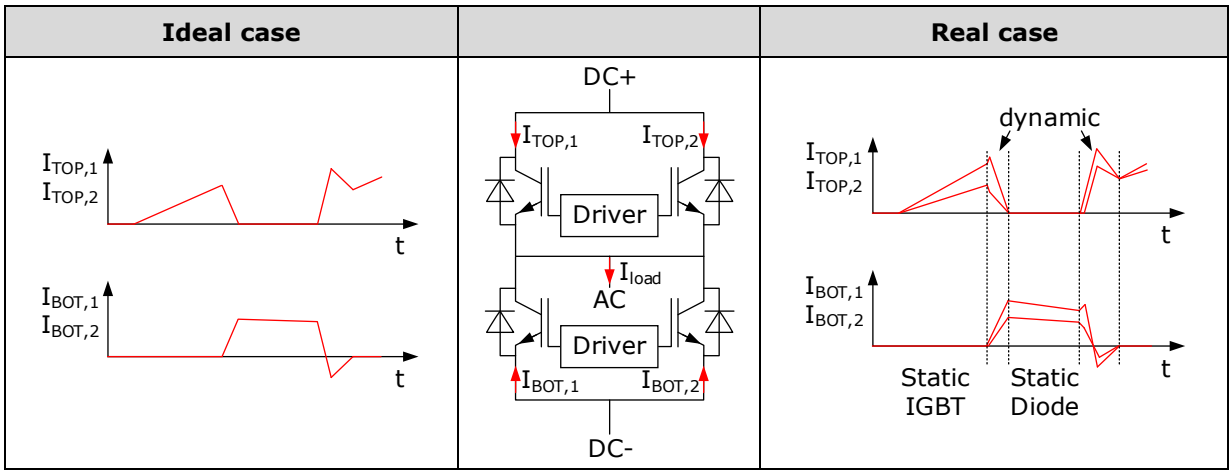


Figure 9.3.2 Exemplary illustration of the ideal and real current flow of two halfbridges connected in parallel

Even with optimum module selection, control and layout design, ideal static and dynamic balancing cannot be achieved. Therefore, a current reduction (derating) must be taken into account with regard to the total rated current load of the switches.
Based on practical experience in a large number of applications and the following influences of static and dynamic semiconductor parameters, a derating of at least 10% is recommended. A semiconductor that can carry 100A as a single component should therefore only be designed for a

current of 90A in the parallel circuit. In asymmetrical setups, the deviations in the currents of the parallel components can be considerably higher. Balancing inductances may be necessary.
Limiting the divergence of the currents is in the interest of the user in order to keep derating as low as possible. Furthermore, the SOA must not be violated with regard to the maximum currents that can be switched off and the maximum overvoltage.
The divergence of the currents in the conduction phase leads to different turn-off and turn-on currents for the switches in the parallel branches. This is accompanied by different conduction and switching losses of the IGBT and the diode. The resulting different junction temperatures in turn have an influence on various semiconductor parameters.

9.3.3 Factors influencing the current symmetry

The user can influence the current symmetry between parallel current paths as follows:

- cooling concept
- the semiconductor itself (forward voltage, transfer characteristic, capacitances, switching times and speeds)
- circuit layout
    - the DC connection (impedance, DC link voltage)
    - the AC connection (impedance - cable length and position)
    - the commutation inductance
- the driver/driver concept (signal propagation times, jitter)

From the user's point of view, the question arises as to which influencing factors have the greatest leverage on the current symmetry (leverage = financial/technical expenditure/influence on the current symmetry).
Table 9.3.1 summarizes the main factors influencing the current distribution between parallel current paths.

Category	Influencing factor	Static Sharing	Dynamic Sharing
Cooling	T_j	x	x
Semiconductor	$I_C=f(V_{GE}, T_j)$		
	On state voltage $V_{CE(sat)} = f(i_C, V_{GE}, T_j) \mid V_F = f(i_F, T_j)$	x	
	Transfer characteristic g_{fs}		x
	Switching time $t_{d(on)}, t_{d(off)}, t_r, t_f$		x
	Threshold voltage $V_{GE(th)}$		x
Driver	Jitter		x
	Propagation delay		x
	Output impedance		x
	Gate voltage (Supply)	x	x
	Gate resistors		x
Circuit	Gate loop impedance		x
	Emitter coupling impedance		x
	Commutation loop impedance	x	x

Table 9.3.1 Key factors influencing the current distribution between parallel current paths

9.3.4 Cooling

Semiconductor parameters are temperature-dependent. Cooling therefore has an influence on the static and dynamic current symmetry. This results in the requirement for good thermal coupling between modules connected in parallel. In the case of parallel connection in the module, the coupling takes place via the substrate or the base plate. In the case of modules via the heat sink. Modules should therefore be mounted close together and thermally well coupled (also due to the symmetry of the inverse and freewheeling diodes) on a common heat sink.
For large parallel systems (system level, stack level, cabinet level in Figure 9.3.1) with several heat sinks, thermal series connection (thermal stacking, see chapter 5.4.4) should be avoided as far as possible, this applies in particular to air-cooled systems. A temperature difference of 10°C means up to 20mV difference in the forward voltage of the same diodes. The hotter diode draws even more current and exacerbates the temperature difference.

9.3.5 Semiconductor

9.3.5.1 Forward voltage

In the switched-on, stationary forward state, the same forward voltage is set across the parallel-connected components. The current distribution depends on the tolerances in the output characteristics. Figure 9.3.3 shows the distribution of the total load current to two parallel-connected IGBT with different output characteristics.

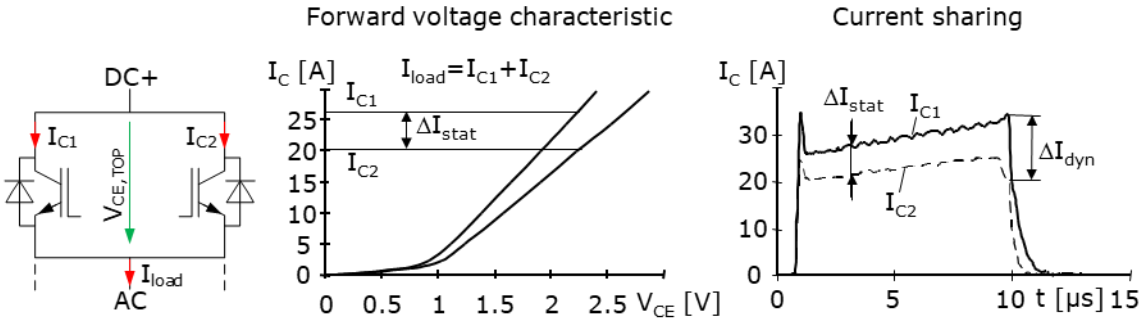


Figure 9.3.3 Distribution of the load current I_{load} to two parallel-connected IGBT with different output characteristics

The transistor with the lower forward voltage initially carries the greater part of the total current and is therefore subjected to higher conduction losses, causing the junction temperature to rise more quickly. At this point, the temperature coefficient (TC) of the saturation voltage plays a decisive role. If the TC is positive, i.e. the saturation voltage increases with rising temperature, the current distribution shifts towards the transistor with the initially lower current component. The result is an equilibrium (ideal case) of the current distribution between the parallel-connected transistors. Power semiconductors with positive TCs of the forward voltage are therefore very well suited for parallel connection. With a few exceptions, all current IGBT technologies have a positive TC above approx. 10...15% of the rated current range. The same applies to the $R_{DS(on)}$ of MOSFET, which always has a high positive TC.

In contrast, freewheeling diodes have a negative TC over almost the entire range up to the rated current (Figure 9.3.4). A strongly negative temperature coefficient (>2mV/K) leads to the risk of thermal overload when diodes are connected in parallel, as they have a certain spread in their forward voltage due to the manufacturing process. Care must be taken to ensure that the spread in the forward voltage is as small as possible. If there is a wide spread, selection may be necessary. No wiring is required for parallel connection.

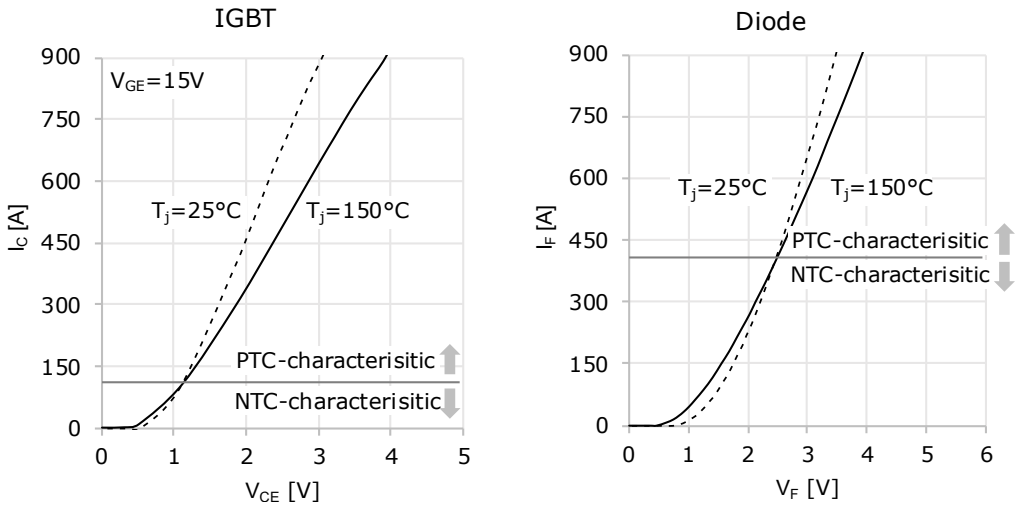


Figure 9.3.4 Temperature dependence of the forward characteristic of the IGBT and inverse freewheeling diode (SEMiX453GB12M7p)

The differences in the forward voltage are counteracted by the switching losses via the technology curve (E_{off} vs. $V_{CE(sat)}$, E_{rec} vs. V_F, see Figure 9.1.3).
The differences in the V_{CE} and V_F voltages are minimized for chips of the same production lot, as these were manufactured under the same conditions.

9.3.5.2 Chip capacitances

The influence of the semiconductor capacitances was investigated in a parallel circuit test. The scattering can be seen in Figure 9.3.5 a) for an arbitrary selection of components. Statistical distributions from production tests do not exist. The maximum deviation is +/- 5%. Differences in the switching behaviour of the parallel components could not be determined. Therefore, in a further test, a capacitance of 4.7nF was connected externally between the gate and emitter of one of the parallel IGBT (=C_{GE} + 20%). Nevertheless, only minimal differences were measured. This leads to the conclusion that differences in the small signal capacitances only have a minor influence on the current symmetry during switching.

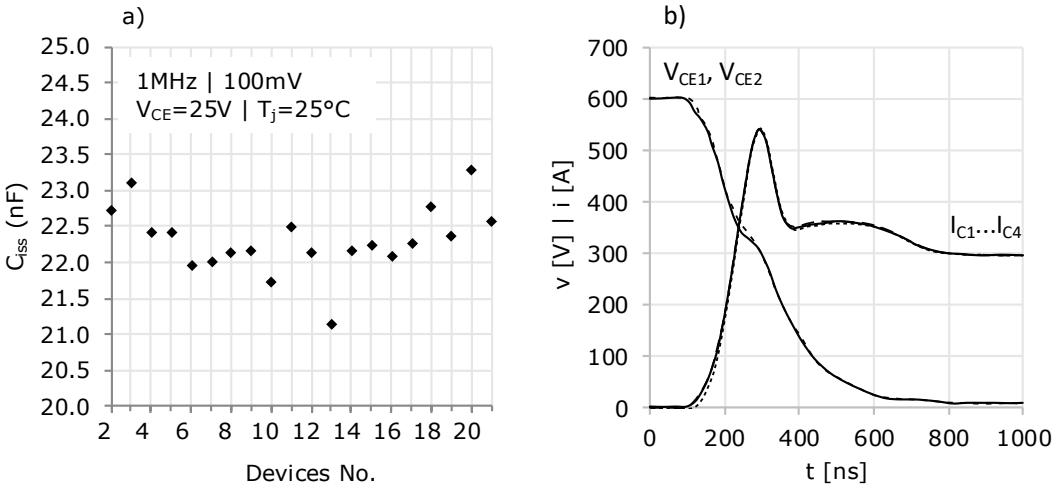


Figure 9.3.5 a) Measured variation of the input capacitance C_{ies} of a selection of 450A IGBT modules; b) Switching test with 4 parallel modules (switching on) with an additional 4.7nF external capacitance between the gate emitter on the module

9.3.5.3 Transfer characteristic $I_C=f(V_{GE}, T_j)$ and threshold voltage $V_{GE(th)}$

The threshold voltage $V_{GE(th)}$ has a negative temperature coefficient TK, while the slope of the characteristic curve g_{fs} has a positive TK. Depending on the operating point, there may therefore be a positive or negative feedback effect with the junction temperature. Figure 9.3.6 shows the transfer characteristic for 450A module. Up to approx. 1.5 times the rated current, the curve has an NTC characteristic (negative feedback). A symmetrical effect (PTC characteristic) therefore only occurs for overloads (e.g. short circuit).
When the diode is commutated to the IGBT, the device with the smaller $V_{GE(th)}$ therefore takes over the output current (switches on earlier) until the parallel one switches on. When switching off, the current of the switch with the higher $V_{GE(th)}$ can already commutate to the one with the lower $V_{GE(th)}$ (switches off later).

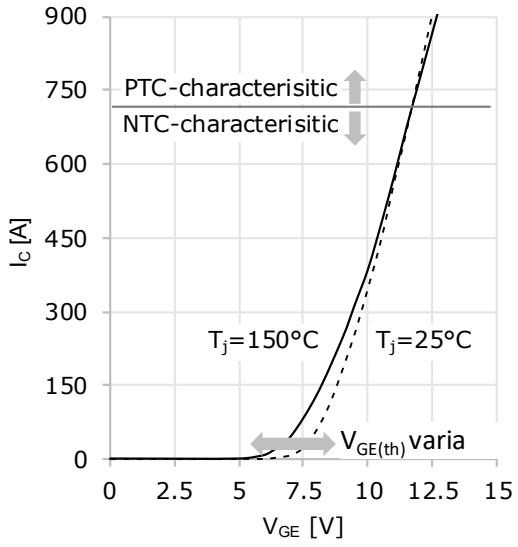


Figure 9.3.6 Transfer characteristic (SEMiX453GB12M7p)

Differences in the transfer characteristic lead to asymmetries in the switching instant and therefore to different switching losses. IGBT of today's generations exhibit only relatively small variations in the transfer characteristic (Figure 9.3.7).
The decisive factor for the current unbalance during switching is the plateau voltage $V_{GE(pl)}$, which occurs during the switching process as a horizontal line of the gate voltage.

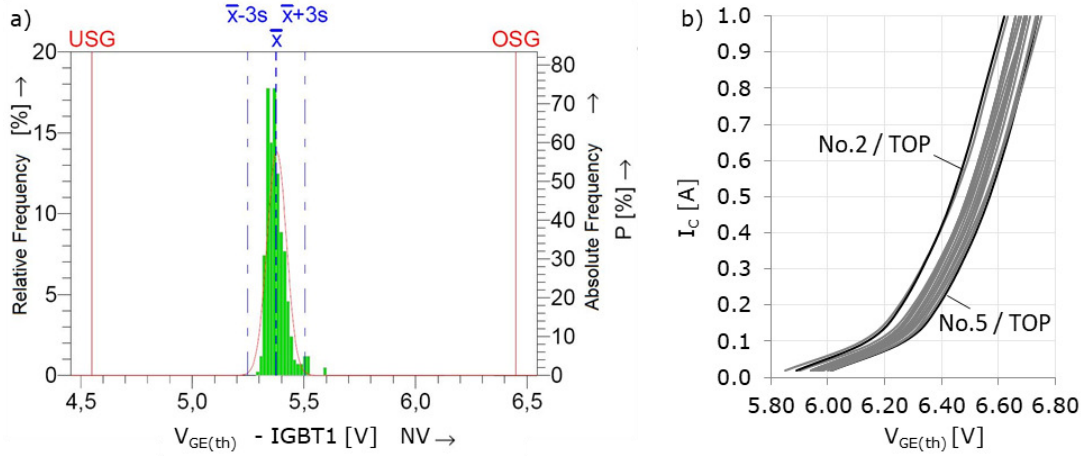


Figure 9.3.7 a) Distribution of the threshold voltage of 800 IGBT chips (@4mA, 25°C) with the specification limits (USG and OSG); b) Measurement of the transfer characteristic of various modules in the threshold voltage range to select extreme pairs for parallel switching tests

The influence of the different transfer characteristics was investigated in a switching test [9.10] with 6 parallel SEMiX modules. For this purpose, the two components with the greatest dispersion of the plateau voltage were placed on the outside of the structure (Figure 9.3.8: Pos. 1 + Pos. 6; $V_{GE(pl)}$ +/- 100mV) and more typical components in the middle (Pos. 2-5). They are controlled by a common driver, shown on the right in the foreground. All IGBT modules are dynamically decoupled by their own gate and auxiliary emitter resistors (Figure 9.3.16). This allows the values for $V_{GE(pl)}$ on the modules to be set relatively independently of each other. For this experiment, the AC connection is symmetrical, centrally between modules 3 and 4 (green arrow) and centred under the structure to the DC circuit. In comparison, the influence of an asymmetrical AC cable connection will be examined in the following section.

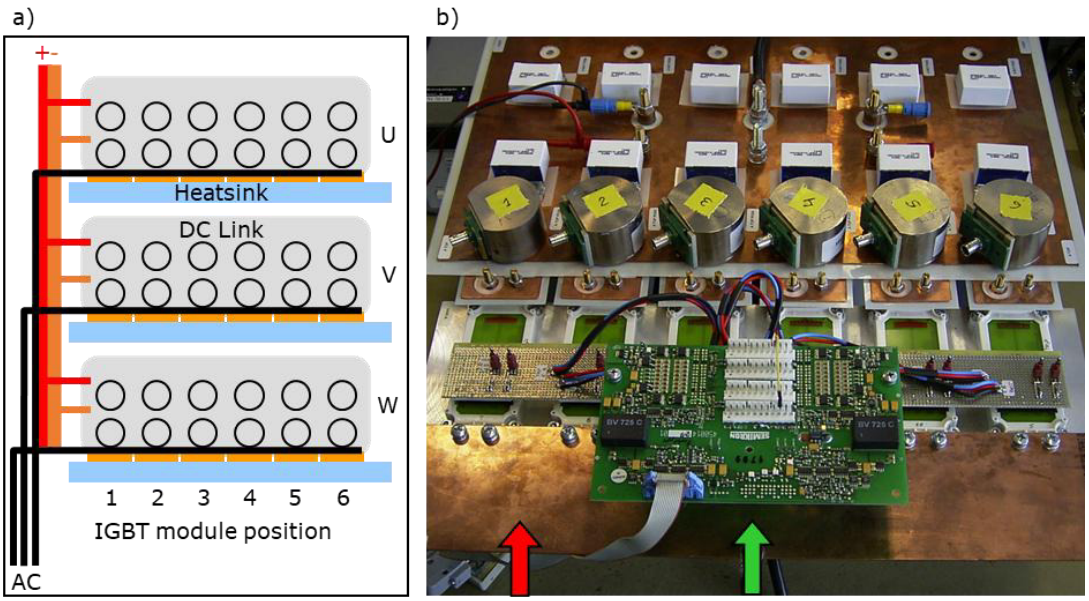


Figure 9.3.8 a) Sketch of an inverter setup with 6 parallel modules per phase and unbalanced AC connection; b) Test setup with 6x 450A SEMiX modules (in the foreground driver unit, in the background DC link with Pearson converters for current measurement and snubber capacitors)

In the switching test, the measured peak currents at turn-on are compared as a measure of the percentage differences in the turn-on losses. Theoretically, the IGBT in the middle position should carry the highest current, as they have the lowest impedance to the AC node (green arrow).

However, the component in position 1 with the lowest plateau voltage has the highest current. The maximum deviation is +10% / -12% of the mean value.
A similar load also occurs when switching off, the component with the lowest plateau voltage switches last and takes over the current from the other components. As a result, the switching losses are also highest for this component.

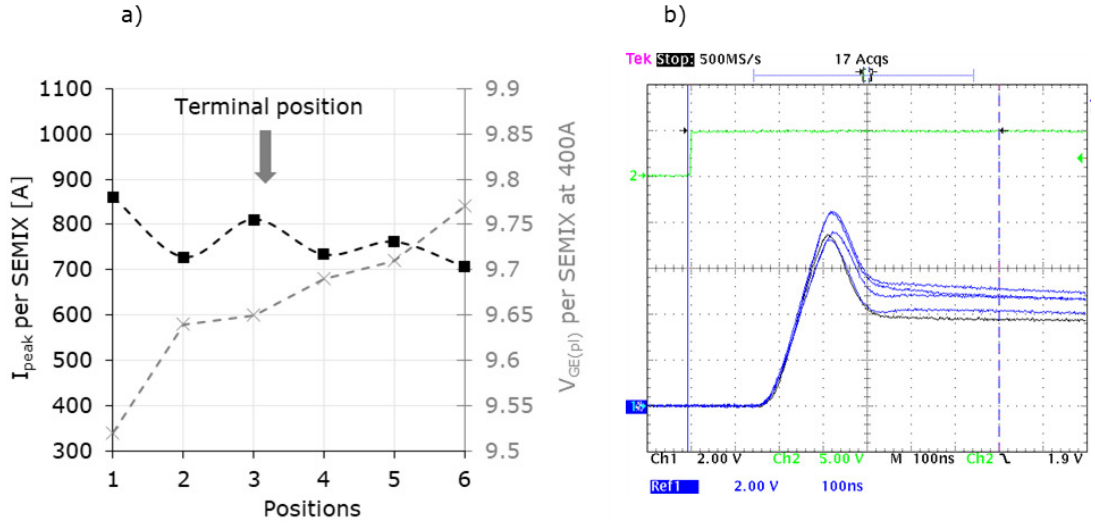


Figure 9.3.9 a) Current peaks with symmetrical AC connection (black, left Y-axis) and plateau voltage of the modules (grey, right Y-axis); b) Measured turn on current peaks in double pulse with inductive load and 400A per module (200A/div)

9.3.6 Circuit layout

9.3.6.1 Balancing the DC link voltages

To avoid differences in the DC voltages of parallel capacitor banks (→ different output voltage despite identical switching times), they should be hard-wired together. Care must be taken to ensure that no oscillations occur between the capacitor banks during switching operation (LC circuit). For large systems (MW), DC fuses are recommended between the capacitor banks in order to limit the energy that flows into the short circuit point in the event of a short circuit. Parallel systems must have the same design and use the same type and capacitance value of capacitors.

9.3.6.2 AC connection

The above-mentioned test to investigate the effects of plateau voltage was modified so that the AC connection was now attached asymmetrically at the side (Figure 9.3.10). The rest of the setup remained the same.

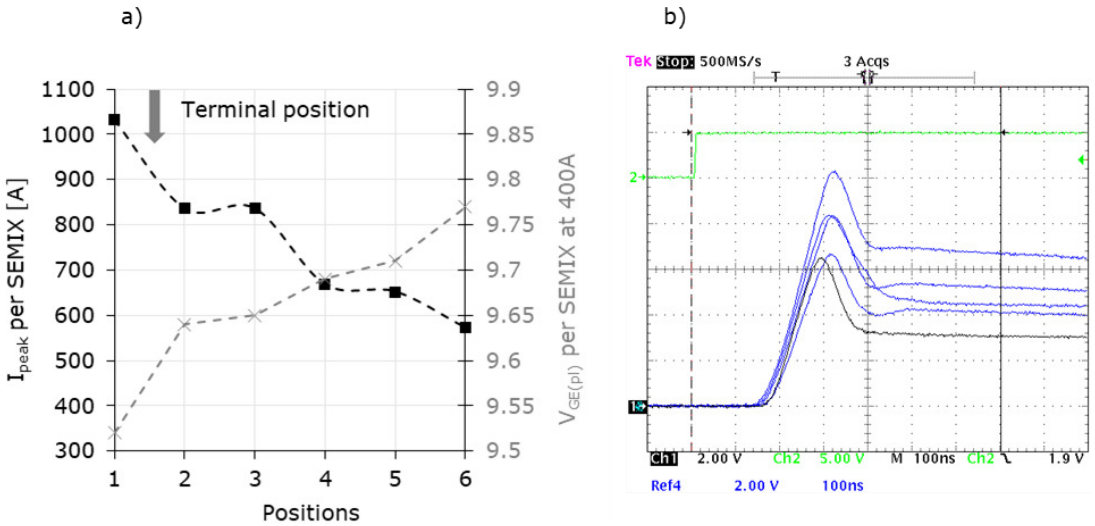


Figure 9.3.10 a) Current peaks with unbalanced AC connection (black, left Y-axis) and plateau voltage of the modules (grey, right Y-axis); b) Measured turn on current peaks in double pulse with inductive load and 400A per module (200A/div)

The differences in the turn on current peaks increase sharply. The deviation from the mean value is +34% / -24%. It is thus 3 times as high as is justified by the different transfer characteristics. The influence of the connection position dominates. The problem for the user is that a cable connected in the middle but routed to the side in front of the modules has the same effect as a cable connected to the side. A central routing of the cables is often opposed by maintenance and service considerations. Differences in the branch impedance also lead quasi-statically to different output currents of the inverter branches.

9.3.6.3 Impedance of the driver circuit

Existing deviations lead to different switching times and thus contribute to an uneven distribution of switching losses. Together with the transistor input capacitances, the loop inductance of the control circuit can generate oscillations that can also propagate between transistors connected in parallel. Voltages are induced across the inductance of the drive circuit L_{E1} through which the main current flows during switching (rapid changes in the emitter current ~ I_C). These can counteract the gate charging or discharging (emitter negative feedback) or amplify it (positive feedback). This is one of the most critical factors influencing the dynamic current distribution. Even 1nH causes a voltage difference of 1V at 1kA/µs.
In modules with an auxiliary emitter, L_{E1} is located inside the housing and cannot be influenced by the user. There is extensive decoupling of the main and control circuits. For IGBT with lower rated currents without an additional auxiliary emitter, the user can improve the symmetry during switching by equalizing the switching speeds by means of symmetrical negative feedback in the emitter current path. When dimensioning, however, it must be taken into account that the switching losses increase due to the resulting slowdown of the switching process. Figure 9.3.11 shows the voltage ratios for different track arrangements during turn-on.

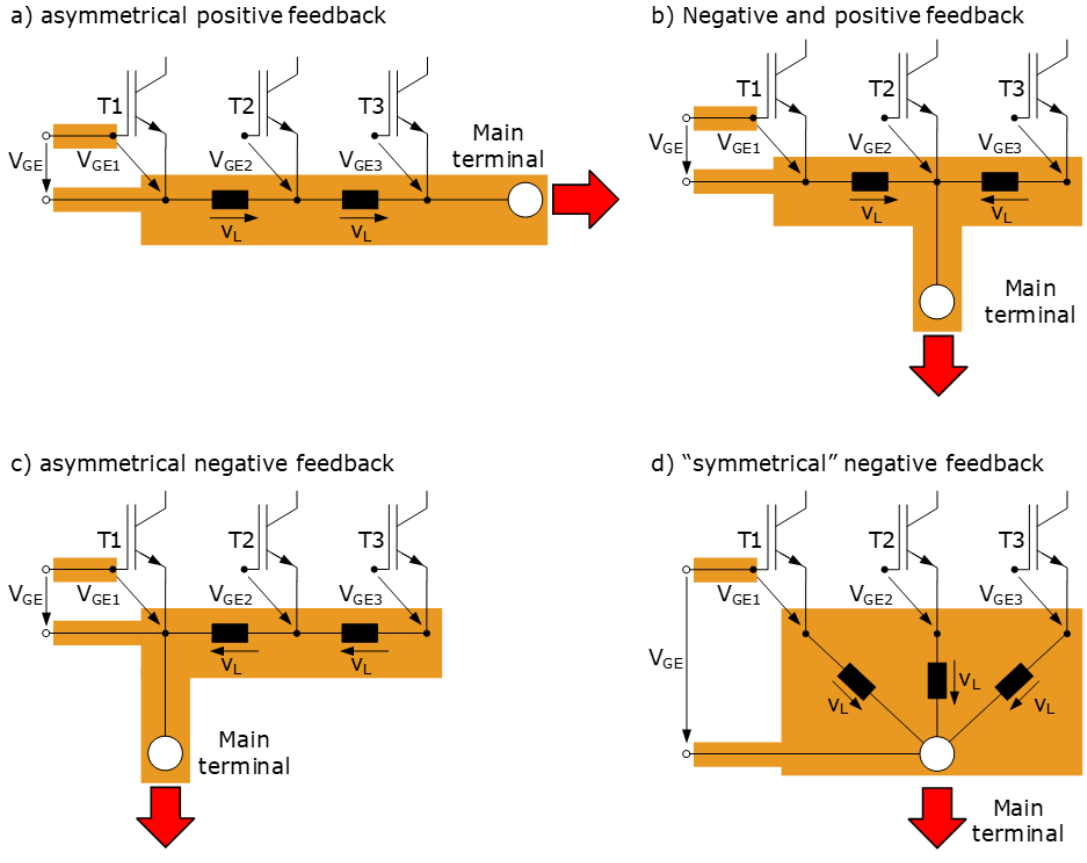


Figure 9.3.11 Examples of positive and negative main current feedback in the driver circuit

Example a) shows different degrees of positive feedback, causing transistor T3 to turn on more quickly than T1:

$$v_{GE3} = v_{GE} + 2v_L > v_{GE1} = v_{GE}$$

In example b) T2 has positive feedback and T3 negative feedback:

$$v_{GE2} = v_{GE} + v_L > v_{GE1} = v_{GE} > v_{GE3} = v_{GE} - v_L$$

In example c) different degrees of negative feedback occur, causing transistor T3 to turn on more slowly than T1:

$$v_{GE3} = v_{GE} + 2v_L < v_{GE1} = v_{GE}$$

In example d), all transistors have approximately equal negative feedback, which means that they will switch synchronously as far as possible:

$$v_{GE1} = v_{GE2} + v_{GE3} = v_{GE} - v_L$$

9.3.6.4 Commutation circuit inductance

As explained in chapter 1 commutation circuit inductance L_s affects the semiconductor turn-on losses (turn-on loss reduction) and turn-off losses (generating switching overvoltage). The commutation circuit basically includes the inductances between the semiconductors and the DC link capacitors. If commutation circuits are subject to different loop inductances, the switching speeds of fast power semiconductors may be different, resulting in dynamic asymmetry which has more impact than variations in semiconductor parameters. Even slight differences in this inductance might lead to asymmetrical distribution of switching losses and oscillations between the semiconductors. For this reason, the commutation circuit layout must be as symmetric as possible (current paths must identical in length and enclose the same areas). Different switching speeds cause loop currents in the conductor loops from the short circuited auxiliary emitter and main emitter. They result in a rapid change in the emitter potential of individual switches and might, under certain circumstances, overload the thin auxiliary emitter terminal.

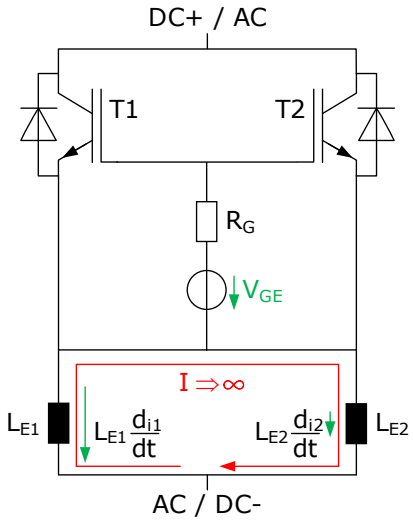


Figure 9.3.12 Different di/dt caused by different commutation inductances, resulting in a high induced loop current

All power and driver circuits within the parallel circuit have to be laid out with minimum parasitic loop inductance and strictly symmetrical wiring. The need for symmetry applies not only to the length of the connection to the common AC terminal (branch impedance) but also to the current path from the semiconductor to the DC link capacitors (commutation inductance). Small capacitors with identical number per module and the same clearances between module and capacitor connections are needed for this. The emitter inductances are to be kept small, since they ensure rapid potential change in the driver voltages during switching.

9.3.7 Driver concepts

Two driver concepts can be considered for controlling the parallel units:

- Central driver
- Individual drivers

In the *individual driver* concept, each paralleled IGBT module has its own gate driver. Each of the drivers has its own primary and secondary side with its associated output stage. Every one of the output stages controls one of the parallel modules. The four individual drivers are connected e.g., on the primary side via an adapter board, which interfaces the signals from the control unit to the individual drivers.

In the *central driver* concept, the output stage of the single gate driver is connected with an adapter board serving as an interface to the parallel modules. On this board are located the gate and emitter resistors as well as the gate protection circuits. Each module switch has its own gate circuit, which is controlled by the secondary stage of the central gate driver.
Figure 9.3.13 shows an example of 4 modules connected in parallel. The coloured markings of the module positions serve as an orientation aid. They correspond to the colours of the traces in the following diagrams.

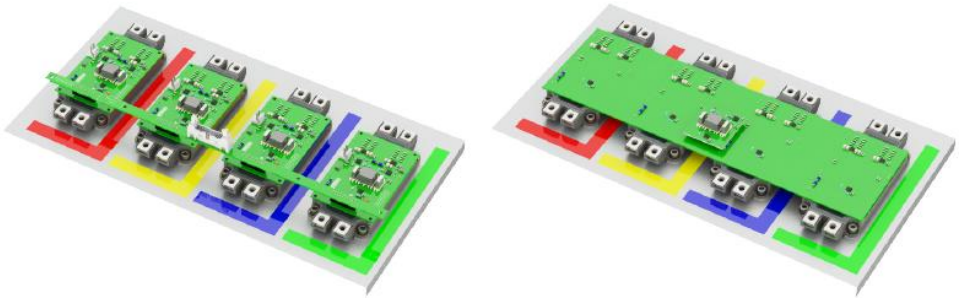


Figure 9.3.13 Modules with individual drivers (left) and central driver (right) [9.11]

Just like the impedances of a system, the characteristics of the drivers also influence the current distribution. In contrast to the mechanical design, which mainly affects the static current distribution, the driver characteristics predominantly affect the dynamic current sharing. The reasons for this are, on the one hand, the differences in the signal propagation times and the gate-emitter voltages, as well as the influence of the jitter. On the other hand, the common emitter path, of the central driver unit, affects the current sharing.

9.3.7.1 Central driver concept

Individual gate resistors R_{Gon}/R_{Goff}
In the case of direct parallel connection of the IGBT gates from a central driver, the IGBT (T1) with the steeper transfer characteristic clamps the gate voltage of the parallel IGBT (T2) on the level of its plateau voltage $V_{GE(pl)1}$ (see Figure 9.3.14 a)). IGBT T1 takes up more current as long as it clamps the gate voltage during the interval Δt1. When the inverse diodes take full blocking voltage the gate voltage increases again and both IGBT could turn on fully.
In order to avoid this, a separate gate resistor R_{G1}/R_{G2} is provided for each IGBT (Figure 9.3.14 b). The gate voltage on the IGBT can then rise independently of one another, which results in only slight switching differences. IGBT modules - particularly for higher currents - already have integrated gate resistors. Nevertheless, an external gate resistor is still required.

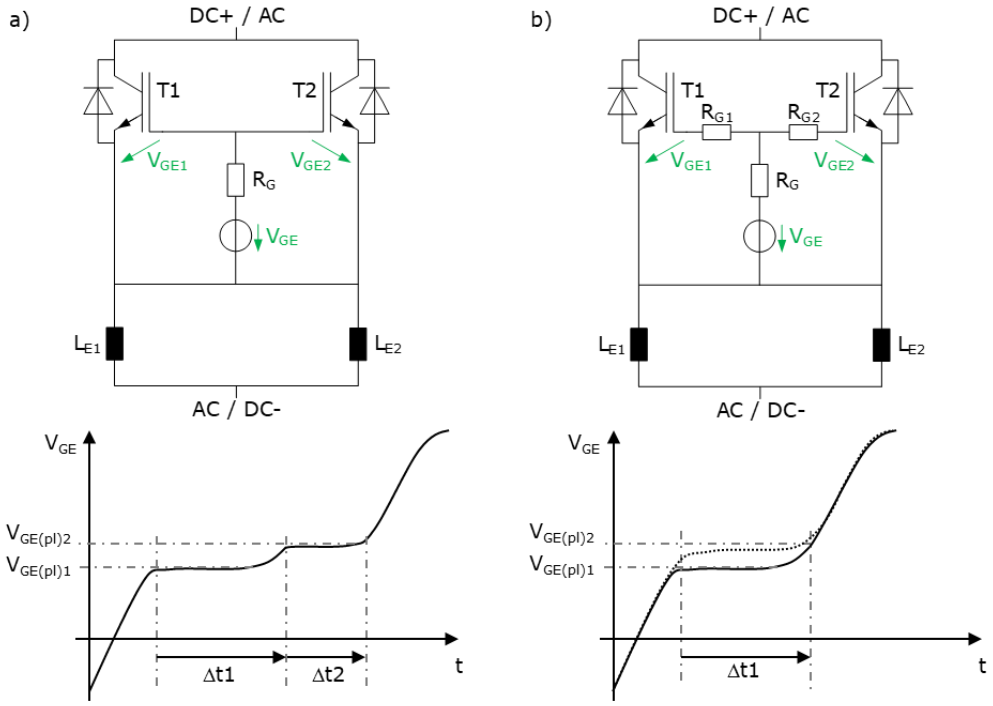
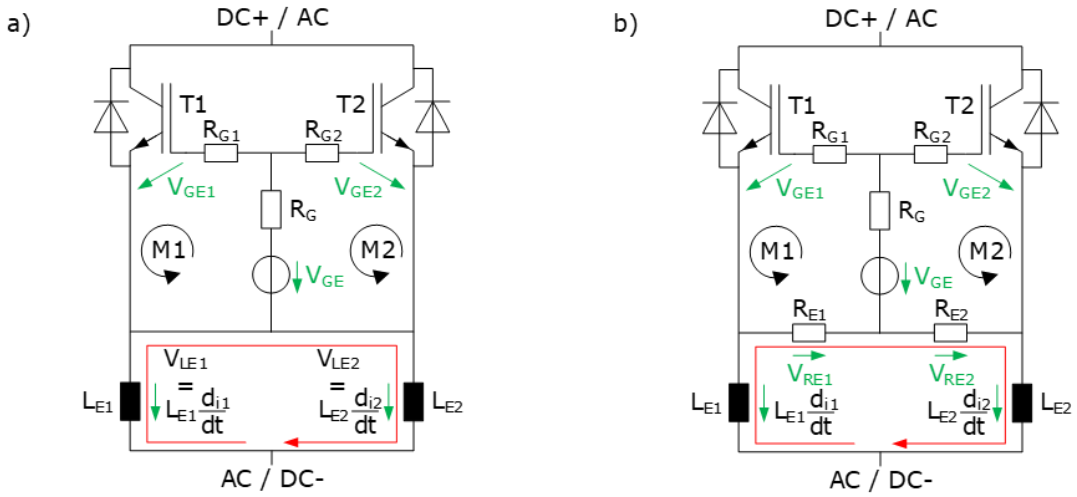


Figure 9.3.14 a) Gate voltage curve with hard-clamped gates; b) Gate voltage curve with individual gate resistors

Emitter resistor R_E

Figure 9.3.15 shows on the left side a hard emitter connection of the driver to the IGBT and the stray inductances in the emitter connection. For the TOP IGBT, the stray inductance results from the AC connection of the modules. For the BOT IGBT this is the inductance in the DC minus connection. Different switching speeds (di/dt) of the IGBT or different emitter inductances L_E result in different voltage drops V_{LE1} and V_{LE2}. These different voltage drops cause a circulating current flowing through the emitter connection of the driver. This circulating current can reach high values and overload the thin auxiliary emitter terminals. To avoid this, current-limiting resistors are inserted into the emitter connections of the driver (Figure 9.3.15 b)). With balanced emitter inductances good results have been achieved with emitter resistors R_E of about 0.5Ω. Note that each resistor R_E is in series with the gate resistance R_G and therefore has an influence on the switching behaviour of the IGBT.



M1: $V_{GE1} = V_{GE} - V_{RG} - V_{RG1}$
M2: $V_{GE2} = V_{GE} - V_{RG} - V_{RG2}$

M1: $V_{GE1} = V_{GE} - V_{RG} - V_{RG1} - V_{RE1}$
M2: $V_{GE2} = V_{GE} - V_{RG} - V_{RG2} + V_{RE2}$
$\rightarrow V_{GE1} < V_{GE2}$

Figure 9.3.15 Balancing effect of the R_E: voltage drop across the emitter inductance L_E caused by loop current

The voltage drop across the resistors R_{E1} and R_{E2} counteracts differently steep current slopes. A higher induced voltage across the emitter inductance L_{E1} of the fastest IGBT T1 ensures a loop current across the auxiliary and main emitter connection. The voltage drop V_{RE1} reduces the gate voltage V_{GE1} on the fastest IGBT when it is switched on (formula M1). The gate voltage V_{GE2} is increased at the slower IGBT T2. As a result, the switching speeds of both IGBT are equalized. This measure only balances the edges but not the divergence of the currents during the plateau phase.

However, this balancing due to the emitter coupling has limitations:

- When the emitter inductance is large, the coupling becomes too strong. Even slight differences in the switching speed of the parallel IGBT result in high gate voltage differences, which can lead to oscillations.
- For unbalanced emitter inductances (for example, $L_{E1} >> L_{E2}$), and even if the IGBT have the same switching characteristics, different couplings to the gate voltages occur, resulting in different switching.

For this reason, in the design low and symmetrical emitter inductances are a must. This is more critical with the TOP switch than with the BOT switch because the AC connection usually has a higher inductance than the minus of the DC link.

This also shows the limits for a central driver. For systems with higher power, many modules must be connected in parallel so that the emitter connections become longer and thus the emitter inductance is large and unbalanced. As described, this leads to uneven current distribution and oscillations. This is why individual drivers are used for large systems.

Other additional gate driver components

To optimise the switching behaviour of parallel-connected IGBT modules, the use of additional components can be useful, as shown e.g., in Figure 9.3.16.

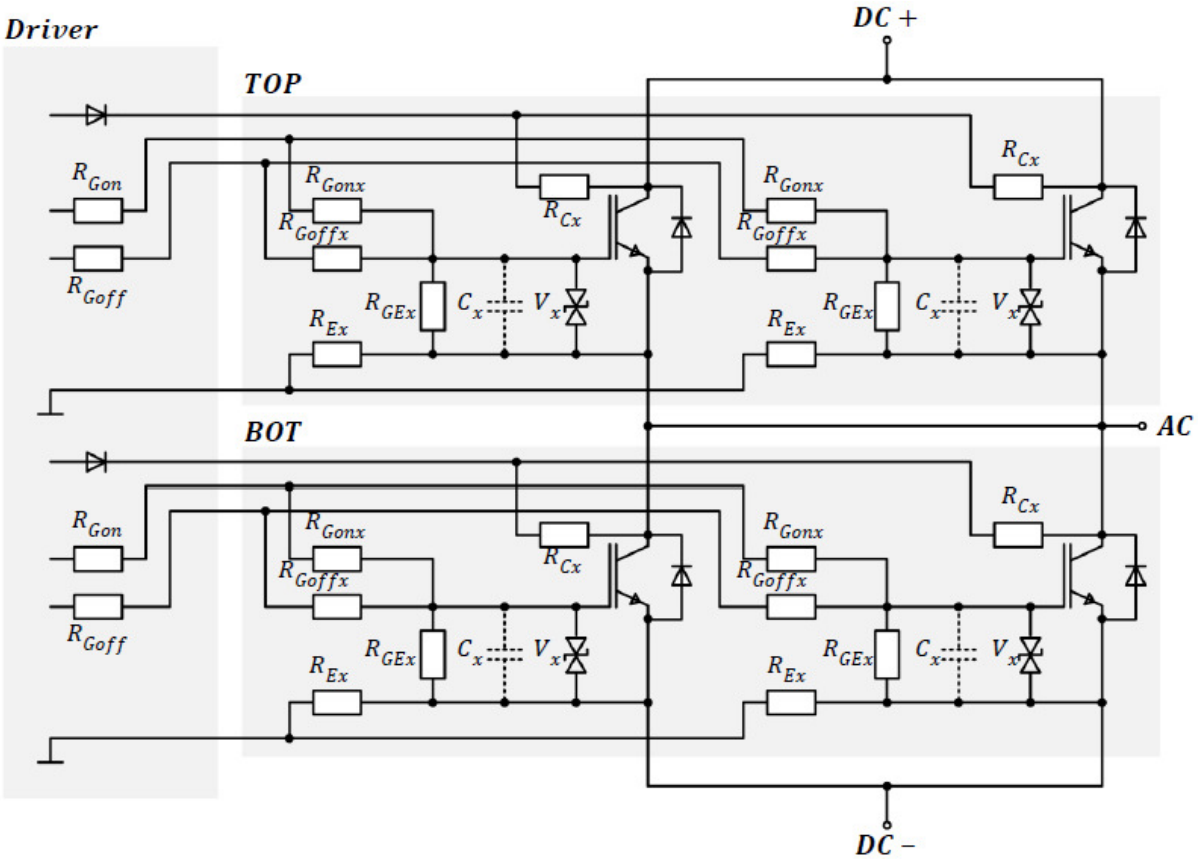


Figure 9.3.16 Block diagram of two parallel-connected modules with interface board and central driver [9.11]

In addition to the gate (R_{Gx}) and emitter (R_{Ex}) resistors, a resistor (R_{GEx}) should be connected gate to emitter. This is to prevent the IGBT from inadvertently turning on when the driver is not supplied. The resistance usually has a value of 10kOhm.
To protect the gate from overvoltage, Zener or suppressor diodes (V_x) are connected from gate to emitter. Make sure that the threshold of the diode is above the maximum gate voltage of the driver but below the maximum allowed gate voltage of the IGBT (±20V).
Possibly a capacitor (C_x) parallel to gate and emitter may have a positive effect on the parallel operation. The capacitor is in the range 10% ... 50% of the IGBT gate-emitter capacitance.
If overcurrent and short circuit protection is implemented on the basis of DESAT monitoring (DCSP), a resistor (R_{Cx}) is used to determine the actual V_{CE}-value. The R_{Cx} resistors are used to average an actual V_{CE} value. They should be dimensioned with approx. 47W. However, measurement at a switch is often sufficient. The resistors and protective circuitry must be close to the module. For this purpose, an interface board should be developed which contains these components. For this interface board, ensure identical cable length to the parallel IGBT. Gate and emitter tracks are to be run in parallel. The driver core can then be plugged directly onto the interface board or connected via cables. The wires should be twisted-pair.
The resistors R_{Gonx} and R_{Goffx} should make up at least 50% of the gate resistance.
The effective total gate resistance of the individual switch is then calculated, e.g. for switching on with:

$$R_G = n \cdot R_{G(on)} + R_{G(on,x)} - R_{G(int)} + R_E$$

n: Number of parallel components
$R_{G(int)}$: IGBT-internal gate resistor

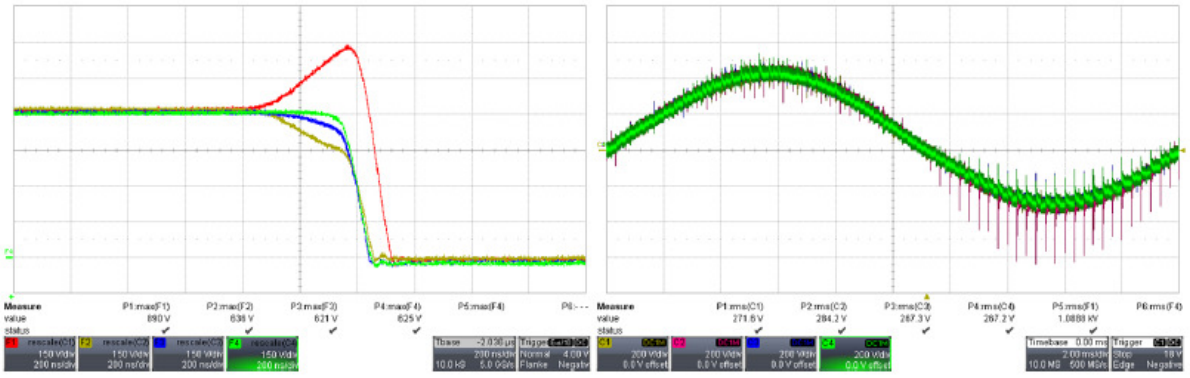
9.3.7.2 Individual driver concept

Minor differences in signal propagation times of individual drivers
The signal propagation time is defined by the time of a valid change of state of the signal at the input of an electronic module, up until a valid change of state of the corresponding output signal. The more devices a signal has to pass, the higher the probability that the differences between the sums of the signal propagation times increase. The likelihood that the output signals of parallel

assemblies will change state at the same time decreases with the number of devices that the signals pass.

$$\Delta t_p = \sum_{i=1}^{n} (t_{p1,i} - t_{p2,i})$$

With regard to the driver concepts, this means that only a small difference between the signal propagation times is much more probable when a central driver is used than in the case of the parallel connection of individual drivers.
The left diagram in Figure 9.3.17 shows the measurement results of IGBT current of the pulse test for four parallel SEMiX603GB12E4p modules. Each of the modules was controlled by a dedicated SKYPER 12 press-fit driver. One of the drivers was prepared in such a way that the associated IGBT (red trace) switches off with a delay time of about 100ns. Due to the longer conduction phase of the IGBT, the currents of the parallel IGBT do not immediately commutate to the corresponding freewheeling diodes, but partly flow through the still conducting IGBT. In this test arrangement, a current increase of approx. 48% occurs, based on the nominal value of a quarter of the sum collector current.
The results for the inverter operation can be found in the right diagram in Figure 9.3.17, in which one of the BOT IGBT (red trace) is switched on approximately 100ns earlier.
The real time offset between parallel SKYPER 12 press-fit drivers, which occurs due to the signal propagation time tolerances, is significantly less than 100ns. The influence of the switching under realistic delay times can be seen on the positive half-wave of the right diagram.



IGBT turn off; collector current; 150A/div; 200ns/div inverter mode; AC current; 200A/div; 2ms/div

Figure 9.3.17 Measured influence of different signal propagation times [9.11]

Small driver jitter
The influence of the jitter occurs with digital drivers connected in parallel, when they have their own system clock. The maximum time offset due to jitter is determined by the frequency of the system clock. If the input signal changes simultaneously at the parallel driver stages, the change in the corresponding output signal may vary in time by the length of one system clock period $1/f_{clock}$.

$$t_{jitter\ (max)} = \frac{1}{f_{clock}}$$

The time offset variance due to jitter approximately shows a Gaussian normal distribution over the values. It is therefore not foreseeable which $0 \leq t_{jitter} \leq T_{clock}$ driver provides a valid output signal at which time.
Looking at the effect of the jitter in isolation, it can be assumed that with an increasing number of signal changes at the input of the parallel drivers, the summed time offset variance between the output signals approaches zero.

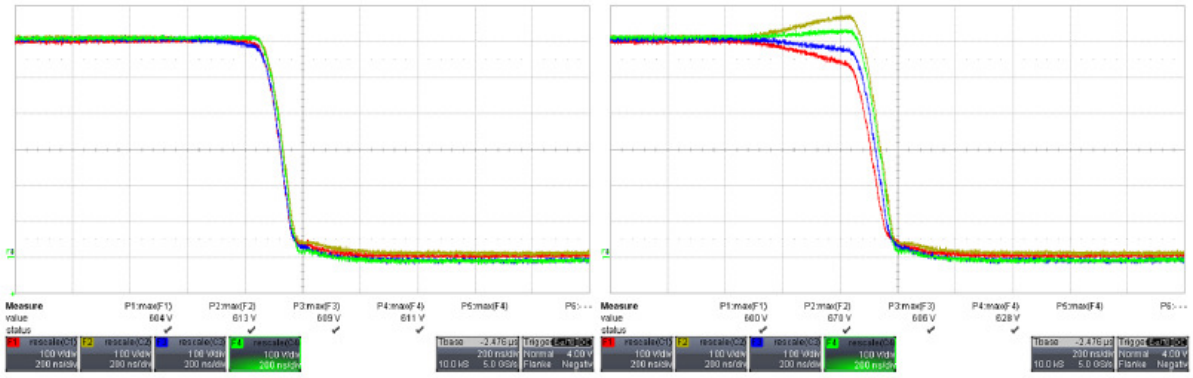
$$\sum_{i=1}^{n} t_{jitter,i} - \sum_{k=1}^{n} t_{jitter,k} \approx 0 \qquad \text{for } n \to \infty$$

In the real application, the time offset of the jitter is added to the time offset of the different signal propagation times. The effect of the jitter can, however, be neglected for the central driver concept.

$$t_d = \Delta t_p + t_{jitter}$$

Figure 9.3.18 shows the measured results of the pulse test with four parallel individual drivers. The delay time due to the jitter is approximately 25ns, which corresponds to the reciprocal of the system frequency of the SKYPER 12 press-fit driver of 40MHz.

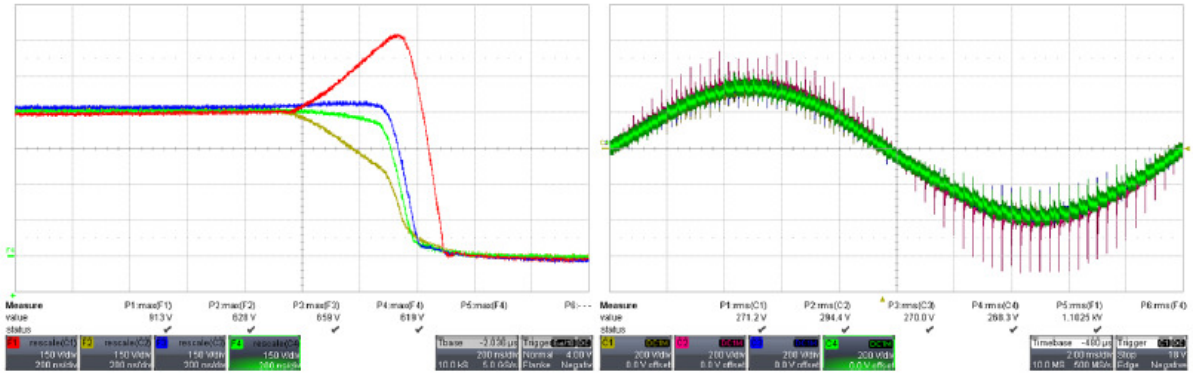
The left diagram shows a nearly symmetrical current distribution. The delay between the driver outputs is almost zero at this time.
The right diagram shows the effect on the dynamic current distribution with a time delay of approx. 25ns between the outputs of the parallel drivers. In this measurement, a time delay of approx. 25ns results in a current increase of approx. 12% (yellow trace), based on the nominal value of a quarter of the sum collector current.



IGBT turn off; collector current; 100A/div; 200ns/div IGBT turn off; collector current; 100A/div; 200ns/div

Figure 9.3.18 Measured influence of the jitter [9.11]

Low differences in gate-emitter voltages
It can be assumed approximately that the switching speed of an IGBT depends on the speed of the charging and discharging of its input capacitance. On the presumption that the parallel-connected semiconductors have identical characteristics and the gate circuits are identical, the gate-emitter voltage determined by the driver sets the speed of the charging process.
If each semiconductor module has an individual driver with its own gate voltage regulation, differences in the gate-emitter voltages between the modules may occur. This can be neglected for the central driver concept.
To illustrate this effect, the gate turn-on and gate turn-off voltage of a driver (red trace) was increased by approximately 0.7V. As a result, the corresponding IGBT turns on faster and turns off slower (Figure 9.3.19).
The left diagram in Figure 9.3.19 shows the dynamic current distribution during a turn-off process. Due to the longer conduction phase of the IGBT, the currents of the parallel IGBT do not immediately commutate to the corresponding freewheeling diodes, but partly flow through the still conducting IGBT. During this particular switching process, there is a current increase of approx. 52%, based on the nominal value of a quarter of the sum collector current.
The right diagram shows the measured results for the inverter test. Here too, the time-delayed switching can be seen clearly displayed by the current peaks of the red trace. This affects the total output current distribution with a deviation of approx. 7% from the nominal value $I_{AC}/4$.



IGBT turn off; collector current; 150A/div; 200ns/div inverter mode; AC current; 200A/div; 2ms/div

Figure 9.3.19 Measured influence of different gate-emitter voltages [9.11]

9.3.8 Conclusions for paralleling IGBT modules

In order to minimise the influence of the semiconductor properties on the current distribution, modules from one batch should be used. In general, a current unbalance of 5% is to be expected.

This current asymmetry must be taken into account when calculating the conduction and the switching losses.
When selecting the driver concept, the size of the system is crucial. For compact systems, a solution with a central driver is preferable. The negative influences on the current distribution caused by the jitter, the differences in the signal propagation times, as well as the differences in the gate-emitter voltages are largely done away with in this concept. In addition, there is the positive effect of emitter feedback.
In the case of larger systems, the shared emitter path increases by design, and oscillations between the parallel semiconductors or modules can occur due to the emitter feedback. In this case, the concept with individual drivers must be used.
If individual drivers are used, care must be taken that the differences between the signal propagation times of the drivers and the time differences due to the jitter are as low as possible. The time lag between the drive signals of the IGBT and the differences in the switching speeds of the IGBT themselves are critical when dimensioning the AC inductances. With low jitter and low differences in the signal propagation times, an additional AC inductor is generally not required and the modules can be connected hard parallel.
If the current asymmetry of a hard parallel circuit is higher than the desired value, the parallel current branches must be decoupled via as large inductances as possible. Particularly separate motor or line filter windings are suitable for this because, in the case of high power, they are frequently already composed of parallel-connected winding systems. In inverter applications, the current distribution is significantly better than in a simple double pulse test due to the positive IGBT temperature coefficient and the high load inductance.

9.4 Series connection

9.4.1 Objectives and areas of application

Power semiconductors connected in series are uncommon without avalanche effect. Owing to

- additional losses caused by the n-fold diffusion voltage (on-state voltage)
- losses in the parallel resistor
- the substantial charge that has to be taken up by the transistor during switching
- the degree of complexity with regard to the components needed for the circuitry

series connections are seldom used for power semiconductors if a component specified for the higher voltage is available. One exception here might be cases where the on-state power losses do not play a major role and one is reliant on the short switching time and low switching losses in semiconductors of the lower voltage class. Far more common are circuits which in themselves work on a voltage level which is not critical for the individual semiconductor. Examples here are multi-level inverters with clamping diodes, flying capacitors or cascaded inverters. Provided clearances, creepage distances and dielectric strength in relation to ground are considered, these can be seen as individual switches with no series connections.

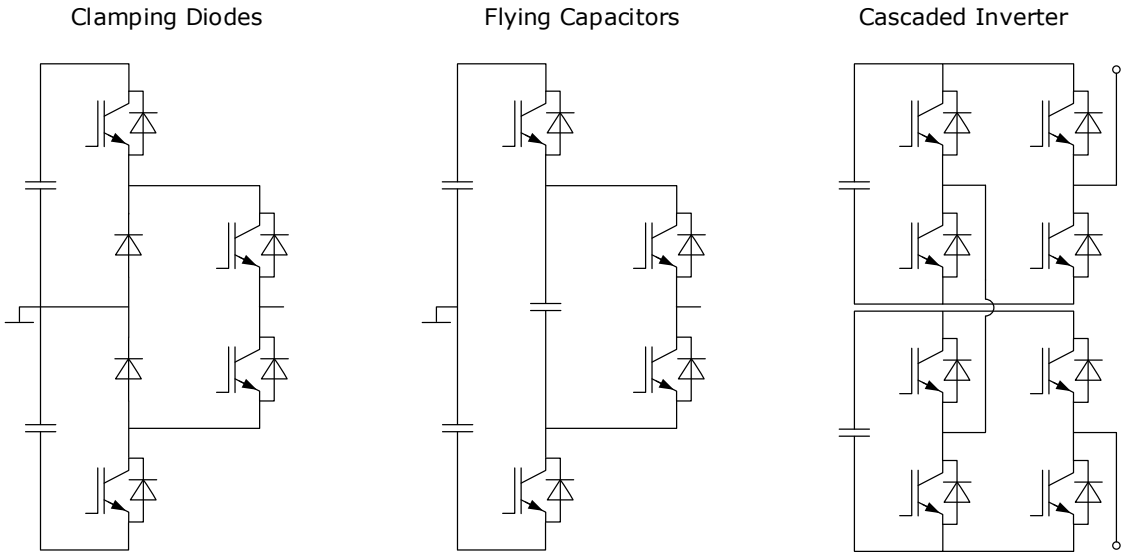


Figure 9.4.1 Examples of IGBT series connection without critical voltage distribution

In series connection, a symmetrical voltage distribution between the components connected in series in the blocking (static) and switching on and off (dynamic) state is crucial.

9.4.2 Static, dynamic voltage symmetry and derating

To increase the blocking voltage of power electronic switches, IGBT modules may be connected in series. In module applications, series connection applies to both the transistors and the corresponding inverse and freewheeling diodes.
Maximum utilisation of the switch generated by series connection is only achieved in the case of ideal static (i.e. in blocking mode) and dynamic (i.e. at the moment of switching) voltage balancing among the individual modules. This is why, in real applications where series connection is used, it is crucial that symmetry be optimised.

Category	Influencing factor	Static sharing	Dynamic sharing
Cooling	T_j	x	x
Semiconductor	Leakage current $I_{CES} = f(V_{CE}, T_j)$	x	
	Transferkennlinie $I_C = f(V_{GE}, T_j)$		x
	Threshold voltage $V_{GE(th)}$		x
	Transfer characteristic g_{fs}		x
	Switching time $t_{don,}$ $t_{doff,}$ $t_{r,}$ $t_{f,}$		x
Driver	Output impedance incl. Gate resistors		x
	Gate voltage slope $v_{CE} = f(V_{GE}(t), T_j)$		x
Circuit	Emitter coupling impedance		x

Table 9.4.1 Key factors influencing the current distribution between parallel current paths

9.4.2.1 Cause of static asymmetry

During stationary off-state, symmetry is determined by the blocking characteristic of the series-connected semiconductors. The bigger the blocking current or the lower the blocking resistance, the lower the voltage taken up by the series-connected semiconductor. The blocking current increases exponentially to the increasing temperature. In stationary off-state, the variation in blocking current due to production processes will drive the components with the lowest blocking current into the region of breakthrough voltage. As long as the avalanche stability of the components can be relied on, no resistors will have to be connected. If, however, components with a blocking capability of >1200V are connected in series, it is common practice to use a parallel resistor.

9.4.2.2 Reasons for dynamic asymmetry

The factors influencing dynamic symmetry as described in Table 9.4.1 will all ultimately result in different switching times for the components connected in series. The factors influencing dynamic symmetry as described in will all finally result in different switching times for the components connected in series. The transistor that turns off first and the one that turns on last will be burdened with the highest voltage and, consequently, the highest switching losses. To prevent the maximum permissible semiconductor voltage from being exceeded, the countermeasures discussed in the following section must be taken. Essentially, dynamic voltage distribution may differ from static voltage distribution. If one of the pn-junctions connected in series is free of charge carriers earlier than the others, this will take up voltage earlier, too.

9.4.3 Ways of improving voltage symmetry

Optimum symmetry is essentially achieved by ensuring minor variations in the parameters of the modules in the series connection; for dynamic symmetry minimum differences in the signal propagation times for the driver stages are the key. Different types of modules or modules produced by different manufacturers should not be connected in series. The layout of power and driver circuits is basically to be done with a view to achieving minimum parasitic inductance and strictly symmetrical arrangements.
Modules should therefore be mounted close together and thermally well coupled on a common heat sink. For large parallel systems with several heat sinks, thermal series connection (thermal stacking, see chapter 5.4.4) should be avoided as far as possible. A temperature difference of 10°C means 1.5...2.5 times the blocking current of the same IGBT or diode. However, the hotter semiconductor therefore takes on less voltage and somewhat mitigates the temperature difference.

9.4.4 Ways of improving static voltage balancing

To achieve optimum static symmetry, the influence of different blocking currents has to be decreased by using parallel-connected resistors. This resistor has to be dimensioned with respect to the fact that voltage distribution is always determined by the parallel resistance. If the blocking current is accepted as independent of the voltage and if resistance tolerances are neglected, the simplified rule for dimensioning the resistance for series connection of n diodes is as follows:

$$R < \frac{n \cdot V_r - V_m}{(n-1) \cdot \Delta I_r}$$

V_m: maximum voltage occurring across the entire series connection
V_r: maximum voltage which is to drop across a single semiconductor l
ΔI_r: the maximum variation in blocking/leakage current

This is based on the maximum operating temperature. V_r is to be selected such that sufficient safety margin to the maximum reverse voltage of the component exists (e.g. < 66% V_{CES}). As regards ΔI_r, the following assumption can be made with a sufficient degree of certainty:

$$\Delta I_r = 0.85 \cdot I_{rm}$$

where I_{rm} is specified in the datasheet (see also Figure 2.3.7. The series connection can now be optimised for n and R. Experience shows that for state-of-the-art power semiconductors it is sufficient to dimension the resistor such that at maximum voltage, it will carry current three times the maximum leakage current. However, even then considerable power losses are generated within the resistor. For IGBT modules with integrated antiparallel diode, the total leakage current of both components is to be given as I_{CES}. Here, too, the current conducted through the parallel resistor may be rated to about 3-5 times the transistor blocking current.

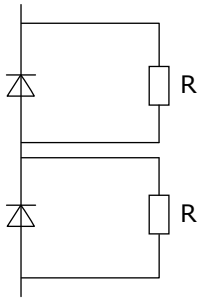


Figure 9.4.2: Resistor circuitry for static voltage symmetry of diodes in series connection

9.4.5 Ways of improving dynamic voltage balancing

9.4.5.1 Passive networks

To achieve dynamic symmetry, RC or RCD networks may be used (cf. Figure 9.4.3). These networks reduce and thus balance dv/dt speeds during switching (compensation of non-linear component junction capacitances). However, the high degree of reliability achieved using RC or RCD networks goes hand in hand with the need for more passive power components, which have to be designed for high voltages. Snubber networks are responsible for generating what in some cases are considerable additional losses. Furthermore, one disadvantage is the fact that the quantitative effect depends on the circuit operating point. That said, an important advantage is the fact that no additional control components are needed and standard driver stages can be used. If capacitor tolerances are neglected, a simple dimensioning rule can be used for this capacitor for series connection of n diodes of a specified reverse voltage V_r:

$$C > \frac{(n-1) \cdot \Delta Q_{rr}}{n \cdot V_r - V_m}$$

Here, ΔQ_{rr} is the maximum variation in diode storage charge. The following can be assumed with relative certainty:

$$\Delta Q_{rr} = 0.3 \cdot Q_{rr}$$

provided diodes from one production batch are used. Q_{rr} is specified by the semiconductor manufacturer. When the freewheeling diode is turned off, the charge stored in this capacitor is generated in addition to the storage charge and also has to be taken up by the IGBT during turn-

on. Based on these dimensioning rules, the resultant charge will be as much as twice the storage charge of a single diode.

If passive networks are combined with active balancing technologies, they may be dimensioned smaller in terms of parameters. In [9.12] and [9.13], a combination of active balancing and a passive RC network is shown. Here, the RC networks have R = 3.3Ω and C = 15nF at a DC link voltage of 2.4kV for four series-connected 1200V / 600A IGBT switches.

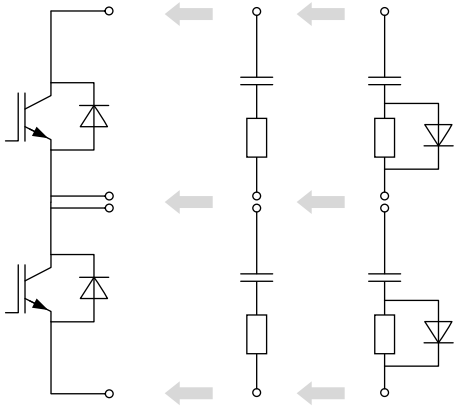


Figure 9.4.3 Passive networks for dynamic voltage symmetry

9.4.5.2 Active balancing measures; switching time correction

Figure 9.4.4 shows a possible way of achieving dynamic voltage symmetry using the principle of switching time correction based on delay time control [9.14]. No additional passive power components are needed for this process. No additional losses occur in the IGBT / MOSFET either.

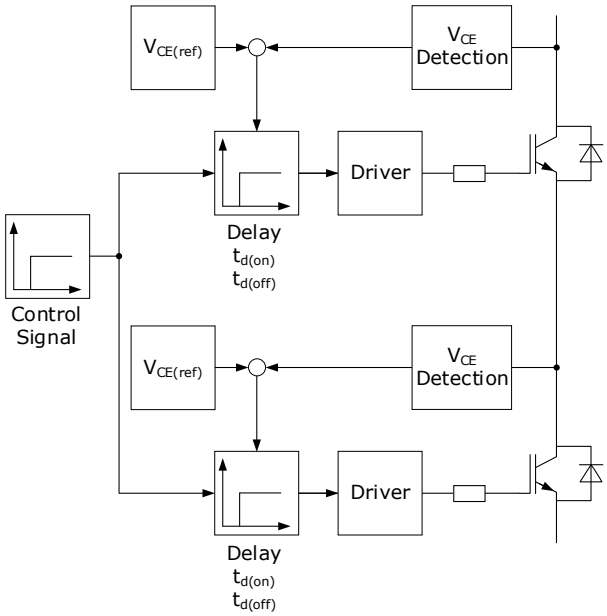


Figure 9.4.4 Principle behind switching time correction

9.4.5.3 Dynamic symmetry by way of dv/dt, di/dt control

In dv/dt control (Figure 9.4.5), reference value for the dv/dt speed of single modules during switching is compared to the actual values by the driver and the difference transmitted to the driver output stage. One problem here is the precise and reproducible capacitive coupling or feedback of the actual dv/dt values. If the dv/dt reference value is lower than the "natural" dv/dt during hard switching, additional losses will be generated in the power transistors. Consequently, the driver layout has to be more sophisticated, and standard drivers may no longer be used. Similarly, di/dt control with inductive feedback of the di/dt speed of IGBT / MOSFET may be implemented [9.15], [9.16].

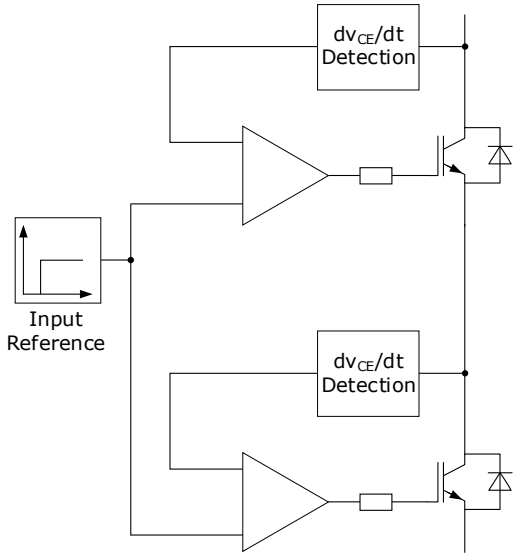


Figure 9.4.5 Dynamic voltage symmetry using dv/dt control

9.4.5.4 Active voltage limitation / Active Clamping

In the process of active clamping [9.13], [9.17], [9.18], [9.19] the collector-emitter voltage or drain-source voltage is measured and fed back to the gate via a Zener element (cf. chapter 9.6.2.4, Figure 9.4.6). If the transistor voltage exceeds the given maximum voltage, the gate voltage will be increased to such an extent that the operating point is shifted to the active region of the output characteristic in accordance with the collector/drain current that is flowing.
The additional losses generated in the transistor during active clamping are relatively low. Active clamping has no influence on the symmetry of the switching edges. This method works without time delays, the limitation voltage value being independent of the operating point of the inverter. A further advantage is the fact that almost any standard driver may be equipped with the clamping device and that active clamping will be performed automatically for antiparallel diode turn-off, too. Protection is guaranteed even in the case of driver supply voltage failure.

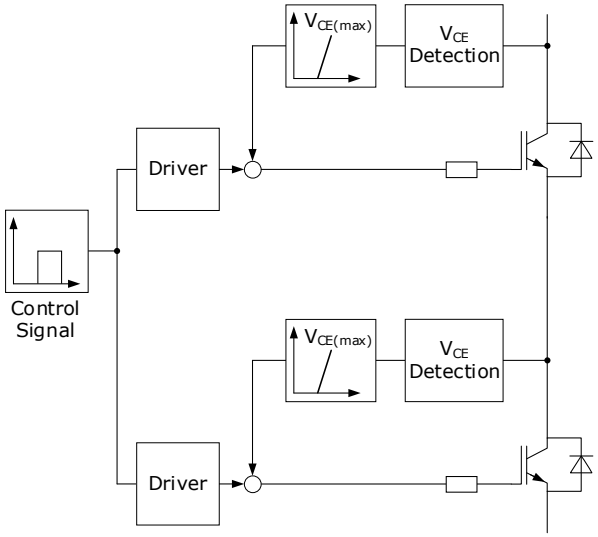


Figure 9.4.6 Active voltage limitation / active clamping

9.4.5.5 Master slave concepts

An adaptation of the commonly known master slave principle, which originates from thyristor technology [9.20], can also be used to achieve dynamic voltage symmetry (Figure 9.4.7). Only the bottom switch (master) is equipped with a complete driver circuit with auxiliary power supply and potential-separated control pulse input. This is the major advantage of the principle. The driver circuit of the top switch (slave) integrates nothing but the output stage. The decoupling between master and slave is done by a high blocking diode. The slave will be turned on as soon as its emitter potential has dropped to a point where the decoupling diode is able to turn on, i.e. with a

slight time delay. The slave is turned off by blocking the decoupling diode. In principle, several slaves may be connected in cascade. While this concept is able to achieve turn-off symmetry rather well, turn-on symmetry is very limited. For this reason, a combination of the master slave concept and active clamping is recommended. The disadvantage of limited turn-on symmetry can be ignored in ZVS applications.

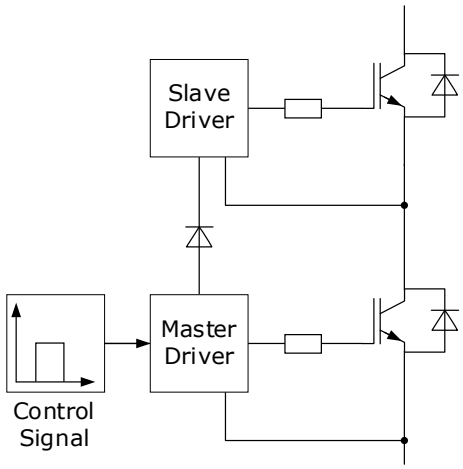


Figure 9.4.7 Basic principle behind the master slave concept

9.4.6 Conclusions

In addition to the high-resistance parallel resistors for static symmetry, passive and/or active measures to achieve dynamic symmetry must be taken when IGBT or MOSFET modules are connected in series. With the exception of active clamping, the methods shown here will protect the transistors only, meaning that additional passive networks will be needed to protect the inverse diodes.

9.5 Drivers

9.5.1 General requirements

In transistorised power electronics systems, the term “driver” or “gate driver” is generally used to describe the circuit connecting the low-voltage controller (containing software and system logic) to the high-voltage power switches, e.g. modules, containing IGBT or Silicon/Silicon Carbide MOSFET.

General functions of gate drivers are for example:

- Generation of gate currents to turn/turn-off the transistor according to the unit control signals,
- Providing the electrical isolation between control unit and power section,
- Adjustment of gate voltage and current profile for application-optimised switching behaviour and low losses inside the power semiconductors,
- Input pulse forming, short pulse suppression
- Protection of the power semiconductors as well as the power electronic system against overload by monitoring e.g. output current/short circuit, temperature and operation voltage including error management and error signal transfer

The Table 9.5.1 lists the fundamental functionalities of different gate driver designs.

<table>
<tr><th>Driver design</th><th>Functionality</th><th>Insulation</th><th>Signal transmission</th><th>Energy transmission</th><th>Applications range</th></tr>
<tr><td rowspan="4">Monolithic gate driver IC (External components required)</td><td>Low-side gate driver</td><td>no galvanic isolation</td><td rowspan="2">n.a.</td><td rowspan="2">n.a.</td><td rowspan="3">Low power (< 20kW)</td></tr>
<tr><td>Floating/high-side isolated single switch gate driver</td><td rowspan="2">junction isolation or silicon-on-insulator IC technology</td></tr>
<tr><td rowspan="2">Halfbridge (dual channel) isolated gate driver & H-Bridge/Six- and Sevenpack gate driver</td><td>Level shifter (mainly for high side)</td><td>Bootstrap-circuit (for high side) or none</td></tr>
<tr><td>integrated coreless transformer</td><td>coreless transformer</td><td>Bootstrap-circuit (for high side); a low-side supply voltage is needed</td><td>Medium to high power (20…>250kW</td></tr>
<tr><td>Primary side controller</td><td>no galvanic isolation</td><td colspan="2">Pulse transformer or opto-coupler and external secondary-side circuit needed</td><td></td></tr>
<tr><td rowspan="2">Driver cores, plug-and-play gate drivers</td><td rowspan="2">Single switch, H-Bridge/Six- and Sevenpack gate driver circuits</td><td rowspan="2">galvanic isolation</td><td>Optocoupler or pulse transformer</td><td rowspan="2">DC/DC converter</td><td>Medium power (100… 250kW)</td></tr>
<tr><td>Fibre Optic</td><td>High power (> 250kW)</td></tr>
</table>

Table 9.5.1 Fundamental functionalities of IGBT and MOSFET gate drivers

Commercial IGBT or MOSFET gate drivers are available in three basic complexities [9.9]:

Driver IC

Broad category of integrated circuits from basic level shifters (e.g. 3.3V logic input, high current bipolar output) to complete driver circuits integrating logic and isolation into one transfer-moulded package (Figure 9.5.1 a)). Driver ICs are limited to lower power applications due to the physical limitations of the package. Most driver ICs require power supply circuitry to achieve full functionality, some driver IC requires additional isolation.

Driver cores

For medium to high power applications, a driver core (Figure 9.5.1 b) provides all of the functional blocks of a complete driver IC, but on a larger scale. Isolation is usually achieved with pulse transformers or optocouplers. The complete circuit is arranged on a PCB that can be plugged/soldered into a larger board. This design allows flexibility to adjust gate resistance and trip levels for specific modules.

Plug-and-play drivers

Complete driver boards for some widely spread modules in industry-standard housings, containing all the features of a driver core plus the requisite gate resistors and configuration components for a specific module type are already installed. The PCBs are designed to directly press, solder, or plug into a certain module housing (Figure 9.5.1 c).

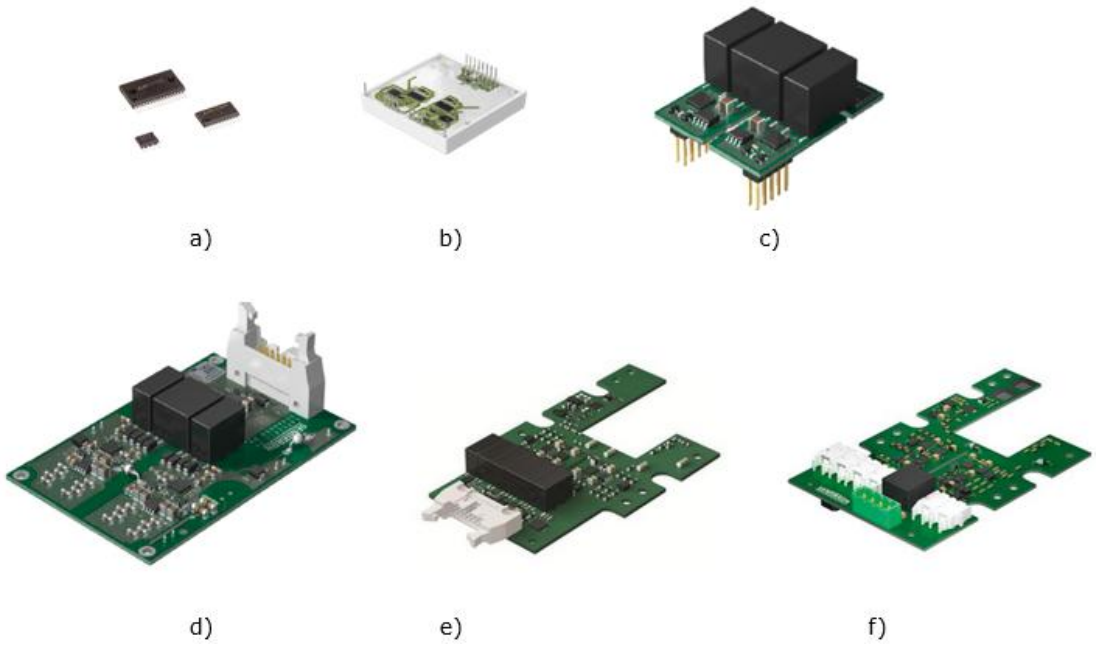


Figure 9.5.1 Examples of IGBT gate drivers: a) Driver ICs; b) SKHI 21/22 driver core (hybrid) c) SKYPER 12 PV driver core (PCB); d) SKYPER 12 press-fit plug-and-play driver for SEMiX 3p modules; e) SKYPER Prime plug-and-play driver for SEMITRANS 10 modules; f) SKYPER Prime O plug-and-play driver with optical signal transmission

Drivers are categorized according to the maximum blocking voltage of the devices they are designed to drive (e.g. 1200V, 1700V). This value corresponds to the voltage that used for the type testing of the driver (V_{isol}), which is mainly determined by the isolation barrier between primary and secondary. Transformer-based isolation barriers, as used in most Semikron Danfoss driver products, are particularly robust in this regard with a typical AC RMS isolation test voltage rating of 4kV. Relevant standards and methods for testing voltage isolation are given in [9.21]

9.5.2 Characteristics of gate voltage and gate current control

9.5.2.1 General

As already described in chapters 2.4.3 and 2.5.3, the switching behaviour of IGBT and MOSFET can be largely controlled by the gate capacitance recharge speed of "gate capacitance" (input capacitance C_{GE} plus voltage dependent miller capacitance C_{CG}). In theoretical borderline cases, the gate capacitance recharge may be controlled by resistance or current (Figure 9.5.2).

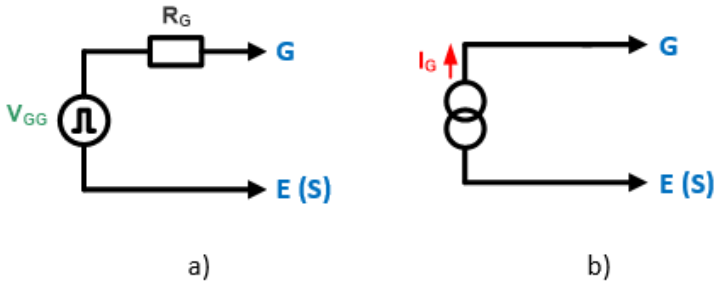


Figure 9.5.2 Gate driving process for IGBT and MOSFET: a) Control by resistance; b) Control by current

The Figure 9.5.3 shows simulated courses of gate current, gate-emitter and gate-collector voltage at turn-on a 400A IGBT.

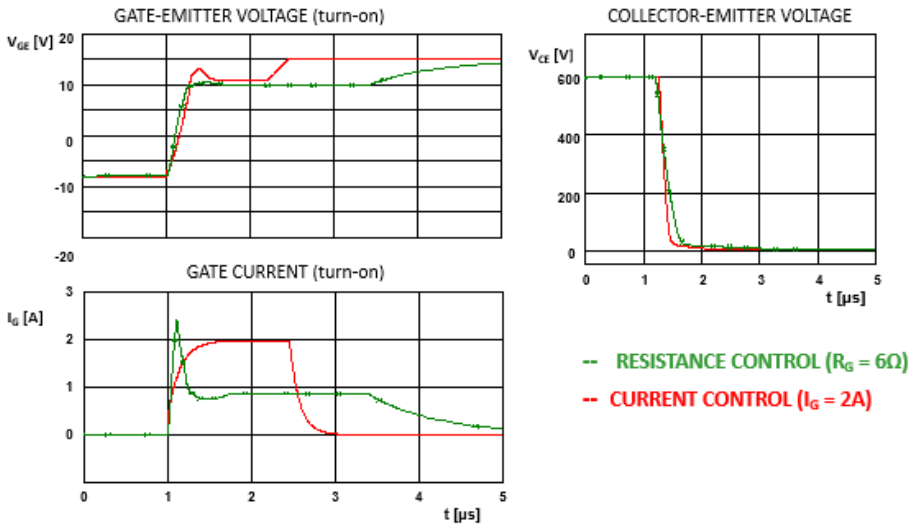


Figure 9.5.3 Simulated gate current, gate-emitter and gate-collector voltage characteristics during turn-on of a 400A IGBT at V_{CC} = 600V, I_C = 300A, $V_{GE(off)}$ = -8V, $V_{GE(on)}$ = +15V

The most commonly used approach is the "control by resistance" via gate resistor (or two separate resistors for turn-on and turn-off), since this is the most practical way of implementing the circuit. Characteristic here is the Miller plateau in the gate-emitter (gate-source) voltage.
Switching speed is adjusted by gate resistor R_G at a continuous supply voltage V_{GG}; the smaller the resistance R_G, the shorter the switching times. In applications using modern IGBT technologies, it may be observed that the turn-off behaviour is not controlled by R_G anymore.
The disadvantage of resistance-based control is that the gate capacitance tolerances of the MOSFET or IGBT will have a direct influence on switching times and switching losses; beyond that, the maximum values for the di/dt and dv/dt during switching are not fully controllable with modern IGBT.
Current control using a "positive" and "negative" gate current generator determines the gate charge characteristics and is comparable to resistance control with respect to gate voltage characteristics. In practice, current control is also used for controlled, one-off slow turn-off due to overcurrent or short circuit. For IGBT, the turn-on and turn-off voltages $V_{GE(on)}$ and $V_{GE(off)}$ are compliant for a given chip technology and selected as a compromise between:

- Protecting the gate oxide (not exceeding V_{GES}/V_{GSS}, also for high di_G/dt and at overcurrent turn-off
- Immunity to parasitic turn-on [9.23]
- Switching speed, switching losses
- Conduction losses (Dependence of V_{CEsat} on $V_{GE(on)}$)
- Cost/complexity (bipolar vs. unipolar Gate voltage supply)

In most cases, the gate control voltages are fixed for off-the-shelf driver solutions so it is only necessary to be aware of the used voltages when looking at other datasheet values (e.g. gate charge Q_G).

9.5.2.2 Turn-on control voltage

The dependencies of the IGBT and Si/SiC power MOSFET forward characteristics on the turn-on control voltage can be derived from their output characteristics. In Figure 9.5.4 this is explained by way of an example each for Semikron Danfoss IGBT and SiC MOSFET modules using the diagrams given in the datasheets.

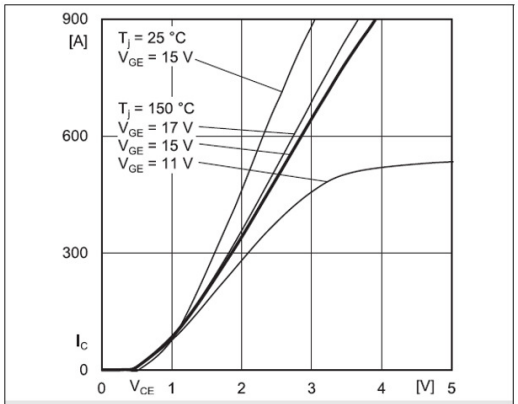


Fig. 1: Typ. output characteristic, inclusive $R_{CC'+EE'}$

a)

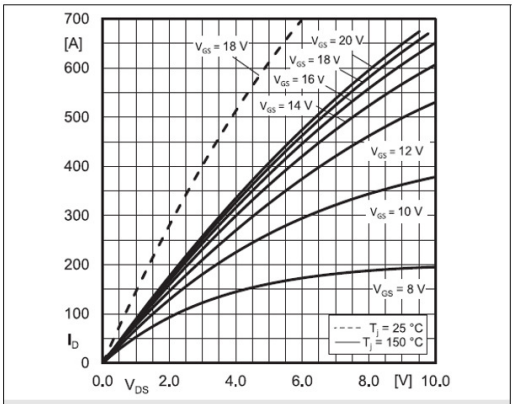


Fig.1: Typ. MOSFET forward output characteristic, incl. $R_{DD'+SS'}$

b)

Figure 9.5.4 Typical output characteristics as a function of the turn-on control voltage: a) IGBT module SEMiX453GB12M7p [9.25]; b) SiC MOSFET module SKM350MB120SCH15 [9.26]

The IGBT collector emitter saturation voltage V_{CEsat} and MOSFET's Drain-source on-resistance on-state voltage V_{DS} are inversely dependent on the gate-emitter voltage V_{GE} resp. gate-source voltage V_{GS}.

The ranges of turn-on control voltages recommended by the manufacturers are as follows

- IGBT: $V_{GE(on)}$ = +15…17V (max. rating 20V)
- Si MOSFET: $V_{GS(on)}$ = +10…15V (max. rating 20V)
- SiC MOSFET: $V_{GS(on)}$ = +15…20V (max. rating 20…22V)

In practice, this means that a high turn-on control voltages has the following consequences:

- lower conduction losses,
- higher short circuit currents (see below),
- (with unchanged gate resistors R_G) faster turn-on, lower switching energy & -times, but longer turn-off propagation delay

On the other hand, low turn-on control voltages have the following consequences:

- higher conduction losses,
- risk of desaturation at peak currents (for IGBT7 at 2…3 · I_{Cnom}), see below,
- (with unchanged gate resistors R_G) slower turn-on, higher switching energy & - times but shorter turn-off propagation delay

Especially when using modules with IGBT of the 7th generation in applications with high pulse currents or capacitive load (for example shielded motor cable), higher turn-on control voltages might be advantageous to prevent desaturation effects. For example, at the upper limit of the permissible junction temperature range, desaturation can already occur at twice the nominal current (Figure 9.5.5).

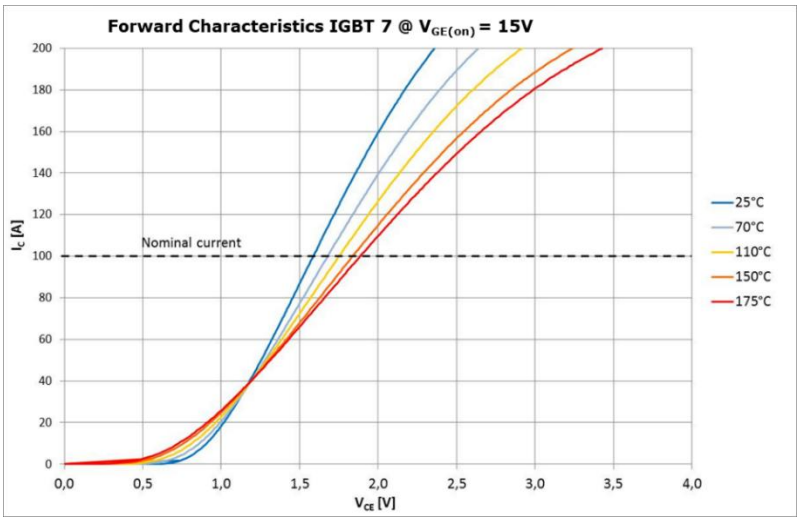


Figure 9.5.5 Exemplary forward characteristic of a 100A, 7th generation IGBT

For SiC MOSFET the example of SKM350MB120SCH15 in Figure 9.5.4 b) illustrates the following behaviour: Because the V_{DS}-difference between V_{GS} = 16V and V_{GS} = 20V at nominal drain current I_{Dnom} is 0.8V (+50% at only 16V), the recommended value of gate-source voltage should be between 18V and 20V, considering the maximum permissible value of V_{GS} = +22V.

Therefore, for low on-state drain-source voltage, a possible high positive gate voltage $V_{GS(on)}$ is required, especially at operation with high peak currents and at low temperatures (risk of "desaturation" for $I_D > I_{Dnom}$ at $V_{GS(on)}$ in the range of only 15V. For more detailed considerations concerning the SiC MOSFET turn-on gate-source voltage, please see chapter 9.5.6 below.

Influence of the turn-on gate control voltage on the IGBT or MOSFET short circuit current

For IGBT and SiC MOSFET there is a general trade-off between short circuit capability and forward losses in the case of short circuit. Because of the heating up the chip volume by the short circuit current I_{sc} with the power $P = V_{DC} \cdot I_{sc}$ becomes more and more critical the further chip area and chip thickness are shrunk in modern IGBT and SiC MOSFET. Especially for SiC MOSFET with their comparatively small chips, the short circuit capability is a critical design criterion.
Also complicating optimisation of short circuit protection are the steep current and voltage transients occurring with fast-switching IGBT and even more so with SiC MOSFET, which make noise-free chip-level measurements virtually impossible with transistor modules.
A drastic limitation of the short circuit current I_{sc} by using a correspondingly low gate voltage $V_{G(on)}$ would allow a longer permissible short circuit time t_{psc}, but would increase the forward losses during normal operation.
Manufacturers of IGBT and SiC MOSFET chips today have very different approaches to trade-off mentioned: the permissible short circuit durations range from 0 to about 10µs.
In the IGBT data sheets, the maximum short circuit duration t_{psc} is given as a limit value, which applies at V_{CE} = 15V. At V_{GE} = +15V, IGBT limit the collector current I_{SC} to 4…5 · I_{Cnom} (IGBT4) or to 3…4 · I_{Cnom} (IGBT7).
A higher turn-on voltage value increases the short circuit collector current I_{SC} and – for the same energy dissipation at short circuit - a shorter t_{psc} is required, see chapter 7.3.2.1, paragraph "Turn-on time during short circuit t_{psc}".
Today's SiC MOSFET are not yet able to handle adequate current limitation. In contrast to IGBT chips, power dissipation during short circuit is produced almost entirely within the channel structure and only heats the surface of the chip, not the complete chip volume. Also SiC MOSFET chips are much smaller than an equivalent IGBT with a higher current density, cf. chapters 2.5 and 7.5.2.1.

9.5.2.3 Turn-off control voltage

The ranges of turn-off control voltages recommended by the manufacturers are as follows

- Low power IGBT: $V_{GE(off)}$ = 0…-5
- High power IGBT: $V_{GE(off)}$ = -7…-15V (max. rating -20V)
- Si- MOSFET: $V_{GS(off)}$ = 0…-3…-5V (max. rating -20V)
- SiC MOSFET: $V_{GS(off)}$ = 0…-3…5V (max. rating manufacturer-dependent, see chapter 9.5.6.3)

In bridge topologies, the gate voltage for power transistors should be negative to the emitter (source) potential during turn off and off-state to prevent parasitic turn on effects with cross conduction over a halfbridge. The smaller the gap between the gate turn-off voltage and the threshold voltage $V_{GE(th)}$ ($V_{GS(th)}$), the more risk there is of a parasitic turn-on of the transistor. Parasitic switching can be caused by the feedback effect of the Miller capacitance or by the influence of the parasitic inductance in the emitter branch. If a halfbridge-transistor turns on parasitically, a cross current may flow in the halfbridge, which creates additional losses in both of the transistors.

Effect of the Miller capacitance causing parasitic turn-on (example IGBT)

The Miller capacitance C_{GC} (gate-collector capacitance) exists due to the internal structure of the IGBT. In the equivalent circuit the capacitances C_{GE} (gate-emitter capacitance) and C_{GC} are arranged in series (Figure 9.5.6). Any change in the collector-emitter voltage causes a displacement current i_{GC} through the Miller capacitance.

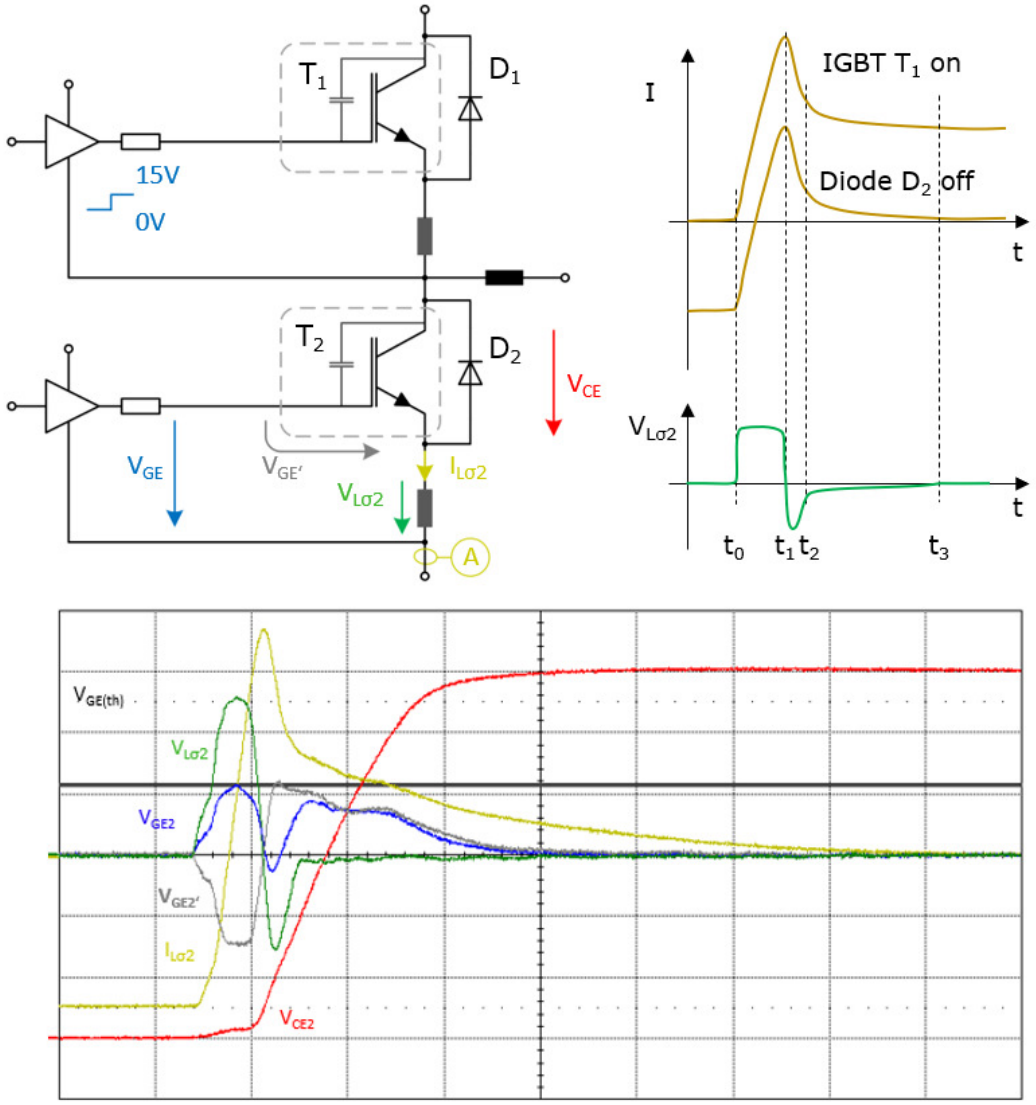


Figure 9.5.6 IGBT halfbridge module: Effects of displacement current I_{GC} and induction voltage $V_{L\sigma}$ of "passive" IGBT T2 at switching IGBT T1

The value of the displacement current is calculated from the product of the magnitude of the Miller capacitance and the rate of change of the collector-emitter voltage.

$$i_{GC}(V_{CE}) = C_{GC}(V_{CE}) \cdot \frac{dv_{CE}}{dt}$$

The current i_{GC} increases the voltage at the on-chip gate-emitter capacitance and thus the gate-emitter voltage $V_{GE'}$ of the IGBT, whose amplitude depends on the capacitive voltage divider of the capacitances C_{GC} and C_{GE}, the internal gate resistance and the gate's external circuitry. Once the gate-emitter voltage $V_{GE'}$ reaches the threshold voltage, the IGBT begins to conduct. A cross-current flows in the halfbridge, causing additional losses in both IGBT. With high-quality semiconductor models the effect can be simulated; a first indication of the risk can be given by using the following formula with the C_{rss} value at high voltage:

$$\Delta V_{GS} = \Delta V_{DG} \cdot \frac{C_{rss}}{C_{GE}}$$

ΔV_{DG}: approx. V_{DC} in the case of a halfbridge circuit

Effect of the parasitic inductances causing parasitic turn-on (example IGBT)

The unavoidable presence of module-internal parasitic inductances in current paths shared by both the load circuit and the gate circuit, will influence the IGBT's gate-emitter voltage $V_{GE'}$ when switching the load current. Figure 9.5.6 also shows the parasitic inductances in the gate-emitter

path of each halfbridge IGBT. For simplicity, only one inductance is shown. In practice, this is a complex system of self-inductance and coupled inductances of the power and control circuit. For example, when turning on the IGBT T1 in which the load current of the diode D2 commutates to IGBT T1. During the decay phase of the reverse current of diode D2, the gate-emitter voltage $V_{GE'2}$ of IGBT T2 is raised because of the inductive voltage $V_{L\sigma 2}$, build up across the parasitic inductance of T2 increases the gate-emitter voltage.

$$v_{L\sigma 2} = L_{\sigma 2} \cdot \frac{di_{L\sigma 2}}{dt} \quad \text{with} \quad v_{GE'2} = V_{GE2} + v_{L\sigma 2}$$

If $V_{GE'2}$ reaches the value of the threshold voltage, IGBT T2 turns on and a cross-current flows in the halfbridge, causing additional losses in both IGBT too. Since the C_{GE}/C_{GC} ratio is higher for IGBT of the 7th generation (e.g. IGBT7) than for IGBT of the 4th generation (e.g. IGBT4), the parasitic turn-on limit is significantly higher for IGBT7 than for IGBT4. Therefore, a negative gate-emitter voltage can be omitted for IGBT7 in many applications (unipolar switching, see Figure 9.5.7).

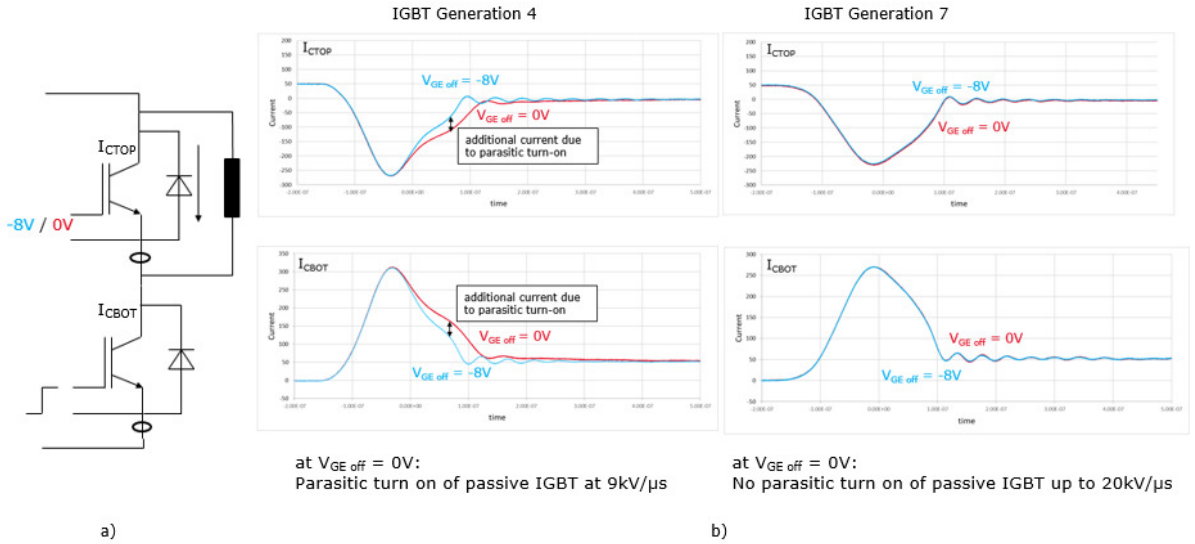


Figure 9.5.7 Comparison of cross currents of IGBT4 and IGBT7 in an IGBT bridge arm due to turn-on by dv_{CE}/dt feedback of the passive IGBT a) Circuit diagram, b) Collector current characteristics

Influence of unipolar switching ($V_{GE(off)}$ = 0V) on the turn on/off delay times

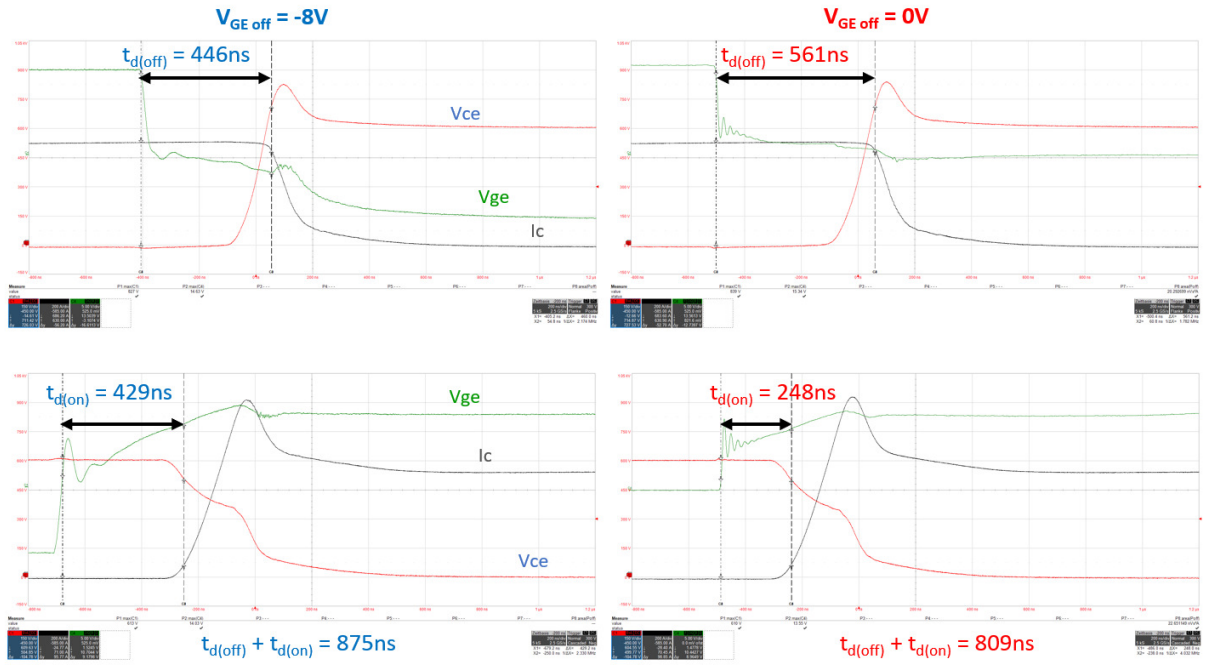


Figure 9.5.8 IGBT7: Impact of unipolar gate control on the delay times $t_{d(on)}$ and $t_{d(off)}$ at V_{CC} = 600V, I_C = 700A, T_j = 150°C and matched R_G values

As can be easily deduced from the physical relationships, unipolar control with unchanged $V_{GE(on)}$ at matched R_G causes a reduction of the turn-on delay time $t_{d(on)}$ and an extension of the turn-off delay time $t_{d(off)}$. In the measured example, the sum of $t_{d(on)}$ + $t_{d(off)}$ decreases insignificantly (approx. 9%) with unipolar switching (Figure 9.5.8).
Because of faster turn-on and slower turn-off at unipolar switching ($V_{GE(off)}$ = 0V), in bridge circuits the required deadtime (time between turn-off of one IGBT and turn-on the other IGBT) must be increased in the order of 30%, compared to bipolar switching.

9.5.2.4 Control current ratings, driving power

Gate charge Q_G

While the internal capacitances of IGBT and MOSFET influence its switching characteristics, they are not directly suitable to size the driver. For that, the gate charge characteristic is used for calculation of driving current and driving power, required for each IGBT or MOSFET of a module. The required gate charge Q_G of a selected IGBT or MOSFET at specified working voltage and current depends on the voltage hub between the positive turn-on voltage and negative turn-off voltage of the driver $V_{GE(on)}$ + $V_{GE(off)}$. Q_G can be found in the corresponding data sheet table "characteristic values" in form of a diagram, e.g. as Figure 6 of the SEMITRANS® Datasheets by Semikron Danfoss, see Figure 9.5.9.

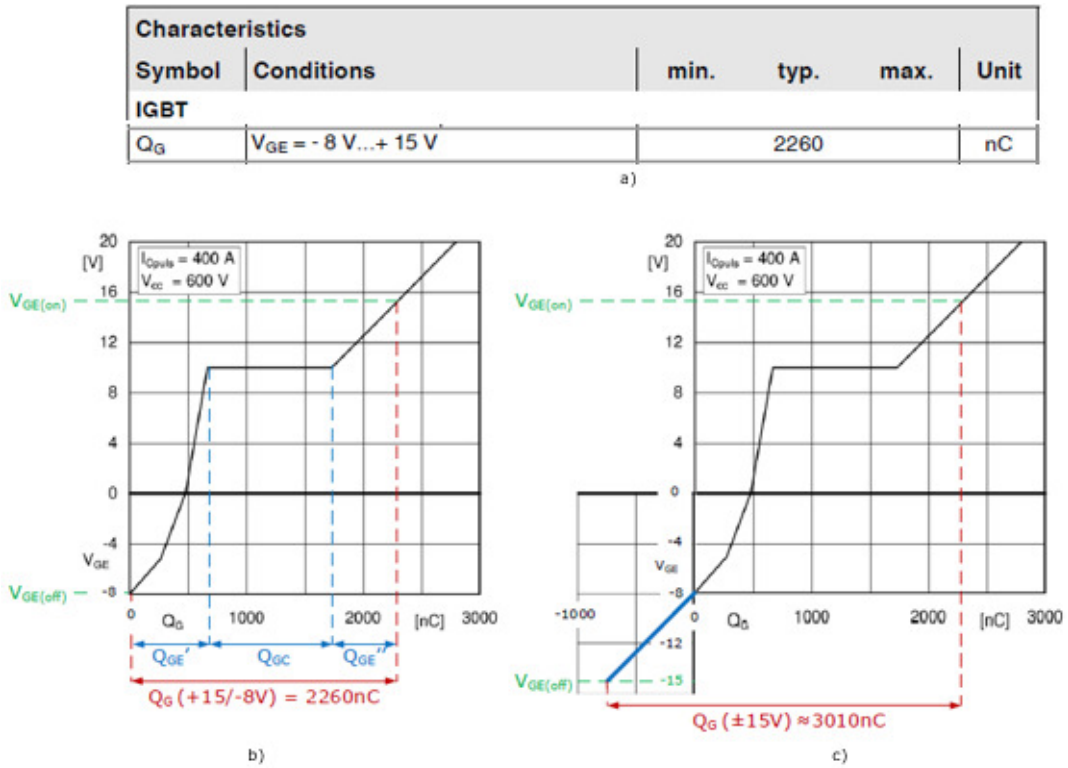


Figure 9.5.9 Exemplary gate charge characteristic from IGBT SKM400GB12E4 datasheet [9.28]: a) Characteristic datasheet value for a selected hub of gate-emitter voltage; b) Dependence of the gate charge Q_G of an IGBT on the gate-emitter voltage hub; c) Extrapolation method for different $V_{GE(off)}$ [9.9]

The gate driver must be able to source or sink the gate charge every switching event without a significant drop of the voltage at the secondary-side power supply (e.g. +15V, -8V). A drop in this voltage during switching can lead to increased switching losses. Because of this, gate driver datasheets give a value for maximum output charge per pulse, Q_{out}, which must be above the value of Q_G determined above.
In some cases, Q_{out} is given with the caveat that some additional boost capacitance must be added by the user. For Semikron Danfoss IGBT gate drivers, the method for calculating this capacitance is given in the respective Technical Explanations. Capacitors are placed on the secondary side in parallel with both the TOP (e.g. 15V) and BOT (e.g. -8V) connections and should be close to the driver power supply pins. It is strongly recommended that these be ceramic capacitors, where electrolytic or tantalum types are to be avoided. Additionally, drivers may require that the additional secondary-side capacitance be duplicated on the primary side as well [9.9], [9.38].

Average gate current I_{GAV} and driving power P_{GAV}

With the gate charge for Q_G (for a given gate-emitter voltage hub) a given device determined, the required average gate current I_{GAV} can be calculated as a function of the transistor's switching frequency f_{sw} as:

$$I_{GAV} = f_{sw} \cdot Q_G$$

An IGBT driver datasheet gives the value $I_{out(avg)}$, the average output current capability per channel (Figure 9.5.10 a). Therefore, the calculated value I_{GAV} must be smaller than $I_{out(avg)}$, which may be derated with temperature. Similarly, the average driving power required can be calculated by factoring in the total available gate voltage (example IGBT):

$$P_{GAV} = I_{GAV} \cdot (V_{GE(on)} + V_{GE(off)})$$

Semikron Danfoss datasheets don't contain an explicit value for the output power but instead diagrams with the permissible working areas switching frequency over gate charge and maximum operating temperatures for the allowed average output current at various switching frequencies, see Figure 9.5.10 b) for the example of the driver core SKYPER 42 LJ PV [9.27], .
However, the data sheet tables contain information on the maximum permissible values for driver switching frequency f_{max} and peak output current $I_{out(peak)}$ (Figure 9.5.10 a).
While the rating for $I_{out(peak)}$ is valid over the full operating temperature range, The maximum rated average output current is limited by the operating temperature T_{op} and the switching frequency. The rated maximum switching frequency itself is also limited by the operating temperature, see Figure 9.5.10 b) and c).

Absolute Maximum Ratings

Symbol	Conditions	Values	Unit
$I_{out(peak)}$	Output peak current[1)]	35	A
$I_{out(avg)}$	Output average current[1)]	180	mA
f_{max}	Maximum switching frequency[2)]	100	kHz

a)

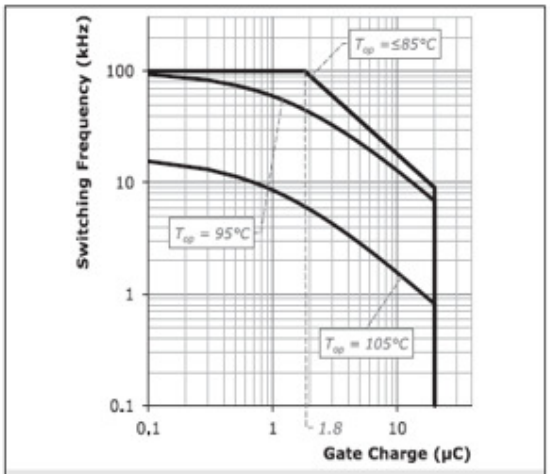


Fig. 1: Maximum Switching Frequency

b)

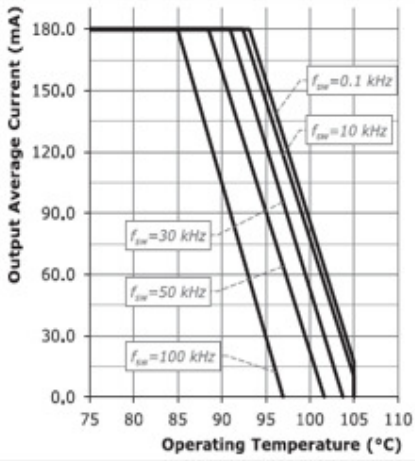


Fig. 2: Output Average Current

c)

Figure 9.5.10: a) Driver Datasheet table with the maximum ratings for $I_{out(peak)}$, $I_{out(avg)}$ and f_{max}; b) Diagram f_{max} over Q_G and T_{op}; c) Diagram $I_{out(avg)}$ over $T_{j(op)}$ and f_{sw} [9.27]

Peak gate current $I_{G(peak)}$

The peak current that occurs in the gate circuit during every turn-on or turn-off event can be roughly calculated using the driving voltage and the total resistance in the gate circuit. In reality, the inductance in the gate circuit further limits the current but since it may not be known during

the initial design stages. The absolute worst-case peak current can be estimated for example for IGBT modules on the driver circuit diagram in Figure 9.5.11 as:

$$I_{G(peak)} = \frac{V_{GE(on)} - V_{GE(off)}}{R_{G^*} + R_E + R_{Gint}}$$

(Calculate with R_{Gon} or R_{Goff} for R_G*.)

The value of an internal IGBT module gate resistance R_{Gint}, listed in the data sheets, is required for the calculation of the peak gate current. All datasheet values for switching losses, switching speeds, etc. already account for this resistance. Therefore, all "R_G" values give on the datasheet are for external, user-applied gate resistors.

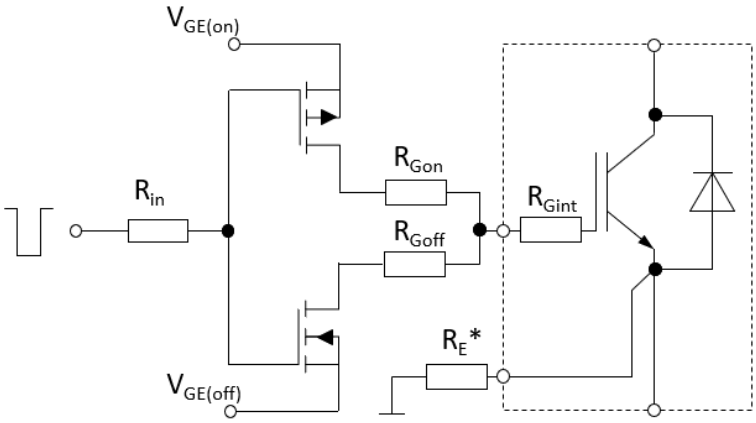


Figure 9.5.11 Circuit diagram (example IGBT) with R_{Gon}, R_{Goff}, R_{Gint} and R_E for calculation of peak gate current

R_{Gint}: internal gate resistor (parallel connected resistors for each parallel chip);
R_E: external resistor for balancing the symmetry of parallel modules (if applicable)

The gate drivers value $I_{out(peak)}$ must be at least the value of $I_{G(peak)}$ determined above.

9.5.3 Driver parameters and switching properties

9.5.3.1 Common gate resistor dimensioning rules

As explained in chapter 9.5.2, the gate resistor controls the charging and discharging of a (gate) capacitance. This, in turn, affects a number of critical parameters:

- Slope of collector-emitter (drain-source) voltage, dv/dt
- Slope of change of collector (drain) current, di/dt
- Transistors switching times and switching losses
- Reverse recovery characteristics of freewheeling diode
- Compliance with the reverse biased safe operating area (RBSOA)
- Compliance with the short circuit safe operating area (SCSOA)
- Electromagnetic (high-frequency) emissions

This behaviour varies between technologies (IGBT/MOSFET "generations"), but in general an increased gate resistance will lead to slower switching speed and increased switching losses. Gate resistance selection is a trade-off between maximum allowed voltage slopes (dv/dt), EMI, and switching losses.
Within the manufacturer's module qualification, switching tests are performed to determine the external gate resistors R_{Gon} and R_{Goff} that will minimize switching losses while also maintaining stable behaviour across the safe operating area for the device. This is done with standardized equipment and a low-inductance DC-link structure.
The resulting recommended resistor values (and corresponding switching speeds and losses) are given in the "Characteristics" section of the module datasheet (Figure 9.5.12). While these values can be taken as a starting point, the gate resistors for a given application should be optimised experimentally by the user in his development process. It is recommended to use different values for R_{Gon} and R_{Goff} to achieve low turn-on losses and manage the overvoltage at turn-off.

Characteristics					
Symbol	Conditions		min.	typ.	max.	Unit
IGBT						
R_{Gint}	T_j = 25 °C			1.0		Ω
$t_{d(on)}$	V_{CC} = 600 V I_C = 450 A V_{GE} = +15/-15 V $R_{G\,on}$ = 1.1 Ω $R_{G\,off}$ = 1.1 Ω di/dt_{on} = 6300 A/µs di/dt_{off} = 3800 A/µs dv/dt = 5250 V/µs L_s = 25 nH	T_j = 150 °C		280		ns
t_r		T_j = 150 °C		75		ns
E_{on}		T_j = 150 °C		39		mJ
$t_{d(off)}$		T_j = 150 °C		410		ns
t_f		T_j = 150 °C		100		ns
E_{off}		T_j = 150 °C		49		mJ

Figure 9.5.12 SEMiX453GB12M7p datasheet specification of internal gate resistor R_{Gint} as well as minimum recommended turn-on and turn-off gate resistors R_{Gon} and R_{Goff} [7.27]

9.5.3.2 Influence of gate resistors on switching times and switching losses

The effects of gate resistance on switching times and switching losses are shown in diagrams of the transistor data sheets, cf. chapters 7.3.4 and 7.5.4.
The turn-on resistor (R_{Gon}) determines the turn-on energy of the IGBT/MOSFET as well as the turn-off (reverse recovery) energy of the corresponding freewheeling diode. The turn-off resistor (R_{Goff}) determines the turn-off energy of the IGBT/MOSFET. However, for IGBT of the 4th generation and IGBT of the 7th generation in the typical current range, R_G has only a minor influence on the current fall time and the turn-off losses.
With SiC MOSFET, a lower gate resistance always means comparatively shorter switching times and lower switching losses. Limiting aspects will be discussed below and in the chapters 2.4 and 2.5.

Turn-on

R_{Gon} has a clear influence on rise time t_r and turn-on losses E_{on}, both increase with increased R_G. IGBT of the 7th generation have a high ratio between a small Miller capacitance C_{GC} at high V_{CE} and a large gate emitter capacitance C_{GE}. When the gate voltage exceeds the threshold voltage only C_{GE} is charged by i_G. A high i_G (low R_G) is necessary to achieve a reasonable di_C/dt and low turn-on losses E_{on}. The small Miller-capacitance C_{GC} is discharged during the following plateau phase of V_{GE} with the same low R_G, causing a high dv_{CE}/dt in that case (Figure 9.5.13).

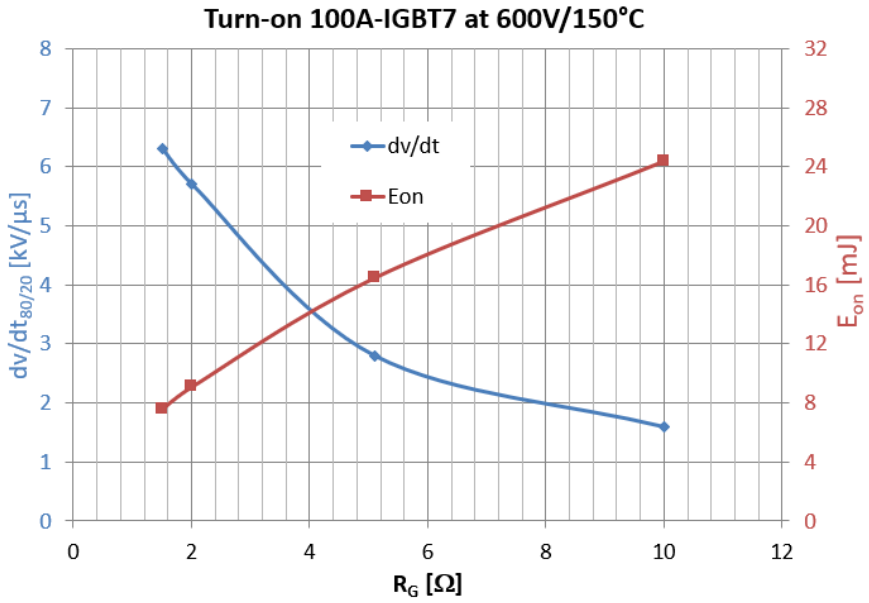


Figure 9.5.13 Typical dependence of E_{on} and dv_{CE}/dt_{on} on gate resistance R_G at turn-on a 100A IGBT7

In general, fast switching is possible and very low turn-on switching losses can be achieved if high dv_{CE}/dt is acceptable for the application. If necessary, by adaption of R_G, a compromise has to be found between dv_{CE}/dt and E_{on} [9.24]. With a larger R_G, the turn-off losses E_{rr} of the freewheeling diode naturally decrease.

In (SiC) MOSFET, the drain current is directly connected to the gate-source voltage during turn-on. Rapid charging of the gate via a low R_G causes very high di/dt of 30...50 kA/µs, which is five to ten times higher than in IGBT modules. The use of the body diode as a commutation partner also leads to recovery losses in the MOSFET chip itself.
The body diodes behaviour differs slightly from the behaviour of the IGBT inverse diodes: In the lower R_G range E_{rr} decreases with R_G increase, but at higher R_G, E_{rr} remains constant or even increases slightly with R_G increase [9.29].
As the falling steepness of the drain-source voltage at SiC MOSFET can get very high (up to 50kV/µs), it is necessary to increase R_G in many applications to reduce the $-dv_{DS}/dt$.
The transfer characteristic of SiC MOSFET shows a negative temperature coefficient, cf. Figure 7.5.18. The consequences of the SiC MOSFET specific temperature dependency are a faster turn-on but a slower turn-off with increasing junction temperature T_j. Thus, the lower limit of the R_{Gon} is set by the turn off overvoltage of the freewheeling diode at the highest junction temperature. In contrast, the lower limit of the R_{Goff} is set by the MOSFET's turn off overvoltage at the lowest junction temperature.

Turn-off

As mentioned above, the influence of the R_G size on the turn-off behaviour is only limited for IGBT of both Generations 4 and 7 [9.22]], [9.24]. The turn-off behaviour is independent from R_G in a certain range typically given in data sheet characteristics. Only a different turn-off delay time in the gate voltage is visible when changing R_G. Consequently, the turn-off losses are almost independent of R_G. The delay time increases for even higher R_G and free charge carriers disappear during that time. This leads to less tail current and an increased di_C/dt of the collector current. An increased di_C/dt causes a higher voltage spike ΔV_{CE} across the parasitic inductances, which is added to the DC link voltage (red range in Figure 9.5.14). At nominal device current this is normally within the gap between DC-link voltage and maximum permissible collector-emitter voltage, but it can become a serious problem at turn-off high overcurrent or short circuit current.
A gate-controlled turn-off behaviour with substantial reduction in the overvoltage is achievable only for very high R_G values but to the disadvantage of high switching losses and a very long delay time in active mode (grey range in Figure 9.5.14). Therefore, relative low R_G values are recommended to assure low switching losses and a low overvoltage.

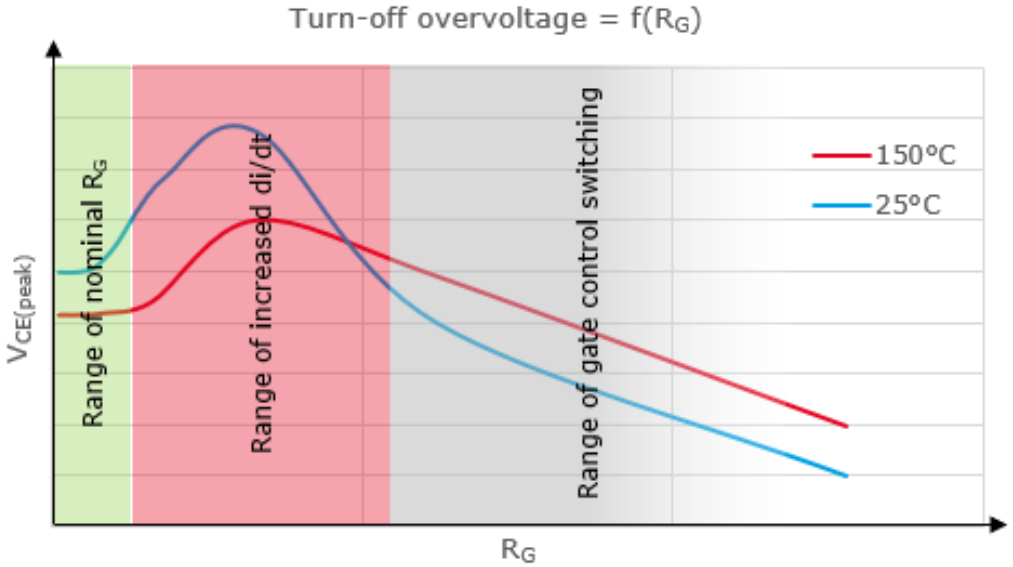


Figure 9.5.14 Basic behaviour of turn-off overvoltage for different R_G at T_j = 25°C and T_j = 150°C [9.24]

In MOSFET made of Si or SiC, di_D/dt of the drain current and the dv_{DS}/dt of the drain-source voltage can be well controlled by the gate resistors, in contrast to IGBT. The statement of many manufacturers for IGBT modules, that twice the nominal current can safely be switched using the datasheet recommended gate resistors is not valid for SiC MOSFET modules because the required gate resistor would be far too large. The current at which the losses are specified is only about 50% of the nominal current, because this is closer to operating conditions for applications with higher frequencies [9.30].

Influence of gate resistors on switching behaviour of the freewheeling diode

The turn-off behaviour of the freewheeling diode is also affected by the turn-on gate resistor and limits its minimum value. This means that the transistor's turn-on switching speed may be only increased up to a level compatible with the reverse recovery behaviour of the freewheeling diode being used.
For example, in chapter 7.3.4, the Figure 7.3.39 depicts a typical dependency of the freewheeling diode reverse recovery current i_{rr} on $-di_F/dt$, determined by the control of the given gate resistor R_{Gon} exemplarily on an IGBT module: The smaller R_{Gon} is selected, the more $-di_F/dt$ and thus also I_{RR} of the freewheeling diode. The Figure 7.3.40 depicts the typical dependencies of the freewheeling diode recovery charge Q_{rr} on $-di_F/dt$, determined by the control of R_{Gon} and I_F before commutation: The smaller R_{Gon} is selected, the more $-di_F/dt$ and thus also Q_{rr} of the freewheeling diode. Naturally, however, Q_{rr} increases to a much greater extent with increasing diode current I_F before commutation. An increase in I_{RRM} will also cause higher turn-off power dissipation in the freewheeling diode, see also chapter 4.6 in [9.9].
In datasheets of IGBT- and SiC MOSFET modules with hybrid integrated SBC diodes, both diagrams don't exist, because I_{RRM} and Q_r will be neglected here.

Gate resistor's power dissipation

A high peak gate current passes through the gate resistor during each switching transition at a frequency typically in the kHz range. This results in a large amount of power dissipated in the small-sized (typically surface mounted PCB) gate resistors.
The construction and size of the gate resistors must be suitable for the switching frequency-dependent high-power dissipation and withstand the high pulse load during the turn-on and turn-off sequences (Figure 9.5.15).

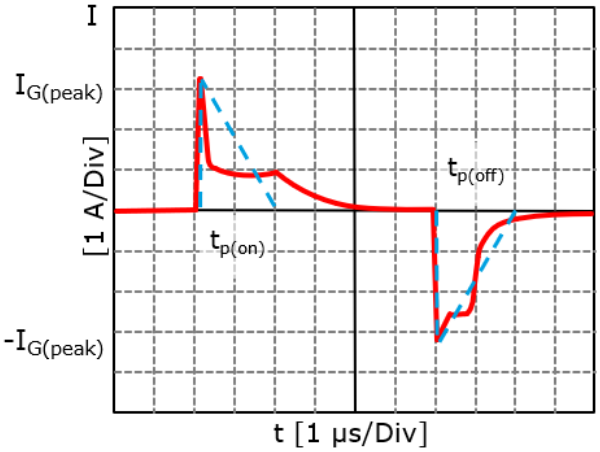


Figure 9.5.15 Current waveform through a gate resistor at IGBT switching

For the RMS value of either turn-on or turn-off gate current $I_{G(RMS)}$ by triangle pulse shape derivation is valid:

$$I_{G(RMS)} = I_{G(peak)} \cdot \sqrt{\frac{t_p}{3 \cdot T}} = I_{G(peak)} \cdot \sqrt{\frac{t_p \cdot f_{sw}}{3}}$$

With relatively low resistance values, high allowable operating temperature and high pulse current capability, MELF metal film resistors are most suitable for the application, preferably several resistors in parallel connection. Paralleling is useful to reduce the peak power, distribute the losses over a wider PCB area and gives redundancy in case of a failure.

Using the general formula for the power dissipation P_{RG} in a resistor R_G:

$$P_{RG(on)} = I^2_{G(on)RMS} \cdot R_{Gon} \qquad P_{RG(off)} = I^2_{G(off)RMS} \cdot R_{Goff}$$

P_{RG}: Power dissipation either in the turn-on or turn-off gate resistor
$I_{G(RMS)}$: turn-on or turn-off RMS gate current
R_G: turn-on or turn-off gate resistor value

Soft turn-off resistor $R_{Gsoft\text{-}off}$

Many drivers offer dynamic short circuit protection (DSCP, V_{CE}-monitoring, DESAT), where the secondary side of the driver can detect a rise in the on-state voltage of a device due to a short circuit and immediately switch off the device. However, turn-off at high current with the "normal" gate resistor can lead to overvoltage across the power transistor, because of the voltage spike produced across the stray inductances of power circuit.
Therefore, gate drivers often incorporate an additional soft turn-off circuit. For soft turn-off an overcurrent does not trigger the transistor for R_{Goff} but a turn-off transistor with a much higher gate resistance than R_{Goff}, see red circuit with $R_{Gsoft\text{-}off}$ in Figure 9.5.16.

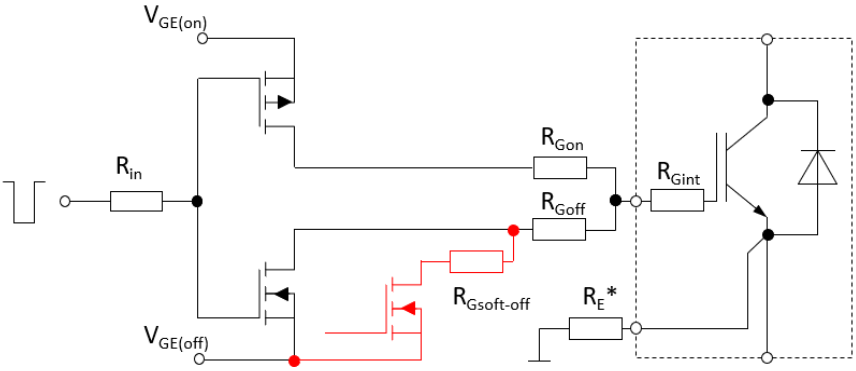


Figure 9.5.16 Gate driver output stage (example IGBT) with R_{Gon}, R_{Goff} and an additional $R_{Gsoft\text{-}off}$ circuit (one of the possible topologies)

A usual starting value for $R_{Gsoft\text{-}off}$ is 10 · R_{Goff}. However, the proper value has to be evaluated in the system in accordance with the individual application parameters. The setup is a balance between staying within the maximum permitted short circuit time t_{psc} of the transistor while also not exceeding the voltage limit V_{CES} (or V_{DSS} for MOSFET), see also the explanations in chapter 4.3 of [9.9].
Alternatively, the soft turn-off circuit can also be implemented via a resistor connected in series with R_{Goff} in the event of a short circuit, by reduction of $V_{GE(on)}$ or by an intermediate step to 0V V_{GE} in the event of a desaturation at short circuit, see also chapter 9.5.4 below.

9.5.3.3 Influence of inductance in the gate circuit

At fast switching of IGBT and especially of SiC MOSFET, their high-speed switching transitions require that minimizing gate circuit inductance L_G is crucial. Otherwise, large gate resistors are required to damp oscillations. A minimum gate resistance for damping oscillations can be calculated by:

$$R_{G,min} > \sqrt{\frac{L_G}{C_{iss}}}$$

This corresponds to a damping factor >=1 in a RLC network. The capacitance is given by the selected semiconductor, remains only a small L_G to switch with a low R_G.
Gate inductance can be reduced by a short distance between driver output stage and semiconductor as well by reducing the loop area of the gate-source path. This is best achieved with a PCB-based design. The emitter resp. source node is laid out on one layer as a larger plane. The gate track is placed on the layer immediately above the emitter (source) contact area.

9.5.3.4 Avoiding passive turn-on by an additional gate-emitter capacitor C_{GE}

Especially for power modules with 4th Generation Trench Field-stop IGBT is an external capacitor between the gate and (auxiliary) emitter terminals an appropriate measure to avoid passive turn on caused by dv/dt induced displacement current across the Miller capacitance (Figure 9.5.17).
The purpose is to decrease virtually the ration of $C_{GC}/C_{GE.}$ It has to be connected directly to the gate terminals and is only useful if the module has no internal gate resistance. Otherwise, it cannot fulfil its purpose in the high frequency domain.
It reduces also the rising gate potential during short circuit events.

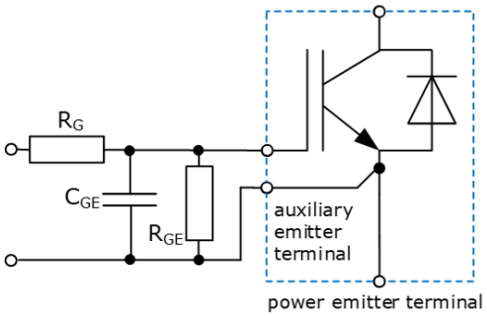


Figure 9.5.17 External Capacitor C_{GE} to avoid passive turn-on

9.5.4 Gate driver circuit structure, description of functional blocks

9.5.4.1 Block circuit

A modern two-channel driver circuit is generally constructed as in Figure 9.5.18 with the critical feature for safety being a clear separation of primary (low voltage) and secondary (high voltage) sides. The controller is interfaced to the primary side, where logic (perhaps in the form of an ASIC) provides short pulse suppression, interlock and/or deadtime, and generally forming the gating signals so that they can be transmitted across an isolation barrier. Additionally, an isolated power supply is needed to provide the positive and negative voltage supply that are used to turn the power devices on and off. Secondary side components include this as well as fast-acting protection features (e.g. DSCP) that avoid the delay of sending an error and the ensuing turn-off signal across the isolation barrier.

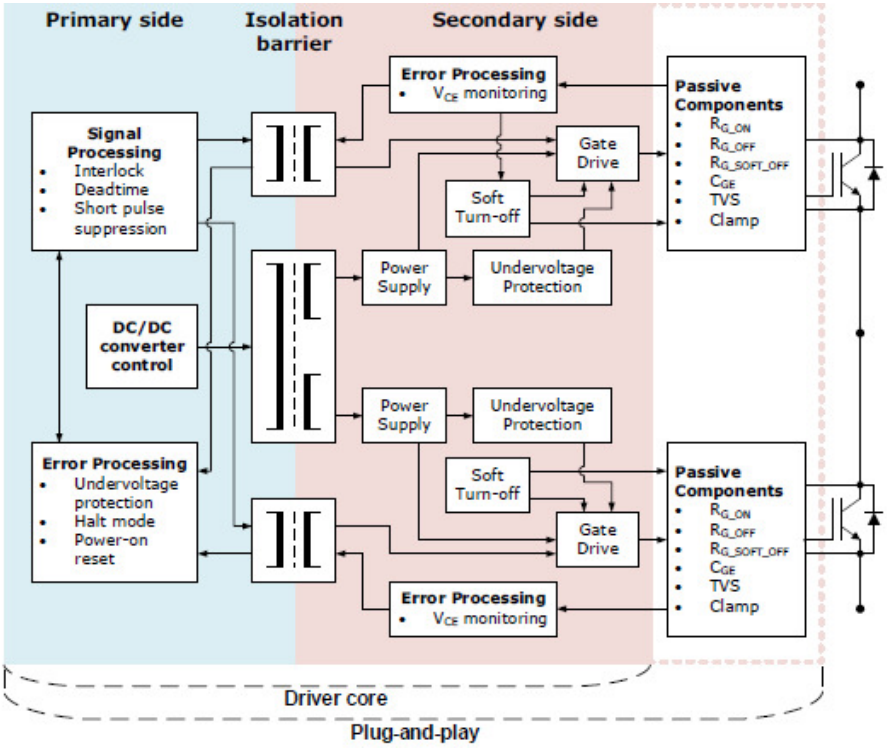


Figure 9.5.18 Two-channel driver block circuit diagram [9.9]

9.5.4.2 Signal processing

Short-pulse suppression (SPS)

When pulse transformers or optocouplers are used to isolate the control signal potential, it is particularly important to ensure that the driver is protected from control pulses (interference pulses, electromagnetic noise) which are too low or too short and might cause the driver to malfunction. The most gate drivers suppress very short on- and off-pulses on the control signal inputs (Figure 9.5.19).

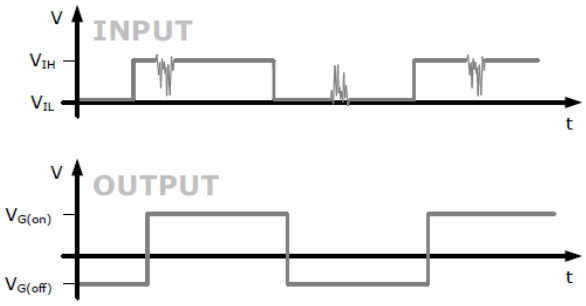


Figure 9.5.19 Short Pulse Suppression

Deadtime (t_{IDT}) generation/bridge arm Interlock TOP/BOT (DT/IT)

To avoid a short circuit in a in voltage source converters, power transistors in the same halfbridge must not be switched on at the same time. In the static state, this may be avoided by interlock of both drivers channels even if the driver input signals are affected by interference. The interlock prevents the two outputs of a dual gate driver from being activated simultaneously.
Because the turn-off of a power semiconductors is much longer than the turn-on (caused essentially by $t_{d(off)} >> t_{d(on)}$) is a deadtime at the transition of the two inverted signals necessary to prevent a bridge leg short circuit during switching. The deadtime generation starts with each turn-off command at the driver's primary side. Depending on the type of transistor, specific application and driver, the deadtime t_{dead} – e.g. for IGBT modules - is typically between 2µs and 6µs. Normally, the deadtime is not added to a deadtime given by the controller. It is possible to control the most driver with one switching signal and its inverted signal. No error signal is generated when signals are overlapped.
Selected drivers realise no deadtime or a deadtime adjustable down to 0µs and interlock can be disabled to enable their use in current source (resonant) converters, where overlapping operation is required or for operating both driver channels independently of each other.

Propagation delay times $t_{d(on)}$, $t_{d(off)}$

The signal propagation times are defined by the time of a change of the driver's input signal until the change of the corresponding output signal.

Adjustable jitter and propagation delay time by input filter selection

Some highly-integrated gate drivers permit the selection of input filter type, jitter and propagation delay time to meet specific requirements of applications. These drivers provide a flexible and individual adjustment of the input filter which also effects the skew/jitter:

- Analogue filter: noise-based skew/jitter; very low jitter of typically ±3ns possible
- Digital filter: skew/jitter is dominated by internal system clock ($1/f_{Clock}$); very low tolerance over the full temperature range

The jitter is defined as the maximum deviation of the switching signal propagation delay time at constant environmental conditions (Figure 9.5.20).

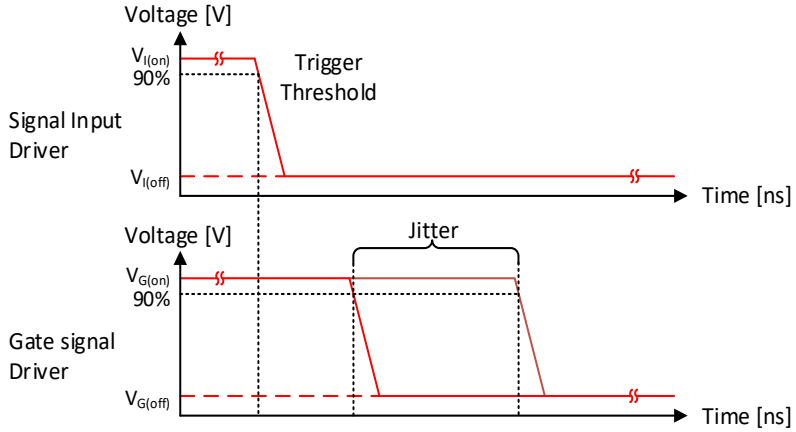


Figure 9.5.20 Definition of jitter time

The skew is defined as the maximum deviation of signal propagation delay times – including the jitter – between individual driver channels which are controlled simultaneously (Figure 9.5.21).

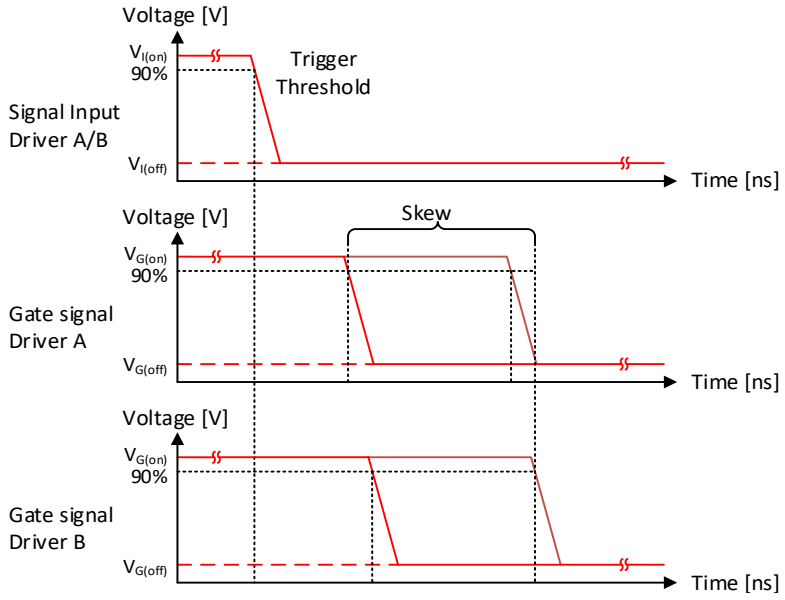


Figure 9.5.21 Definition of skew time

Both a short jitter time and a short skew time are significant for the parallel connection of modules with individual gate drivers.

9.5.4.3 Isolation barriers for energy and signal transmission

In less complex driver circuits such as used in low-cost applications these potential isolations may or have no electrical isolation with bootstrap circuits for TOP voltage supply and level shifter for signal transmission to the TOP switch), see explanations below. Low-voltage switches, especially those used in applications with low converter voltages or low-side choppers (only BOTTOM switch is active), require a very simple driver structure only, since individual driver functions can be easily implemented or even dispensed with (e.g. interlock and dead-time functions). In more demanding applications potential separation using inductive, capacitive or optical coupling is used.

The most important requirements applicable to potential isolation are sufficient static isolation strength (RMS 2.5...4.5... kV), as defined in the applicable standards; partial discharge test, if required) and sufficient application-specific dv/dt ruggedness (50...100kV/µs).
High dv/dt-ruggedness can be achieved by using small coupling capacitances (within 1…10pF range) between the primary and secondary sides of the potential isolation. This will minimise or even avoid control signal transmission interference caused by displacement currents during switching (Figure 9.5.22).

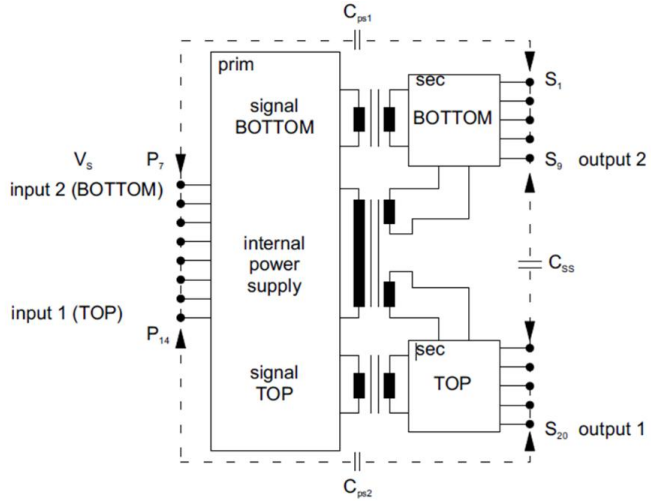


Figure 9.5.22 Equivalent coupling capacitances in a halfbridge driver with potential isolation

C_{ps1}: Effective capacitance between primary and BOTTOM secondary side
C_{ps2}: Effective capacitance between primary and TOP secondary side
C_{ss}: Effective capacitance between secondary sides TOP and BOTTOM

Transmission of driving energy: Potential-separated power supplies

In the majority of applications, driving energy is transmitted inductive (magnetic) with potential isolation or via "quasi"-potential isolation such as bootstrap circuits, see explanations below. The control unit of the DC/DC converter is located on the primary side of the driver circuit. Table 9.5.2 shows a comparison of common methods for energy potential separation with regard to important properties.

Potential separation	transformatory		none
System	Switched-mode power supply		Bootstrap circuit
Usually for power modules	≥ 1200V	≥ 1200V	up to 1200V
Supplied by	Aux. voltage + DC/DC converter	DC-link	Low-side operating voltage
Driver output voltage	positive and negative		only positive
Transmission frequency	very high (>500kHz)	medium	medium (pulse. fr.)
Duty cycle restrictions	no		yes
smoothing requirements	very low	low	low
Coupling capacitance	low	medium	low
HF Interference emission	high	low	none
Costs	medium	high	very low

Table 9.5.2 Comparison of common energy potential separation principles

A two-channel halfbridge gate driver requires two secondary side power supplies which are isolated from each other. These have to supply the positive and negative gate-emitter (gate-source) voltage or - for unipolar gate control - only a positive voltage.
The coupling capacitance C_{ss} between both secondary sides has to be as small as possible to avoid control signal transmission interference caused by displacement currents during switching. The power conversion is done by a high-frequency switched mode converter, e.g. as push-pull mode converter. In high power applications, the secondary voltages of some drivers are stabilised by linear voltage control. Some drivers offer the possibility to increase the possible output gate charge beyond the upper datasheet limit by means of external circuitry using boost capacitors.

Driving TOP-side transistors from the BOT driver channel

The Bootstrap topology enables cost-saving drive of TOP-side transistors, as it can be used to generate drive energy from the BOT-side driver channel without real potential separation.
Because of no galvanic insulation between TOP and BOT driver channel, the bootstrap topology is mainly used with 600/650V- or low power 1200V modules respective in monolithic HVIC drivers.
The principle behind a bootstrap circuit to supply energy to the TOP switch without "proper" potential isolation is depicted in Figure 9.5.23.

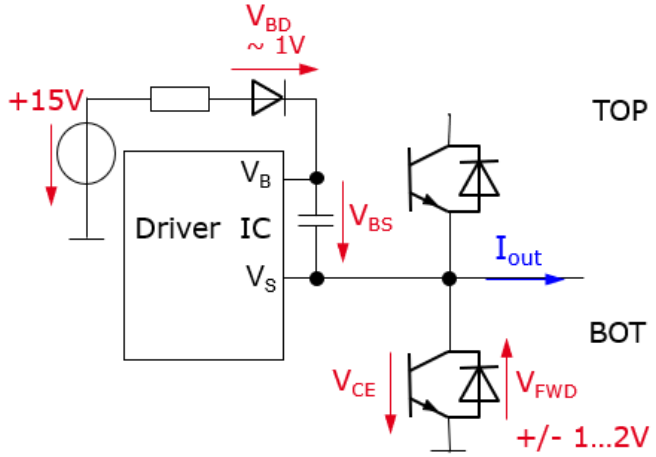


Figure 9.5.23 Bootstrap principle [9.48]

When BOT-IGBT is turned on, the V_S node is near ground potential (-DC). The Bootstrap diode is forward biased, and the bootstrap capacitor can be loaded up to V_{BS} as the powers supply of the driver IC for driving TOP-IGBT.
Before continuous operation, a Start-up regime is necessary. The bootstrap circuit can (only) generate positive supply voltage $V_{GE(on)}$ for the TOP switch. Other drawbacks are a minimum required switching frequency and duty cycle requirements (problems with very short OFF pulses for TOP-IGBT). $V_{GE(on)}$ for the TOP switch is not really constant, depends on output current level + direction (V_{BS} = 15V – V_{BD} + V_{FWD} = 15…16V at positive I_{out}; V_{BS} = 15V – V_{BD} - V_{CE} = 12…13V at negative I_{out}).

Transmission of control and feedback signals

Control signals are transmitted via optical or transformer (magnetic) potential isolation or via "quasi"-potential isolation such as level-shifters.
Table 9.5.3 shows a comparison of common methods regarding important properties.

Potential separation	**transformatory**	**optical**		**none**
System	Pulse transformer (magnetic core)	Optocoupler	Fibre optic	Level shifter
For power modules up to…	≥ 1200V	≤ 1200V	≥ 1700V	≤ 1200V
Transmission direction	bidirectional	unidirectional		
Duty cycle restrictions	low (no)	no	no	no
Temperature restrictions	$T_{ambient}$ < 130°C	T_a < 100…110°C	T_a < 100…110°C	T_a < 150…200°C
Coupling capacitance	5 … 20pF	1 … 5pF	< 1pF	> 20pF
dv/dt-immunity	high (50 … 100kV/µs)	lower	high	lower
Costs	medium	low to medium	high	low

Table 9.5.3 Comparison of common transmission principles for control signals

Digital signal transmission

In contrast to the "analogue" gate drivers described below, with the technically much more complex "digital" gate drivers the control signal is not edge-triggered but transmitted in the form of a pulse train via the isolation barrier's pulse transformer.
Therefore, a digital driver provides two independent signal channels communicating from low voltage to high voltage side to transfer switching and sensor signals. This approach ensures avoidance of temperature and aging effects, possible repetitive transmission of actual operating conditions (e.g. output current, temperature and DC-Link voltage feedback) for optimum control of the power transistors and high noise immunity.
An analogue-digital converter processes sensor signals and the digitised values can be transmitted potential-free as a serial data stream via the pulse transformer back to the primary side. Because events, error states and error data are stored in registers, a diagnosis is possible at a later stage. Semikron Danfoss has integrated digital gate drivers in its SKiiP 4 IPMs [3.20].

Level Shifter

Level shifter topologies enable cost-saving drive of TOP-side transistors, as they can be used to control signal from the BOT-side driver channel without real potential separation. Because of no galvanic insulation between TOP and BOT driver channel, such topologies mainly used with 600/650V- or low power 1200V modules respective in monolithic HVIC drivers.
Figure 9.5.24 shows a basic circuit diagram of a level-shifter, where the control signals for the TOP-IGBT are transmitted without galvanic isolation via a high-voltage switched current source.

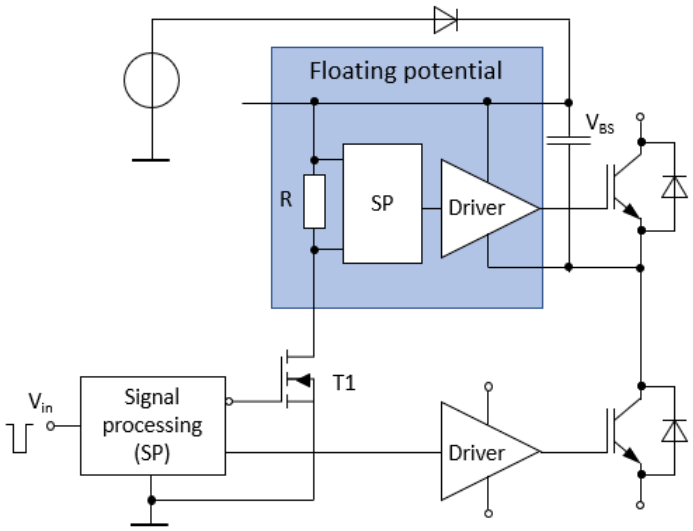


Figure 9.5.24 Basic circuit diagram of a level-shifter, (T1 high voltage small signal transistor, V_{BS} - voltage supplied by bootstrap capacitor, V_{in} controller signal)

The output signals of the low side signal processing unit switches T1 on and a current flow. The voltage drop across the resistor R is analysed in a high side signal processing unit (SP) that controls the TOP IGBT gate potential. Transistor T1 blocks the maximum voltage of the system, also cascodes (combination of low and high voltage FET) are used for that purpose. For voltages higher than 100V the losses might get to high for a permanent signal. In that case two channels transmitting the on and off edge of the control signal using a Flip-Flop circuit in the high side SP unit as a signal memory.

9.5.4.4 BOT and TOP gate driver output stages

Figure 9.5.25 shows four basic structures of a halfbridge gate driver output stage with bipolar gate control voltage for driving IGBT or MOSFET modules.

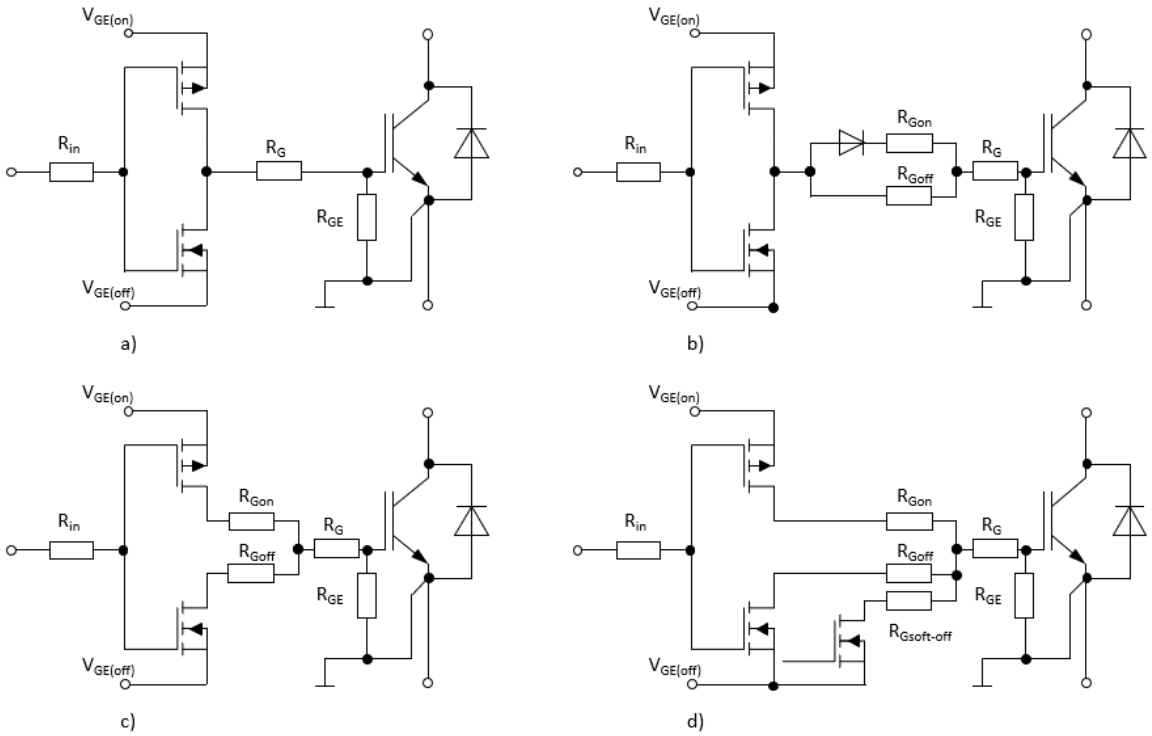


Figure 9.5.25 Driver output stages for bipolar gate control voltage: a) Minimum configuration: R_G selection for optimum turn-on behaviour (turn-off less dependent on R_G); b) Asymmetrical gate control by second resistor and series diode in parallel to gate resistor R_{Goff} for lower R_{Gon} (for lower R_{Goff}: opposite diode polarisation); c) Separate optimisation of turn-on and turn-off behaviour possible; d) Extended configuration with soft turn-off resistor circuit

Besides the complementary stage with low-power MOSFET (logic inverting push-pull output stage) or bipolar transistors also totem-pole drivers with MOSFET or bipolar transistors are commonly used. If only one driver output pin is available for R_G different R_G can be realised by paralleling R_{Gon} and R_{Goff} with a diode connected in series.
The gate-emitter resistance R_{GE} in the range of 10kΩ to 100kΩ should not be omitted in any application, since it prevents unintentional charging of the gate capacitance even in a case of missing driver power supply.

9.5.4.5 Error processing

To protect IGBT or SiC MOSFET modules in case of malfunction/error, gate drivers mostly include various efficient, fast-response protection functions, for example overcurrent and short circuit protection, protection from excessive drain-source or collector-emitter voltage, gate overvoltage protection, overtemperature protection and monitoring of the gate control voltages. In addition, there are several inputs for reacting to external events as well as outputs for transferring status information. The driver's reaction on internal and external events depends on the error mode, selected e.g. by connections of "programming pins".

Important quality criteria of the reaction to error messages are the response times of the error detection:

- Error propagation delay time $t_{d(err)}$: Time between the driver detects an error at the secondary side until the primary side reports an error at the interface.
- External error propagation delay time $t_{d(err,ext)}$: Time between the driver receives an external error signal at the primary side until the driver turns off its outputs at the secondary side.

For low-pass filters, pulse shapers and pulse-width-triggered flip-flops integrated into the signal transmission paths for interference suppression, their delay times must not only be able to accommodate the permissible minimum pulse duration but even the necessary response times in the event of malfunction/error.

With reference to Figure 9.5.18, the integration of protective functions on the gate driver's primary side as well as on its secondary side the driver is explained below.

DC converter control, Power-on reset

A power-on reset is essential for the avoidance of faulty actuation. The gate driver processes a Power-On-Reset after turning on the primary side supply voltage and blocks the power transistors for a time t_{POR}. The control is only enabled after this time, provided that no error is present.

Primary side shut down input

If a primary side shut down or error input is installed in the gate driver, it can be used optionally to report a system related external error event to the gate driver. Depending on the error mode configuration, the driver sets its outputs either immediately or with the next turn-off command at its corresponding input to low-level and locks them. A common wiring of the input is shown in Figure 9.5.26.

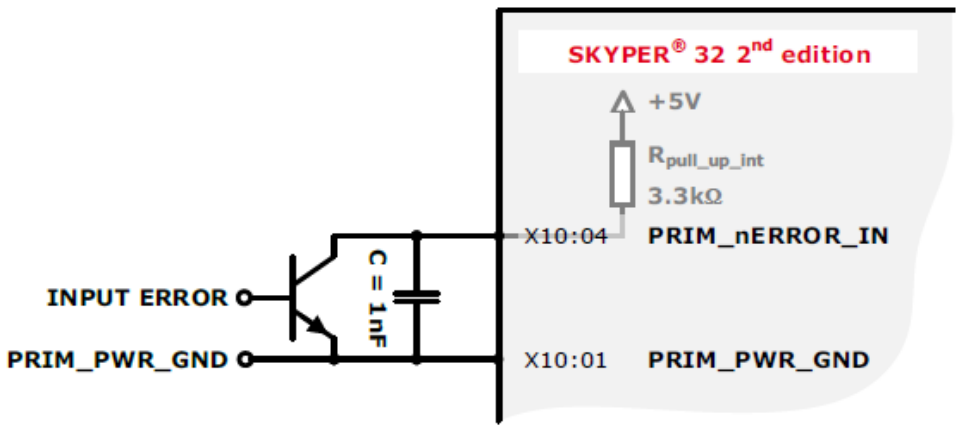


Figure 9.5.26 Connection of primary shut down input at Semikron Danfoss driver SKYPER 32 2nd edition [9.32]

In multiphase or parallel operation this input offers the possibility to force the outputs of each driver in the system to off-state and locks them, simultaneously, without the need of an external control unit. If there also a primary side error output is present, a low-active ERROR input can be connected to it to have a bidirectional error (HALT).

Primary side error output

Some drivers can report any detected error event at a specific pin by pulling it to low-level.
If this pin is an open collector output, that requires an external pull-up-resistor, see example in Figure 9.5.27. This gives the opportunity that, when error in- and outputs are connected together, multiple drivers can share one error line. In this case one driver, that enters error mode, directly switches of the parallel drivers.

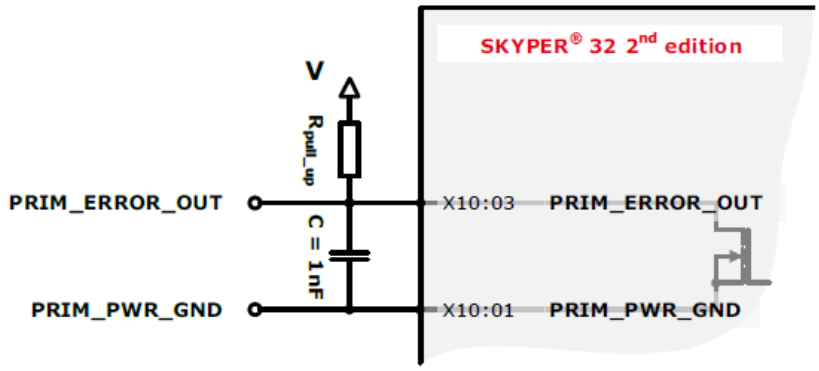


Figure 9.5.27 Connection of primary side error output (open collector error transistor) at Semikron Danfoss driver SKYPER 32 2nd edition [9.32]

Depending on the driver type, the error state will be active for at least 30µs or as long as the driver has not been reset the error output will be at low-level.

Primary side error mode selection, NPC mode input

Power transistors in multilevel NPC applications need a careful control, especially in error conditions like a short circuit. A dedicated three level turn-off sequence avoids damaging the semiconductors due to an unappropriated turn-off sequence. To realise a specific turn-off, sequence several drivers include a terminal to adapt the driver's error behaviour for driving multilevel stages. Via this terminal, it is possible to select between two reactions on error events:

- Immediate blocking of both outputs at the error event, until the error is reset. In the case of an error message on the primary side, the driver activates the standard turn-off path, whereas in the case of an error message on the secondary side, the driver activates the soft-off path (if available) of the affected secondary side. The IGBT on the other driver channel is switched off via the standard turn-off path. As long as the driver has not been reset the error event is reported at the corresponding output
- Immediate blocking of the output concerned. The other output is only disabled when the driver receives a turn-off command at the corresponding signal input. Depending on whether an error is detected on the primary or secondary side the driver activates the standard turn-off or the soft-off path, if available.

Detailed information related to the primary and secondary side error events, as well as on the error reset conditions is referred in [9.33] and [9.35]. For basic information, please refer chapter 9.6.

Primary side HALT logic signal processing

If the driver has terminals for the logic signals, it is possible to show and control the drive status via these terminals.
If the driver core is placed into HALT mode (disable driver), this signal can gather disable signals of other hardware components for stopping operation and switching off the IGBT. Switching pulses from the controller will be not transferred to the output stage. Figure 9.5.28 shows an application example.

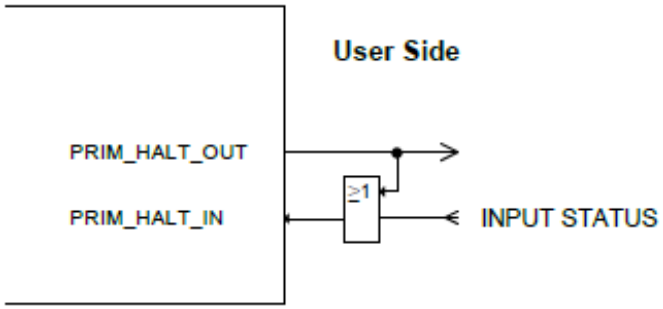


Figure 9.5.28 Connection of PRIM_HALT_OUT and PRIM_HALT_IN at Semikron Danfoss driver SKYPER 32Pro R [9.46]

Overtemperature lockout

Selected gate drivers offer an overtemperature lockout feature which sets both driver output stages to $V_{G(off)}$ and ignores the switching signals on primary side as long as the electrical resistance of the applied temperature sensor is less than the specified over temperature lockout resistance value (design for power module internal sensors with NTC resistor characteristic).
In addition to the locked outputs, the driver's primary side reports an error at the ERROPR_OUT terminal(s). This status is latched as long as the resistance of the temperature sensor is less than the specific resistance and both switching signals have not been set to low state for a specified minimum time initiating the error reset and allow resuming to normal operation.

Temperature monitoring and overtemperature protection

If an isolated temperature sensor is used, a temperature-equivalent signal may be transmitted to a primary side driver input. A threshold switch will set the error memory to ERROR as soon as a limiting value is exceeded.
Some drivers also include external error inputs on the secondary sides. Each secondary side of the driver can handle an external error event like overtemperature. The error events are evaluated and transmitted to the primary side.

Primary/Secondary side undervoltage lockout

Depending on the complexity of the driver, undervoltage monitoring is implemented also for the secondary side supply voltage, as sum detection or/and separately for positive and/or negative gate control voltage. With the "maximum" configuration, the driver permanently monitors the supply voltage of the primary side as well as both positive and both negative gate control voltages of the secondary sides. If either the supply voltage or one of the gate control voltages drops below the 'shutdown' threshold levels the driver enters into error state, its error memory is set to ERROR. The error condition resets when all these voltages have exceeded the 'non-error' threshold level. The driver will be ready again for operation, possibly only after reset.

9.5.4.6 Overcurrent/short circuit and overvoltage protection

Overcurrent- respective short circuit protection of power transistors is closely linked to their overvoltage protection. The higher the collector/drain current to be switched off at the same R_{Goff}, the more voltage is induced across the parasitic inductances in the load circuit. Overvoltage occurring due to periodic overcurrent must be limited by active protective measures in the gate driver that limit the collector current, see also chapter 9.6.
Non-periodic, excessive overvoltage, on the other hand, can also be limited at the main terminals of a power transistor. It can be performed by the transistor itself (e.g. avalanche-proof MOSFET), by passive networks or by an active gate clamping circuit, which implements a defined partial turn-on of the transistor in case of overvoltage.
The (over-) current information can be generated as an analogue signal, measured via shunt resistor, current sensor or chip-internal sense-cells and by evaluation of the voltage across the conducting transistor. The latter is the most used method, e.g. in the form of IGBT desaturation monitoring DCSP, see below.
Certain Semikron-Danfoss IGBT modules (SEMiX 3p shunt series) possess built-in shunt resistor for measuring the AC current, accessible via press-fit pins. This allows the footprint and main connections to remain identical to the standard module, while eliminating the need for current sensors [9.47].

The Semikron Danfoss SKiiP IPMs utilise internal potential-isolating, high-precision current sensors for measuring the AC current and overcurrent detection within the integrated driver (cf. chapter 3.2.7). The sensor's output signal may also serve as the actual AC-current value for control loops. As soon as such an error has been detected by comparing the actual value to a defined maximum current rating, an error memory is set (ERROR status) either on switch potential already or - in the case of potential-isolated sensors - in the primary circuit of the driver, which will block the power transistors until a RESET signal is triggered.
If the error memory is integrated on the secondary side of the gate driver, the error memory status signal will be transmitted to the primary side via the isolation barrier.

Dynamic short circuit protection by DESAT monitoring

In the predominant number of free-purchasable IGBT gate drivers, the short circuit monitoring is performed via monitoring of the on-state voltage drop across the power transistor. A comparator circuit is used to compare the on-state voltage, measured via a blocking diode, and a static reference voltage set by 1 or 2 external connected resistors as shown in Figure 9.5.29 for an IGBT driver (R1, R2). If the on-state voltage drop is too high an error is indicated, the protection circuit switches off the power transistor and an error message is reported to the primary side.

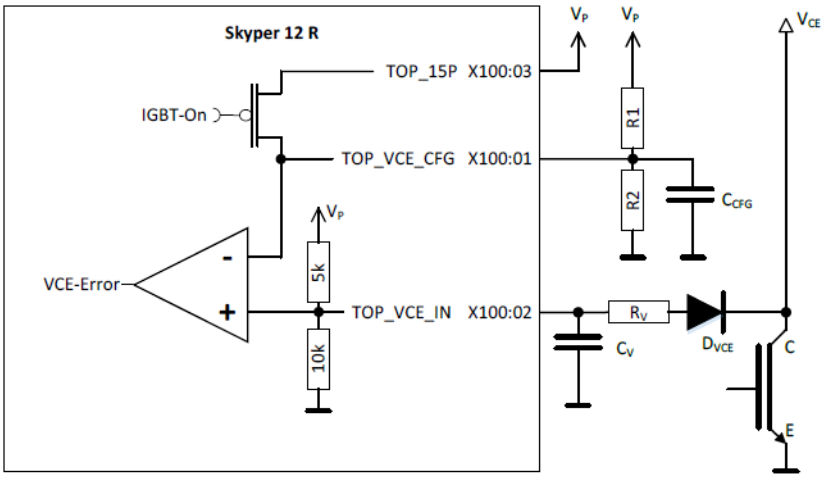


Figure 9.5.29 V_{CE} monitoring on the secondary side at Semikron Danfoss IGBT gate driver SKYPER 12 R (example for TOP secondary side) [9.34]

During the initial microseconds of the turn-on time, $V_{CEsatdyn}$ is far higher than its final value V_{CEsat}. For this reason, short circuit protection must be deactivated during transistor turn-on for a minimum blanking time t_{bl} (Figure 9.5.30). The IGBT protection circuit is called dynamic, because immediately after turn-on of the IGBT, a higher value is effective than in steady state. The time constant of the declining $V_{CE(ref)}$ is set by the capacitor C_{CFG} (see Figure 9.5.29).

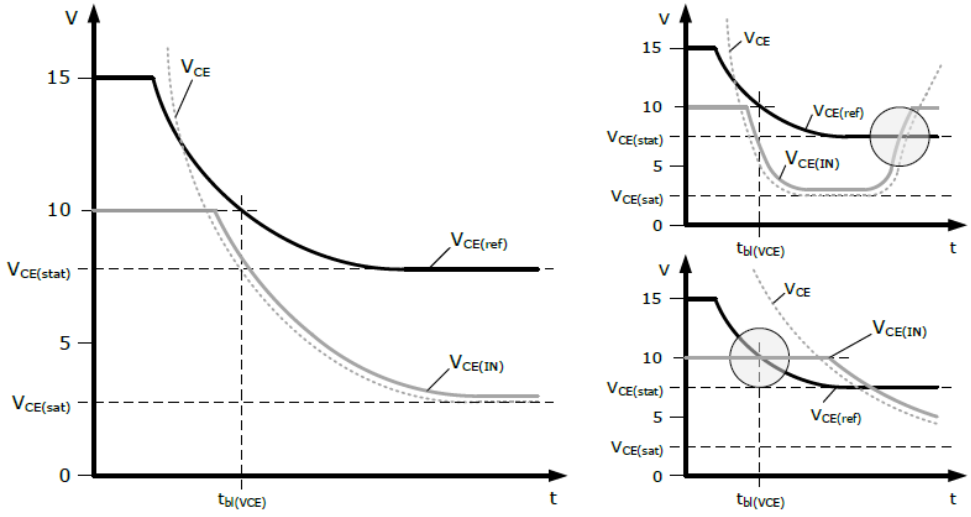


Figure 9.5.30 Dynamic saturation voltage characteristic of an IGBT and possible protection levels [9.27]

The blanking time must not exceed the IGBT maximum short circuit time t_{psc}, which is usually between 5µs and 10µs. Short circuit detection for a Si or SiC MOSFET can be performed via monitoring of the on-state voltage drop too, in a manner similar to that used with an IGBT. The blanking time can be set to a few 100ns, which is possible because V_{DS} drops very quickly. On the other hand, the steep voltage drop complicates the optimisation of the short circuit protection threshold and make noise-free measurements at chip level practically impossible with SiC MOSFET modules.
In contrast to IGBT chips, power dissipation during short circuit is produced almost entirely within the channel structure and only heats the surface of the chip, not the complete chip volume. Also SiC MOSFET chips are much smaller than an equivalent IGBT with a higher current density. Therefore, SiC MOSFET reach critical temperatures at shorter pulses. Some SiC MOSFET only allow short circuit durations of 2µs or less, while others are not capable of withstanding any short circuit. A drastic limitation of short circuit current I_{sc} by using a correspondingly low gate voltage would allow a long permissible short circuit time t_{psc}, but would increase the forward losses during normal operation. Additionally, the use of relatively high gate-source voltage to reduce on-state losses also yields very high currents in the event of a short circuit. It is therefore critical that any short circuit detection circuitry acts as fast as possible to give the best possible chance of device survival [9.30].

Protection from excessive collector-emitter (drain-source) voltage by active gate clamping

Non-periodical overvoltage during turn-off an overcurrent or caused by other transient voltage peaks can be limited by an active gate clamping network, see also the explanations in chapter 9.6.2.4. This option is already integrated in selected gate drivers. Figure 9.5.31 shows a topology, used by Semikron Danfoss. The voltage level where the clamping starts is set by the breakdown voltage $V_{avalanche}$ of the avalanche or suppressor diodes. If, during power transistor's turn-off, the v_{CE} (v_{DS}) raises beyond $V_{avalanche}$ the clamping diodes get conductive. This current switch the gate on again until v_{CE} (v_{DS}) is reduced below the $V_{avalanche}$ reference.
Also, during the active gate clamping process the IGBT or MOSFET is working in linear mode and is producing additional losses coming from the energy stored in the parasitic inductances. The clamping circuit has to work against the driver output stage, if the driver output is not switched-off. In that case are the avalanche diodes directly connected to the gate and it flows a high peak current through the clamping network (several amps) with simultaneously applied high voltage (e.g. 10A · 1100V = 11kW peak power). So active clamping must not work during standard switching to avoid thermal overstress. It should only be used in case of error. This makes a very careful voltage selection the clamping diodes necessary considering also the tolerances of such diodes. On the one hand $V_{CE(peak)}$ at turn-off at normal operation must be lower than $V_{avalanche}$ also at maximum DC-link voltage on the other hand should the voltage across the diodes lower than V_{CES} even at the high peak current via D_{Clmp} (e.g. of 10A). A series connection of clamping diodes is necessary to realise necessary isolation distances on the PCB.

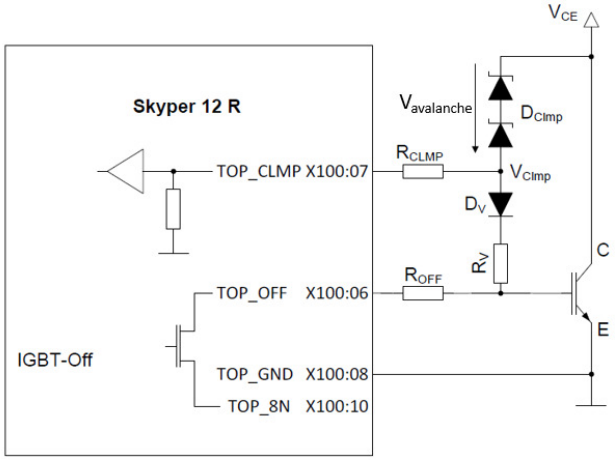


Figure 9.5.31 Application example for active gate clamping [9.34]

The *CLMP* input indicates the driver that the clamping is active so the driver output stage can be deactivated and losses on the driver can be reduced. The resistors R_{CLMP} and R_V have to be set, so that the input voltage on the clamping input raises above the threshold level during active clamping.

9.5.5 Properties of IGBT gate drivers by Semikron Danfoss

Semikron Danfoss IGBT gate drivers are available as hybrid or PCB-based plug-and-play drivers or driver cores for PCB integration.
Table 9.5.4 provides an overview about their properties. Not listed are the features that all drivers have in common, such as:

- 2 isolated driver channels drivers (except single channel drivers SKHI 10)
- Transformer energy transmission
- Transformer signal transmission (except SKYPER Prime O: optical signal transmission)
- Dynamic short circuit protection by DESAT monitoring (DCSP)
- Primary Side undervoltage lockout
- Reinforced insulation for signal and power transmission
- dv/dt resilience of 50kV/µs or 100kV/µs

Type Designation		Maximum values				Properties								
Gate driver class		V_{DC} [V]	$I_{outPEAK}$ [A]	Q_G [µC]	dv/dt [kV/µs]	Interlock time t_D [µs]	Coated or coated version available	SoftOff function	Active gate clamping	Secondary side undervoltage lockout	Primary side shutdown input	Primary side error output	Secondary side external error input	Primary side HALT logic signal processing
Driver Cores	SKHI21A R	1200	20	4	50	4.3	-	-	-	-	-	✔	-	-
	SKHI22A R	1200	20	4	50	4.3	-	-	-	-	-	✔	-	-
	SKHI22B R					0...4.3								
	SKYPER12 R	1200	20	20	50	0 or 2	-	✔	✔	✔	✔	✔	✔	-
	SKYPER12 PV R	1500							-					
	SKYPER32 R	1200	20	9	50	3	✔	-	-	-	✔	✔	-	-
	SKYPER32 PRO		15	6.3		0…4.3	✔	✔	-	✔	-	-	✔	✔
	SKYPER42 R	1200	30	50	100	2	✔	-	-	-	✔	✔	-	-
	SKYPER42 LJ R		24	20		0 or 2		✔	✔	✔			✔	-
	SKYPER42 LJ PV	1500	35	20		0 or 2								✔
Plug-and-Play Drivers	SKHI10/12 R	1200	8	9.6	75	-	-	✔	-	-	-	-	-	-
	SKHI10/17 R	1700												
	SKHI23/12 R	1200	8	4.8	75	0.9…10	-	✔	-	-	-	-	-	-
	SKHI23/17 R	1700												
	SKYPER12 PF	900	15	8	50	2	✔	✔	-	✔	✔	✔	-	-
		1200												
	SKYPER PRIME	900	15	10	50	4	-	✔	-	✔	✔	✔	-	-
		1200												
	SKYPER PRIME O	900	15	10	50	0	-	✔	-	✔	-	-	-	-
		1200												

Table 9.5.4 Main parameters of Semikron Danfoss IGBT gate drivers

Some gate drivers have some special features like a selectable input filter type with adjustable jitter and propagation delay times (SKYPER 12 R/PV R) and SKYPER 42 LJ R/LJ PV), a support of safe controlled short circuit turn-off strategies in multilevel topologies (SKYPER 42 LJ PV).
SKYPER 12 PF plug-and-play drivers have an overtemperature lockout with connected IGBT module internal temperature sensor.
The gate drivers SKYPER PRIME/SKYPER PRIME O enable PWM signal transmission to the primary side of the values for temperature and DC voltage on the IGBT module including a DC overvoltage trip threshold. These drivers are available able with gate resistors, alternatively suitable for Semikron Danfoss and selected competitor IGBT modules [9.37].

9.5.6 Special requirements for driving SiC MOSFET

9.5.6.1 Considerations

Essentially, the same requirements exist for the gate driver when driving SiC MOSFET as when driving IGBT with short switching times resp. higher frequencies. However, the utilisation of the switching properties of SiC MOSFET requires special attention/optimisation of the influence of parasitic circuit elements due to the high current transients and the narrow permissible gate voltage limits.
The high-speed switching transitions of SiC devices means that minimizing gate circuit inductance L_G is crucial. Otherwise, large gate resistors R_G are required to damp oscillations, see chapter 9.5.6.4 for explanations.

Recommendations derived from these for a SiC MOSFET Gate Driver Design are e.g.:

- Reduction of gate circuit inductance by a small loop area of the gate-source path between gate driver circuit and device (best achieved with a PCB-based design with coplanar traces: The source node is laid out on one layer as a larger plane. The gate signal is placed on the layer immediately above the source.
- If cables in the gate circuit are required: Use of twisted cables etc. for stray inductance of gate and source cables as small as possible
- Using a gate clamping circuit close to the SiC MOSFET module as described in chapter 9.6.3.2.

Other – application-dependent - considerations are:

- particularly low stray inductance
- low driver signal delay times
- low $V_{DS(desat)}$ detection propagation times
- blanking time suitable for high switching frequency
- interlock time suitable for high switching frequency
- driver output stage suitable for high switching frequencies
- highest dv/dt capability (isolation material and EMI immunity)
- small coupling inductances and EMC conform PCB layout (star like ground connections instead of long common tracks)

9.5.6.2 Gate voltage range for optimum switching performance

Today, there are no "Standard" for Gate Supply Voltage, but a supplier- and technology-dependent dynamic development with new chip generations. Especially the permissible range of the turn-off gate voltage is closely limited, with the limits depending largely on structural and technological details of the SiC MOSFET and depending on this, various wear problems, details see below.
Possible voltage peaks caused by e.g. high di/dt and dv/dt, ringing and oscillations (EMI, motor windings, …) or weak (small chip size) overload and short circuit capability also limit the maximum level of the turn- on and turn-off supply voltages.
The turn-on voltage, $V_{GS(on)}$, must be:

- Maximized (more positive) for low conduction losses (low $R_{DS(on)}$)
- Minimized for high short circuit capability (longer t_{psc}), see explanations below
- Minimized to avoid long term gate threshold voltage drift with consequential $R_{DS(on)}$ drift.

The turn-off voltage, $V_{GS(off)}$, must be:

- Maximized (more negative) to avoid parasitic turn-on during off-state
- Minimized (closer to 0V) to avoid long term gate threshold voltage ($V_{GS(th)}$) drift

Figure 9.5.32 illustrates the root causes of negative gate overvoltage spikes and parasitic turn-on of SiC MOSFET in a halfbridge topology.

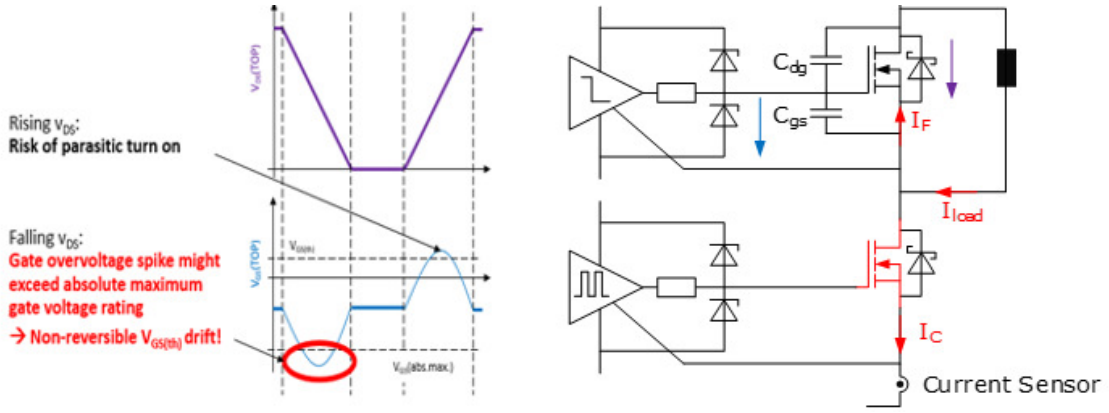


Figure 9.5.32 Root Cause of bidirectional gate overvoltage spikes on the TOP transistor when switching the BOT transistor

Negative gate overvoltage spike

Unfortunately, is a direct and undisturbed dynamic measurement of gate oxide voltage of the passive MOSFET during MOSFET turn off event not possible, because of voltage drops across which might compensate each other but a high uncertainty to which extend:

- chip internal gate resistance R_{Gint} (voltage drop is added to gate oxide voltage)
- common source inductance L_{cs} (voltage drop is subtracted from gate oxide voltage)
- Gate circuit self-inductances L_g (voltage drop is added to gate oxide voltage)

The negative voltage spike can be caused from oscillations after a snappy body diode turn of or by displacement currents across C_{DG} in the passive switch when the active switch turns-off and the voltage across the passive switch falls. A reasonably accurate estimation of gate overvoltage $V_{GS(peak)}$ for a certain configuration possible with simulation only, but a very rough indication of resulting negative gate overvoltage spikes is possible for the worst-case value of negligible gate currents by the formula:

$$V_{GS(peak)} = V_{GS(off)} - \frac{C_{rss}}{C_{iss}} \cdot V_{DC}$$

$V_{GS(off)}$: turn off voltage
C_{rss}, C_{iss}: small signal capacitances @ V_{DC}
V_{DC}: DC supply voltage (power circuit)

Positive gate overvoltage spike and parasitic turn-on

At high switching speeds with di/dt higher by a factor of 5 to 10 compared to IGBT modules, even smallest parasitic inductances inside the gate circuit may induce a gate-source voltage above the threshold voltage.
Since SiC MOSFET have a lower gate threshold voltage than current IGBT, there is also a higher risk of parasitic turn-on resulting. At high dv/dt, the impressed voltage can be estimated using the following formula:

$$\Delta V_{GS} = V_{DC} \cdot \frac{C_{rss}}{C_{iss} - C_{rss}}$$

Some more detailed information is contained, for example, in [9.39].

9.5.6.3 Gate voltage range for securing acceptable reliability

A SiC MOSFET typical characteristic is a low permissible limit of turn-off negative gate voltage $V_{GS(off)}$, typically in the range of -3V to -5V, because of the risk of gate oxide degradation, which causes threshold voltage instability. This instability includes short-term recoverable hysteresis and long-term permanent drift of $V_{GS(th)}$.
Switching SiC MOSFET with too large negative gate-source voltage can lead to gate threshold drift, resulting in a non-reversible increase in gate threshold voltage $V_{GS(th)}$ by gate oxide degradation. It results in an increase in drain-source on-resistance $R_{DS(on)}$ at a given gate-source voltage $V_{GS(on)}$.
The reliability determining switching-induced $V_{GS(th)}$ degradation is thus influenced by the:

- number of switching events, translating into switching frequency and total operation time
- driver's turn-off gate drive voltage $V_{GS(off)}$
- practically no measurable overshoot and undershoot of the gate-source pads directly at the chip

Beyond which limits gate degradation occurs is extremely dependent on the structure, technology and development status of the SiC MOSFET, which also results in the widely varying manufacturer specifications in the data sheets today. Some more detailed information is contained, for example, in [9.40], [9.41] and [9.42].

9.5.6.4 Impact of gate resistor selection

The switching behaviour is essentially affected by the resonant circuit of commutation inductance $L_{\sigma(commutate)}$ and output capacitance C_{oss} of the switching SiC MOSFET.

Oscillations with large amplitudes at frequency f_{osc}

$$f_{osc} = \frac{1}{2\pi \cdot \sqrt{L_{\sigma(commutate)} \cdot C_{oss}}}$$

cause EMI problems and overvoltage spikes. It can be reduced by means of lower commutation inductance or higher gate resistances values. The gate resistor does not damp the oscillation but with a lower dv/dt, the excitation of the oscillations is reduced. Figure 9.5.33 illustrates the turn-on and turn-off behaviour.

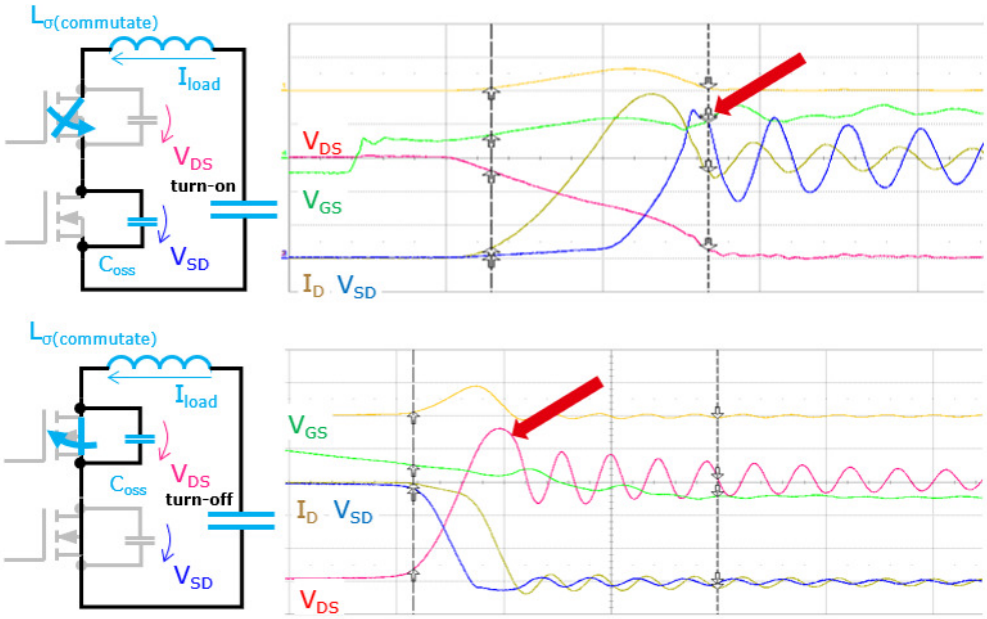


Figure 9.5.33 Influence of gate resistors at turn-on and turn-off

At TOP-side MOSFET's turn-on, the resonant charging of BOT-side MOSFET's C_{oss} induces an additional excitation of oscillations due the snappy behaviour of its body diode. The resulting overvoltage peak can achieve double the supply voltage level, depending on its gate resistance R_{Gon}. Otherwise, at turn-off the TOP-side transistor, its C_{oss} causes a "soft turn-off" like behaviour. The overvoltage is damped, depending on its gate resistance R_{Goff}.
Therefore, the selection of gate resistors must be carried out in such a way that oscillations in the power circuit are largely avoided.

9.5.6.5 Body diode's forward loss reduction by MOS-channel steering at MOSFET off-state

The SiC MOSFET's body diode becomes forward biased when the MOSFET is reverse biased. This diode behaves like a typical PIN diode, but with some added effects from the gate:
As the gate-source voltage is higher than zero volts, the channel begins to open resulting in a lower impedance path for bipolar current to flow. If the gate is fully turned-on during inverse diode conduction, the MOS-channel is open and takes over the current flow. Forward voltage drop is greatly reduced (Figure 9.5.34) to a similar resistive characteristic as in forward direction. In PWM inverter applications with inverted switching signals for TOP and BOT switches, this is anyhow the case. The necessary deadtime at the signal transitions should be as short as possible to minimize the time of current flow across the high body diode voltage drop. The deadtime losses are proportional to two time the switching frequency (during turn-on and turn-off) and can be considered as addition switching losses.

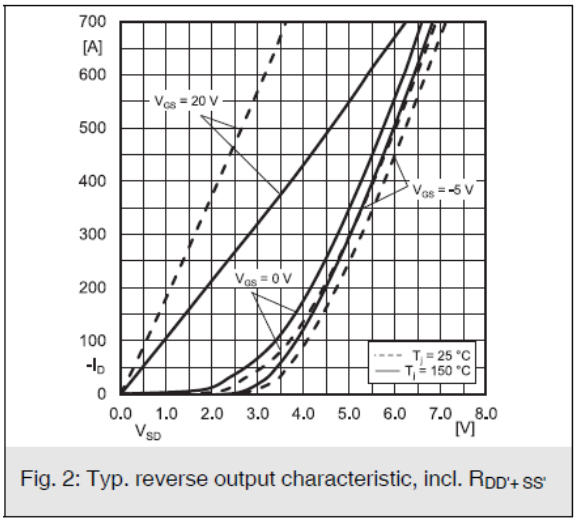


Figure 9.5.34 Influence of gate-source voltage on reverse conduction of a SiC MOSFET module SKM 350MB120SCH15 [9.26]

9.5.6.6 Body diode's switching speed maximising by deadtime optimisation

During the deadtime between the complementary gate signals of one phase leg, the body diode is conducting the load current in reverse direction at closed MOS-channel (Figure 9.5.35).

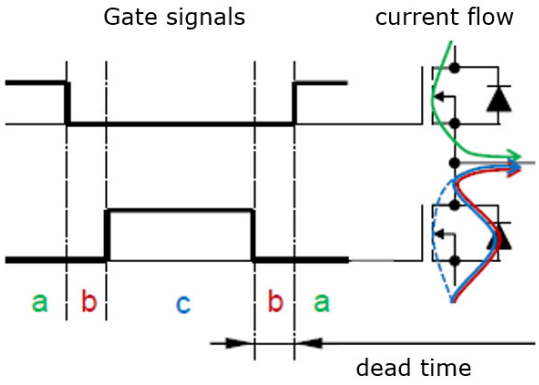


Figure 9.5.35 Current flow through TOP and BOT switch under consideration of the deadtime [9.44]

The length of the deadtime – adjusted by the gate-driver - affects the diodes dynamic behaviour. By reducing the deadtime, the reverse-recovery peak current value decreases, since the number of minority charge carriers in the body diode is reduced. This is resulting in lower diode turn-off and MOSFET turn-on losses. As reported in [9.44], a deadtime below 500ns reduces the body diode reverse recovery and the MOSFET turn on losses. However, if the time becomes too small the switching losses increase due to cross conduction losses.
A further effect is a reduced drop slope of the reverse recovery current after its peak. This results in less overshoot of the voltage across the body diode due to the stray inductances. Thus, it is possible to increase the turn-on speed for a further reduction of the MOSFET turn-on losses [9.43].
For a realistic inverter design it is necessary to consider the tolerances of the gate driver timing (skew, jitter etc.) and of the MOSFET switch itself (tolerances of delay and switching times etc.). A maximum spread of the resulting interlock time of ±100ns can be set as a realistic value.
More detailed information is contained, for example, in [9.42], [9.43], [9.44] and [9.45].

9.6 Behaviour in the event of a fault and protection

9.6.1 Types of faults/errors

Power semiconductors have to be protected from non-permissible stress in every operational state. Leaving SOAs leads to damage and, therefore, reduces component life. In the worst-case scenario, the component will be immediately destroyed. This is why it is important to detect critical states and faults and respond to them with suitable measures. The explanations in this chapter refer mainly to IGBT but may also be applied to power MOSFET Figure 9.6.1 classifies the three types of errors.

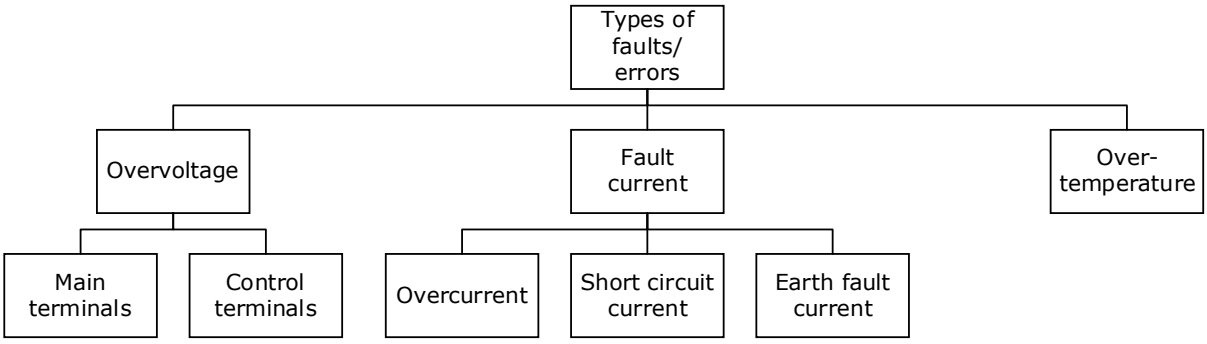


Figure 9.6.1 Classification of error types

Dangerous **overvoltage** occurs if the break-down voltages of power semiconductors are exceeded. This applies to both transistors and diodes. With respect to IGBT and MOSFET, overvoltage may occur between collector and emitter (or drain and source) - i.e. between the main terminals - as well as between gate and emitter (or gate and source) - i.e. between the control terminals.

Fault currents are collector / drain currents that exceed standard operating values of a certain application due to control or load errors.
They might lead to damage to the power semiconductors due to the following mechanisms:

- thermal destruction caused by high power dissipation (T_{jmax})
- dynamic avalanche due to too high current density (SCSOA)
- Aging of metallization (I_{CRM})
- static or dynamic latch-up
- Induced overvoltage after turn-off as a secondary effect ($V_{CE(BR)}$)

Dangerous **overtemperature** occur if the maximum junction temperature specified by the device manufacturer is exceeded (e.g. T_{jmax} = 150°C...175 °C for silicon devices).
During converter operation, overtemperatures might be generated by:

- an increase in energy dissipation caused by fault currents
- an increase in energy dissipation caused by defective drivers
- failure or malfunction of the cooling system

9.6.2 Overvoltage between main terminals

9.6.2.1 Causes

Figure 9.6.2 shows basic types of overvoltage between the main terminals of power semiconductors on the example of a commutation circuit.

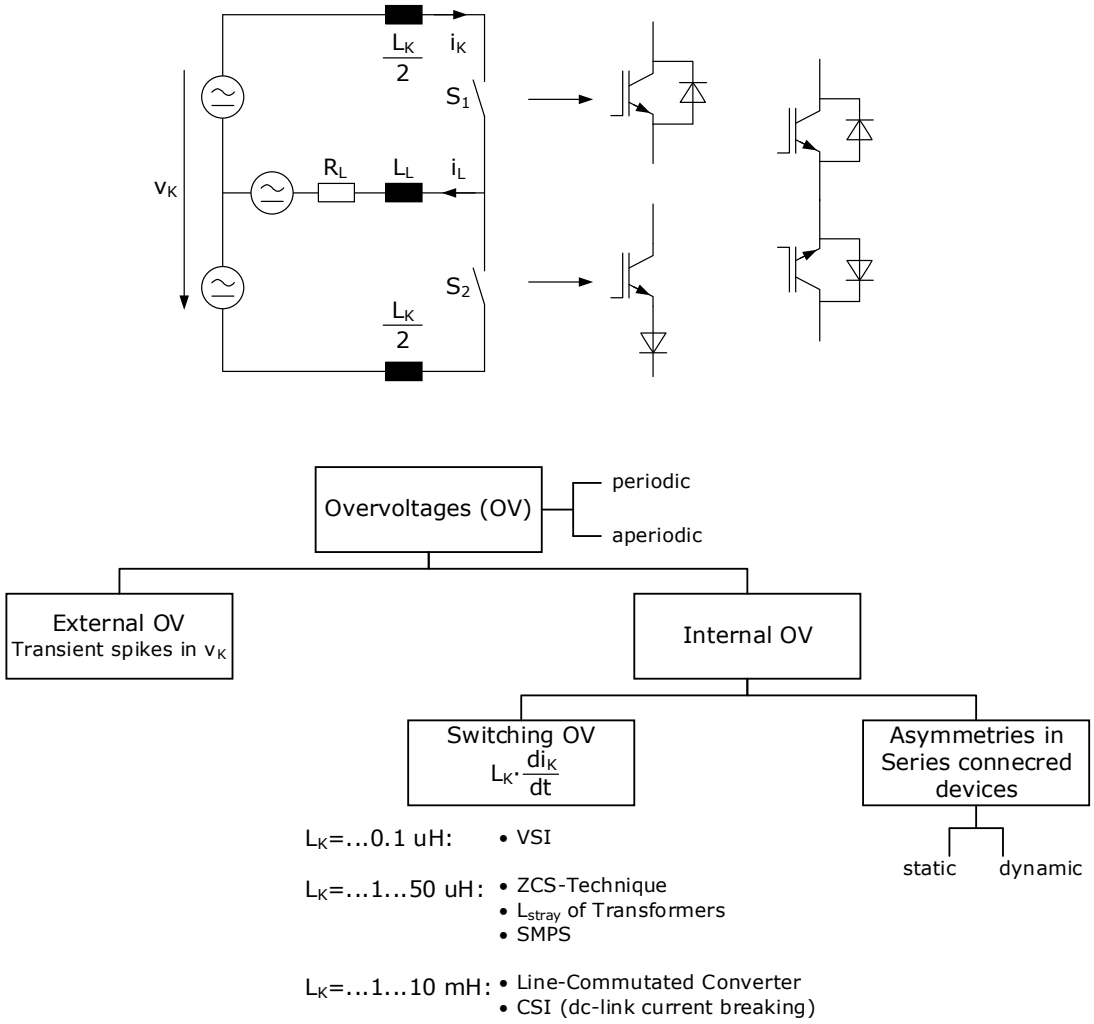


Figure 9.6.2 Types of overvoltage

Generally speaking, in commutation circuits a distinction is made between external and internal overvoltage. In connection with this, an "external overvoltage" is to be seen as a transient increase in the impressed commutation voltage v_K. This may happen, for example, in the DC voltage mains in electric traction power circuits or in any power supply system. Increased DC link voltages are to be seen in the same way (caused e.g. by active feedback loads or control errors in pulse rectifiers/active frontend).

"Internal overvoltage" $\Delta v = L_K \frac{di_K}{dt}$ are generated, for example, if the power electronic switch is turned off against the commutation circuit inductance L_K or if oscillations occur due to switching procedures. The following cases are typical examples of the generation of switching overvoltage:

- Active turn-off of load current i_L by the active elements of switches S1 and S2 during normal converter operation:
  In many SMPS applications (Switch-Mode Power Supply), the inductance L_K is generated as a result of the stray inductance of transformers, which may be as much as 1…100µH.
- Reverse recovery di/dt during passive turn-off of fast diodes in hard switching converters or ZCS converters:
  Owing to their operating principle, ZCS converters may also show an increased commutation inductance within the range of 10µH (cf. chapter 9.8).
- High di/dt (...10kA/µs...) in the event of short circuits and during turn-off of short circuit currents in converters with DC voltage link
- Active interruption of DC link currents in CSI topologies (failure)

Furthermore, overvoltage in power electronic devices may be generated by static or dynamic asymmetries in switches connected in series (cf. chapter 9.4). Overvoltage during normal operation of converters and converter fault operation may appear as periodic (...Hz...kHz...) or aperiodic overvoltage.

9.6.2.2 Overvoltage limitation between main terminals

First measure is always the reduction of the commutation (stray) inductance by

- using low inductive capacitors,
- parallel connection of capacitors
- use laminated busbar systems or wide area layers on PCB with +DC and -DC on top of each other between capacitor and power semiconductor
- avoid narrow tracks for the current flow
- avoid changes in the current flow direction

If this is not sufficient additional measures to limit overvoltage between main terminals (collector-emitter voltage, DC link voltage) are necessary, which can be divided into passive snubber-networks, active clamping and dynamic gate control.
Irrespective of the type of overvoltage limitation, the avalanche operation mode of MOSFET can be utilised, if applicable. The limiting values given in the datasheets must be strictly adhered to. In addition, the suitability of avalanche operation for the intended application should be confirmed by the manufacturer.

9.6.2.3 Overvoltage limitation between main terminals by passive snubber networks

Passive networks (snubbers) are combinations of passive elements such as R, L, C, suppressor diodes, diodes, varistors etc. Figure 9.6.3 shows basic and frequently used circuits.

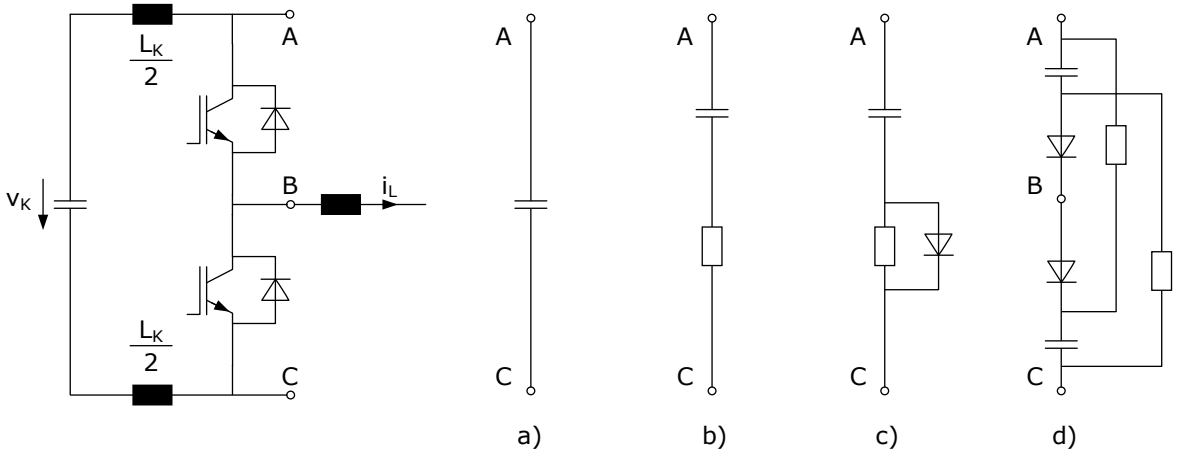
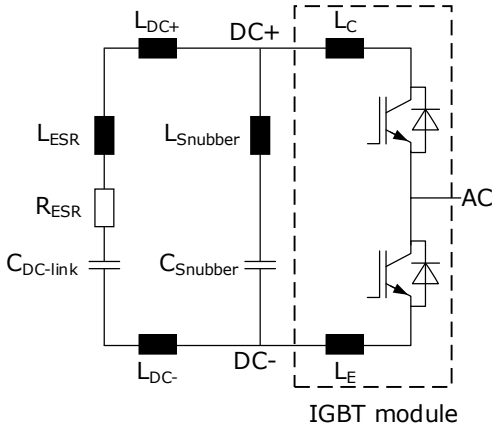


Figure 9.6.3 Passive overvoltage limitation networks (snubbers)

Passive snubber networks prevent dangerous overvoltage from being induced by the inductances of the commutation circuit L_K by attaching a capacitor which absorbs the energy $E = \frac{L_K}{2} i^2$ stored in L_K.
To ensure that the circuit continues to work effectively, the absorbed energy has to be discharged again between two charging processes. With simple snubbers, this task is performed by heat conversion in the snubber resistors or by feedback to the DC link capacitor.
The simplest method is to clamp the DC link voltage directly to the power module terminals by means of a capacitor (such as a film capacitor). This measure is sufficient for many VSI applications. In this case, the capacitance value lies in the region of 0.1...2µF (Figure 9.6.3 a).

- The following parameters must be considered when dimensioning the capacitor:
- DC voltage class of the capacitor (e.g. 1000V, 1250V, 1600V)
- Capacitance and minimum parasitic internal inductance
- Pulse current capability
- Effective capacitor voltage and current (power losses!)
- Service life

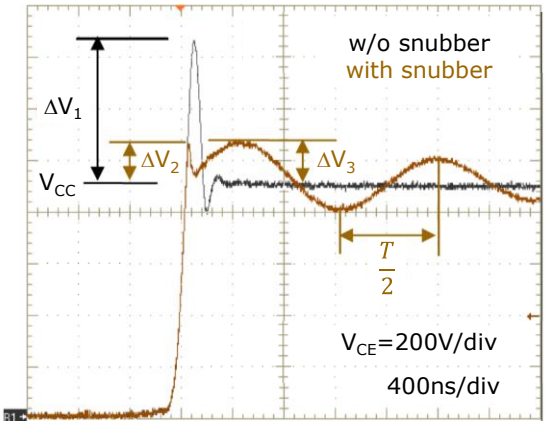
Figure 9.6.4 shows a simplified equivalent DC link circuit with typical, concentrated parasitic inductances.



DC+, DC-, AC	IGBT module terminals
L_C, L_E	IGBT module collector and emitter parasitic inductance
L_{DC+}, L_{DC-}	Bus bar parasitic inductance
$C_{snubber}$	Snubber capacitor capacitance
$L_{snubber}$	Snubber capacitor series inductance
$C_{DC-link}$	DC-link capacitor capacitance
L_{ESR}	DC-link capacitor series inductance
R_{ESR}	DC-link capacitor series resistance

Figure 9.6.4 Simplified equivalent DC link circuit with typical, concentrated parasitic inductances

Figure 9.6.5 shows the typical voltage characteristics of an IGBT turn-off process with and without snubber and compiles simplified equations for dimensioning the snubber circuit. Further technical information is provided in [9.3].



$$\Delta V_1 = \sum L \frac{di_C}{dt}$$

$$\sum L = L_C + L_E + L_{DC+} + L_{DC-} + L_{ESR}$$

$$L_{DC-link} = L_{DC+} + L_{DC-} + L_{ESR}$$

$$\Delta V_2 = (L_C + L_E + L_{Snubber}) \frac{di_C}{dt}$$

$$\Delta V_2 \leq \sqrt{\frac{L_{DC-link} \cdot i_C^2}{C_{Snubber}}}$$

$$f_{OSC} = \frac{1}{T} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{DC-link} \cdot C_{Snubber}}}$$

Figure 9.6.5 IGBT turn-off process: typical voltage characteristics with and without snubber; simplified equations for snubber circuit dimensioning

Figure 9.6.6 shows two different versions of snubbers that are mounted to the DC terminals of a 3-level TNPC in a SEMiX 5 package. On the left side, two capacitors are housed in series in one housing. On the right side, two individual capacitors are used. For these two embodiments, overvoltage measurements have been carried out and compared.

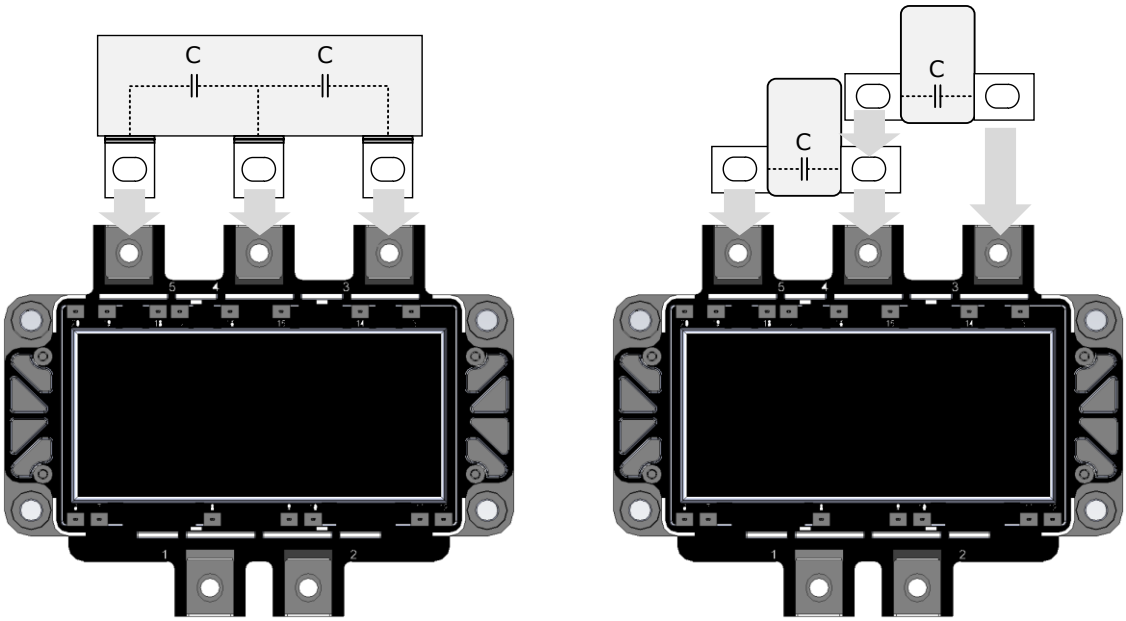


Figure 9.6.6 Two embodiments of snubbers on a 3-level TNPC in the SEMiX 5 package

Figure 9.6.7 and Figure 9.6.8 show the overvoltage measurements at the turn-off moment of the IGBT and the diode of the TNPC in the SEMiX 5. The design with two individual snubbers (b) can significantly reduce the overvoltage at the IGBT and the diode. This is an example of how snubbers should be placed as close as possible (low-inductive) to the module's terminals.

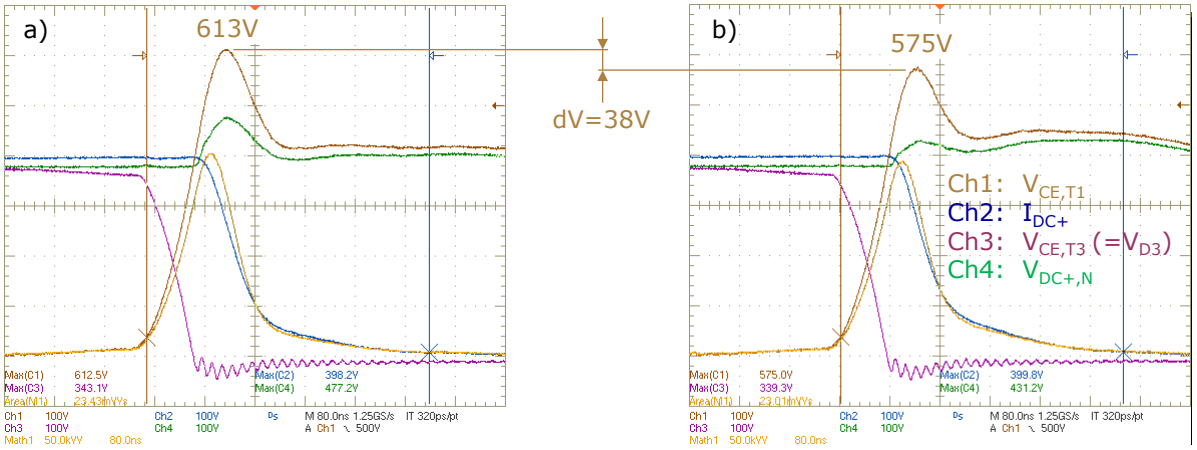


Figure 9.6.7 overvoltage measurement at T1 of a TNPC at turn-off moment

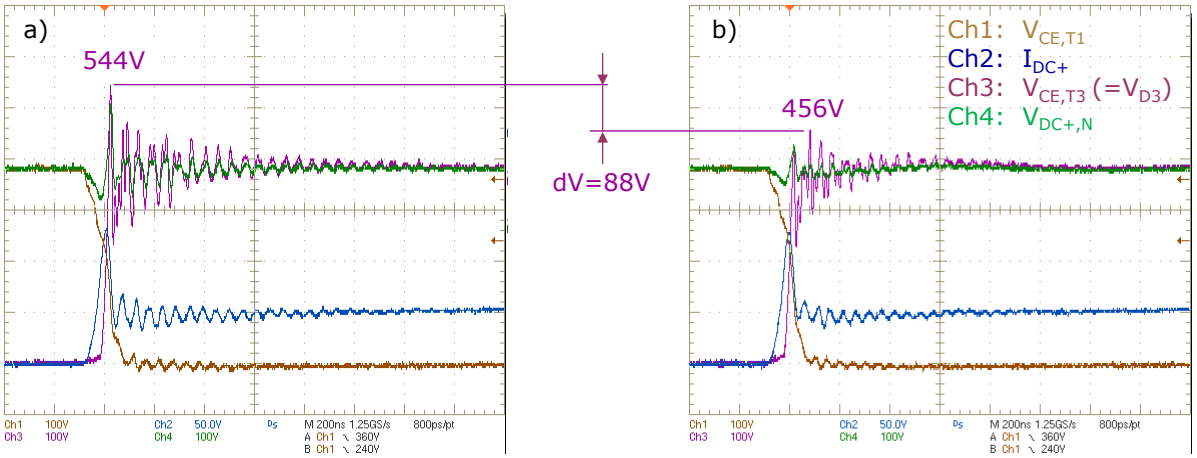


Figure 9.6.8 overvoltage measurement at D3 of a TNPC IGBT module

To absorb parasitic oscillations between C and L, voltage clamping may be implemented using an RC element (Figure 9.6.3 b). This measure is often taken for low-voltage / high-current applications (e.g. MOSFET converters) to avoid parasitic oscillations in the DC link voltage at the module terminals when switching high currents.
Figure 9.6.3 c) and d) show RCD networks. The integrated fast diodes should display low forward turn-on overvoltage and soft reverse-recovery behaviour. The design of the snubber network itself and the power module terminals (A,B,C) must be as low-inductive as possible. An advantage of passive networks besides their simple topologies is that they do not require active components. A disadvantage of this, however, is that the overvoltage limit value varies depending on the operating point of the converter. For this reason, dimensioning has to be based on the worst case scenario (overcurrent, short circuit, high di/dt).

9.6.2.4 Overvoltage limitation between main terminals by Active Clamping

Active clamping of MOS-controlled transistors refers to direct feedback of the collector / drain potential to the gate via a Zener element. Figure 9.6.9 shows the basic principle and variants produced with the example of an IGBT-switch. Other embodiments of the clamping network are not covered here.

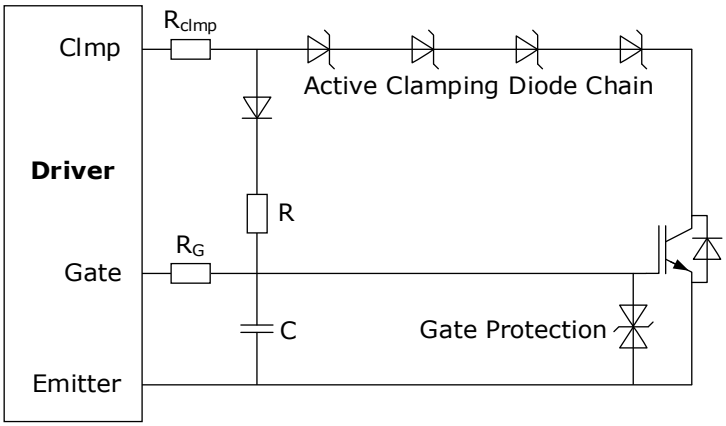


Figure 9.6.9 Basic principle of Active Clamping with Zener diodes

Active clamping is intended to protect the IGBT from excessive voltage peaks. However, it must not increase the losses of the IGBT in normal operation by tripping the clamping diodes. Active clamping is usually done by connecting suppressor diodes in series. The type of diodes and the number of diodes connected in series depend on the following factors:

- Level of protection to be achieved
- Voltage limitation at the diode due to the creepage distance on the PCB
- Peak current and power losses on diodes

The suppressor diodes trigger quickly, which can lead to vibrations at the gate. To dampen these vibrations, a resistor R and a capacitor C can be used at the gate. The resistance value is usually a few ohms and has no influence on the protection level. The Clmp input on the driver detects active clamping.
Figure 9.6.10 shows measurements of the losses and peak voltage on a 650V IGBT in the horizontal branch of a TNPC with three different combinations of clamping diode chains. The full DC link voltage is 900V. The commutation voltage corresponds to half the DC link voltage and thus 450V. The maximum turn-off current is 350A.

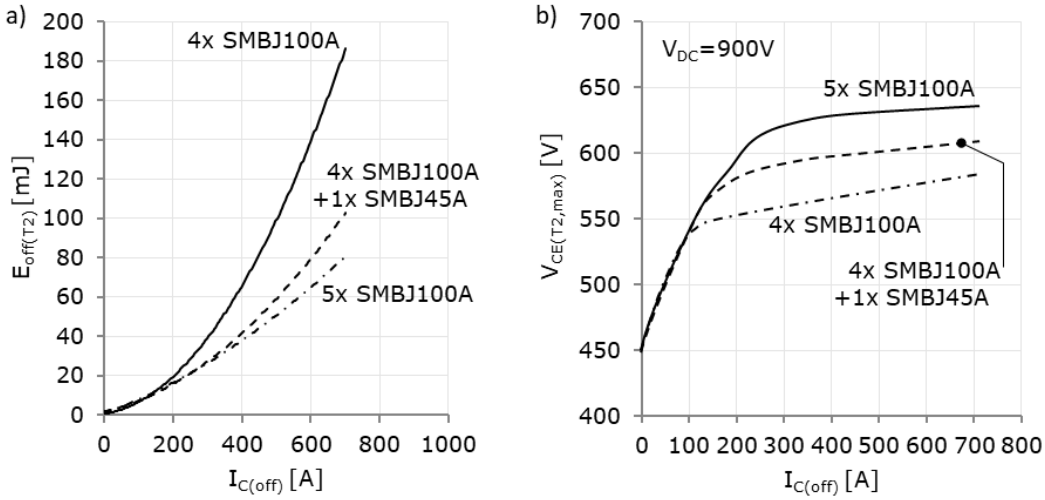


Figure 9.6.10 a) Turn-off power dissipation for different variants of the diode chain; b) Maximum overvoltage for different variants of the diode chain

The measurement of 5x SMBJ100A shows that the maximum voltage is V_{CEmax}=640V.
This means 128 V per diode. It can be seen that the overvoltage increases with the turn-off current, i.e. with the energy that has to be dissipated.

ELECTRICAL CHARACTERISTICS @ 25°C

MICROSEMI PART NUMBER		REVERSE STAND-OFF VOLTAGE V_{WM}	BREAKDOWN VOLTAGE $V_{(BR)}$ @ $I_{(BR)}$ Volts		MAXIMUM CLAMPING VOLTAGE @ I_{PP}	PEAK PULSE CURRENT (See Fig. 2) I_{PP}	MAXIMUM STANDBY CURRENT @ V_{WM} I_D µA
GULL-WING LEAD	MODIFIED "J" BEND LEAD	Volts	MIN. MAX.	$I_{(BR)}$ mA	Volts	Amps	
SMBG45A	SMBJ45A	45	50.0 – 55.3	1	72.7	8.3	1
SMBG100A	SMBJ100A	100	111 – 123	1	162	3.7	1

SYMBOLS & DEFINITIONS

Symbol	Definition	Symbol	Definition
V_{WM}	Working Peak (Standoff) Voltage	I_{PP}	Peak Pulse Current
P_{PP}	Peak Pulse Power	V_C	Clamping Voltage
$V_{(BR)}$	Breakdown Voltage	$I_{(BR)}$	Breakdown Current for $V_{(BR)}$
I_D	Standby Current		

Figure 9.6.11 Datasheet SMBJ45A/SMBJ100A [9.49]

The name of the suppressor diode differs from the actual protection level.
The datasheet according to Figure 9.6.11 shows that the diode voltage for SMBJ100A at V_{RWM}=100V at I_D=1µA and $V_{(BR)}$=111-123V at $I_{(BR)}$=1mA. At I_{PP}=3.7A, the maximum diode voltage is 162V. So, the level of protection depends on the current that flows through the diode chain and into the driver stage to charge the gate (see Figure 9.6.12). Furthermore, the temperature dependence and the type spread must be taken into account. To do this, it is necessary to measure the actual characteristic curve of the diode and compare it with the data sheet. Subsequently, tests must be carried out with suppressor diodes that cover the entire scattering range.

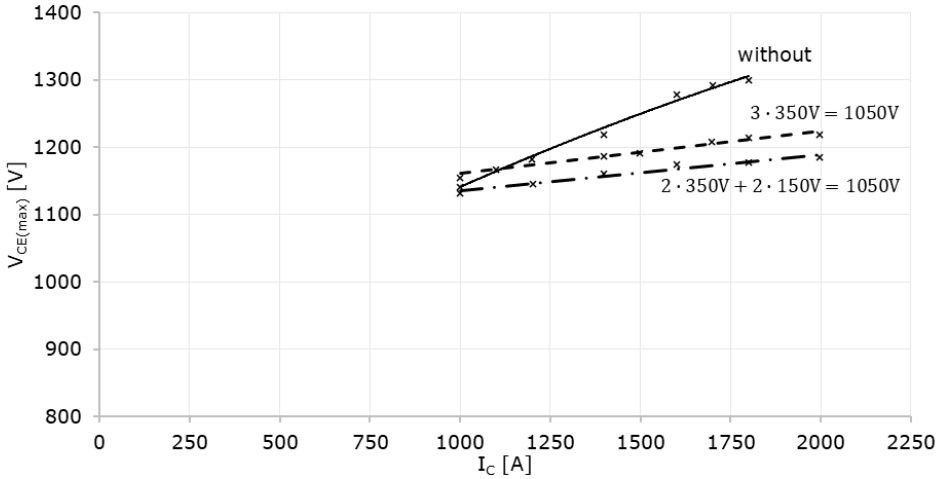


Figure 9.6.12 Turn-off overvoltage from double nominal current up to short circuit current for a 1200V IGBT for two different selection of diodes voltages in comparison to turn-off without clamping circuit.

Active clamping involves the following features:

- simple circuit arrangement
- the transistor to be protected is part of the protection itself and converts the main share of energy stored in the inductance during the clamping process
- there is no need for power resistors and snubber capacitors
- steep clamping characteristic
- the switch voltage to be limited does not depend on the operating point of the converter
- no separate power supply is needed
- conventional drivers may be used
- overvoltage during reverse-recovery di/dt of the inverse diodes are limited inherently
- option to equip either every single transistor switch with a clamping circuit or to attach one central clamper for one or several pairs of switches

The principle of active clamping is applicable to both aperiodic (e.g. short circuit turn-off) and periodic (e.g. in certain ZCS-topologies) clamping processes and has to be dimensioned accordingly

9.6.2.5 Overvoltage limitation between main terminals by dynamic gate control

In the process of dynamic gate control, the di/dt and dv/dt of MOSFET and IGBT and the resultant induced overvoltage is directly determined by the driver.

Simple dynamic gate control includes soft turn-off of IGBT and MOSFET in the event of overcurrent or short circuit; soft turn-off here is achieved either by applying higher gate series resistances (e.g. driver SKHI 23, SKYPER 52) or by implementing turn-off with a defined small gate current (current source control).
In more complex driver circuits, the gate series resistors are switched consecutively even during standard-mode converter operation in order to optimise switching times, switching losses and switching overvoltage (e.g. "intelligent turn-off" function in the Semikron-Danfoss SKYPER 52 driver).

9.6.3 Overvoltage limitation between control terminals

9.6.3.1 Causes

Overvoltage between control terminals of IGBT and MOSFET can be due to:

- supply voltage error in the driver stage
- dv/dt feedback (displacement current to the gate) via Miller capacitance (e.g. SC II),
- emitter / source di/dt feedback,
- increase in gate voltage during active clamping (cf chapter 9.6.2.4)
- parasitic oscillations in the gate circuit (e.g. connection to collector/drain, transient oscillations between gate circuits of paralleled transistors etc.).

9.6.3.2 Overvoltage limitation between control terminals by gate voltage clamping

Overvoltage limitation between control terminals is required to maintain the maximum gate-emitter / gate-source voltage, on the one hand, and limit the dynamic short circuit current amplitude, on the other hand.
Charge carrier storage effects can increase the gate voltage above the supply voltage in case of a short circuit. This charge should be dissipated via a low-impedance path, which can alternatively be realised by a suppressor diode between gate and emitter Table 9.6.1 a) or a Schottky diode with low-impedance connection to a capacitor of the power supply Table 9.6.1 b).
The use of fast Schottky diodes to clamp the gate voltage to the driver supply voltages has proven particularly efficient in switching applications.
Dynamic Gate overvoltage spikes can be limited by a gate clamp circuit, low-inductive placed close to the module gate connection. The Schottky diodes D1 and D2 in Table 9.6.1 c) providing a return path to the negative and positive voltage rails for transient voltage spikes.
Because the overvoltage-sensitive SiC MOSFET are operated very close to critical gate-source voltage limits, gate clamping measures are recommended in any case.

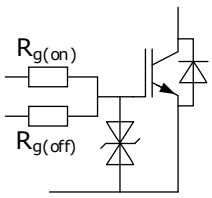
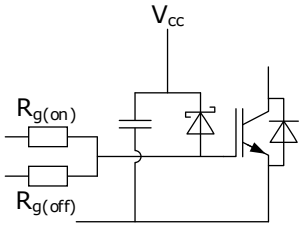
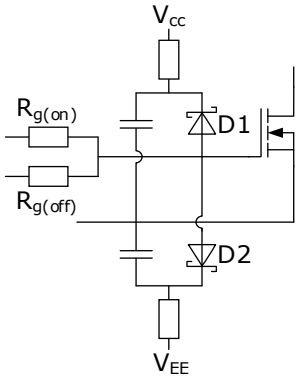
Zener Diode	Schottky Diode (unidirectional)	Schottky Diode (bidirectional)
		

Table 9.6.1 Simple passive gate voltage limitation circuits (passive gate clamping)

By limiting the gate voltage, the collector or drain current is limited, also because the gate voltage is no longer greatly increased by the current across the miller capacitance. During the clamping process the IGBT or MOSFET is working in linear mode and is producing additional losses coming from the energy stored in the parasitic inductances. So, clamping measures must not work during standard switching to avoid thermal overstress and reduced the transistor's lifetime. It should only be used in case of error.

In contrast to the protection functions described so far, the gate protection might have to limit the gate voltage periodically without the presence of an actual error that would require the power transistors to be turned off. For this reason, there is no connection to the error memory.

9.6.4 Overcurrent

9.6.4.1 Causes

Overcurrent is usually characterized by relatively low rates of rise of the collector current. The slew rates depend on the load inductance and the driving voltage. The fault current flows through the DC Link, whereby the transistor does not desaturate. Potential causes include a reduction in load impedance and errors in the converter control and regulation.
Essentially, the switching and on-state behaviour under overload does not differ from "standard operation" under rated conditions. In order not to exceed the maximum junction temperature and to ensure safe operation, the overload range has to be restricted, since increased load current may cause increased power dissipation in the device or destruction of components such as diodes due to dynamic failure mode effects.
Here, limits are set by the absolute value of the junction temperature as well as by overload temperature cycles. These limits are specified in the datasheet SOA diagrams (Safe Operating Area). Figure 9.6.13 shows the example of an IGBT.

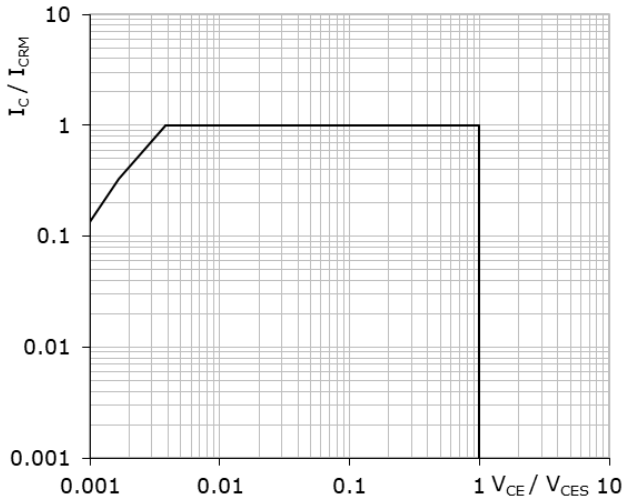


Figure 9.6.13 SOA-diagram of an IGBT

9.6.5 Short circuit current

Short circuit currents are characterized, among other things, by very high rise rates of the collector current di/dt and a multiple of the nominal component current. In this case, the fault current flows through the DC link and the transistor located in the short circuit path desaturates.
Based on the cases shown in Figure 9.6.14, two can be assigned to the short circuit. The branch short circuit, marked as Case 1, can be explained by a defective switch or incorrect control of the switch by the driver. The load short, marked as Case 2, can be caused by an insulation fault or incorrect installation.

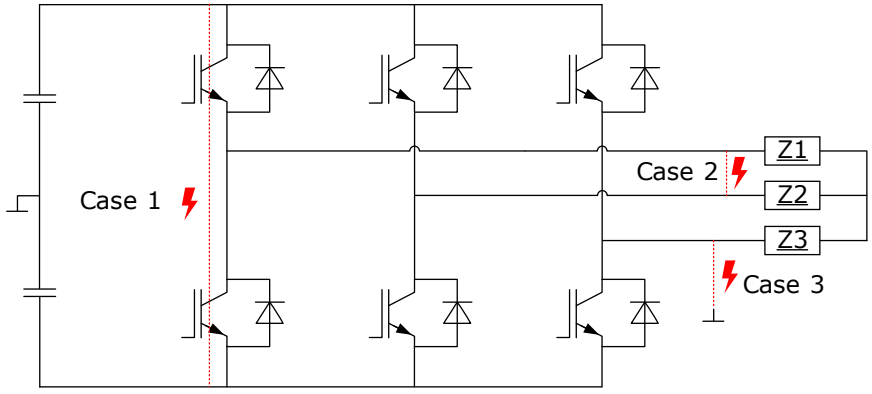


Figure 9.6.14 Causes of fault currents

Essentially, IGBT and MOSFET are short circuit proof, i.e. they may be subjected to short circuits under certain given conditions and actively turn these off without damaging the power semiconductors. Two different types of short circuit must be distinguished between (on the example of an IGBT).

9.6.5.1 Short circuit I

With short circuit 1 (SC I), the transistor is turned on when a load or bridge short circuit already exists, i.e. the full DC link voltage is applied to the transistor before the short circuit even occurs. The di/dt of the short circuit current is determined by the driver parameters (driver voltage, gate resistor) and the transfer characteristic of the transistor. This transistor current increase will induce a voltage drop over the parasitic inductance of the short circuit, which is manifest as a decrease in the collector-emitter voltage characteristic (Figure 9.6.15).

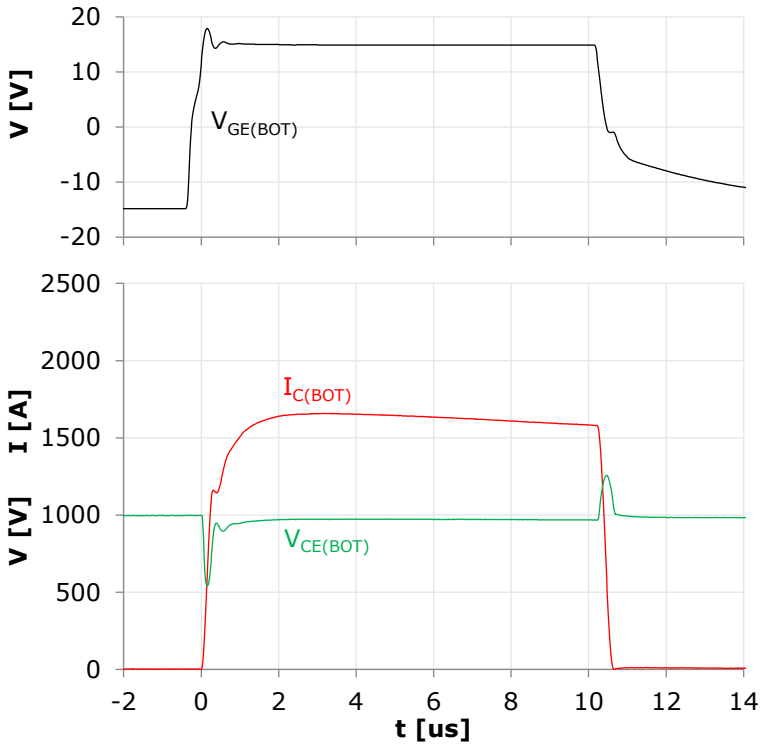


Figure 9.6.15 SC I characteristics of an IGBT

The static short circuit current adjusts itself to a value determined by the output characteristic of the transistor. Typical values for IGBT of different technologies are as much as 6...10 fold the rated current (cf. Figure 9.6.18 b).

9.6.5.2 Short circuit II

In this case, the transistor is already turned on before the short circuit occurs. Compared to SC I, this case is much more critical with respect to transistor stress.
Figure 9.6.16 shows an equivalent circuit and principal characteristic to explain the short circuit II (SC II) procedures.

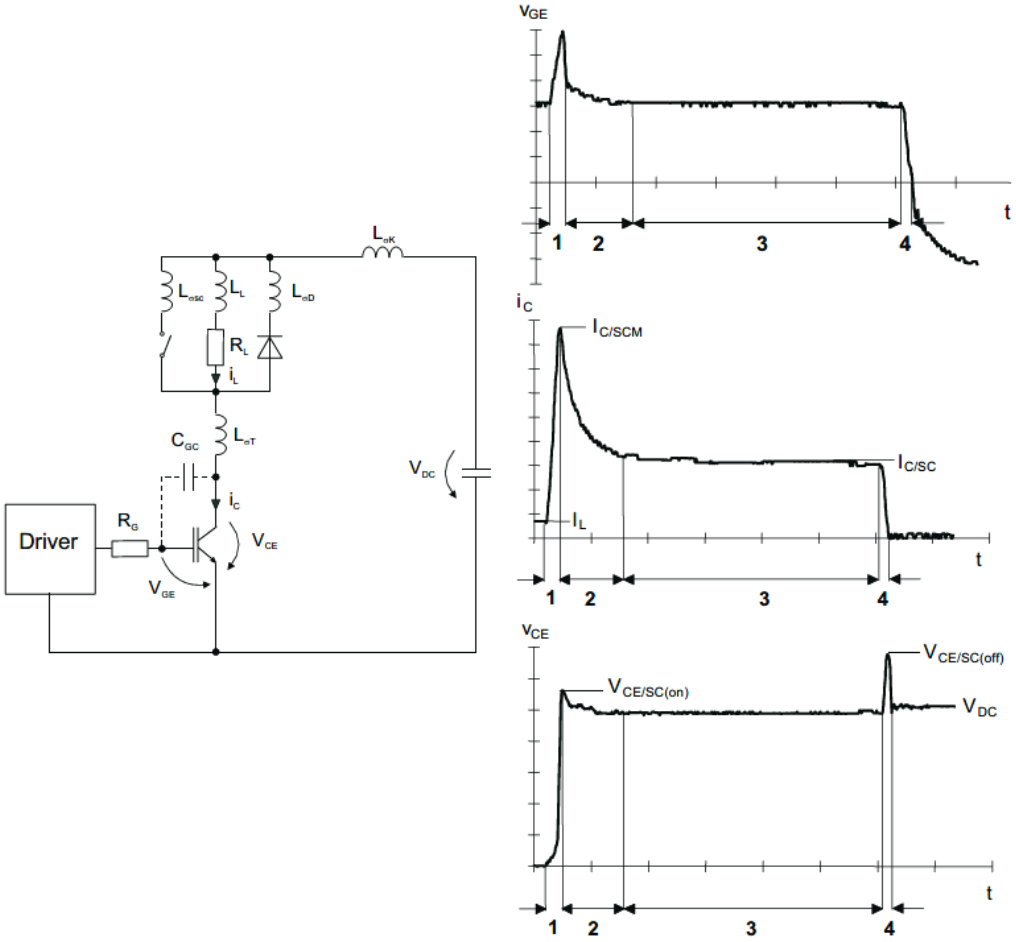


Figure 9.6.16 Equivalent circuit and principal characteristics of SC II [9.50]

As soon as the short circuit has occurred, the collector current will increase very steeply, the di/dt is determined mainly by the DC link voltage VDC and the inductance of the short circuit loop. During time interval 1, the IGBT is desaturated. The resultant high dv/dt of the collector-emitter voltage will cause a displacement current to flow through the gate-collector capacitance which will increase the gate-emitter voltage. This in turn will cause a dynamic short circuit peak current $I_{C/SCM}$.
Once the desaturation phase is complete, the short circuit current will drop to its static value $I_{C/SC}$ (time interval 2). During this procedure, a voltage will be induced over the parasitic inductances which becomes effective as overvoltage in the IGBT. The stationary short circuit phase (time interval 3) is followed by turn-off of the short circuit current towards the commutation circuit inductance L_K, which will in turn induce an overvoltage in the IGBT (time interval 4).
The transistor overvoltage induced during a short circuit may be several times higher than the normal operating values. The processes that occur during the stationary short circuit and turn-off phase are identical for SC I and II.

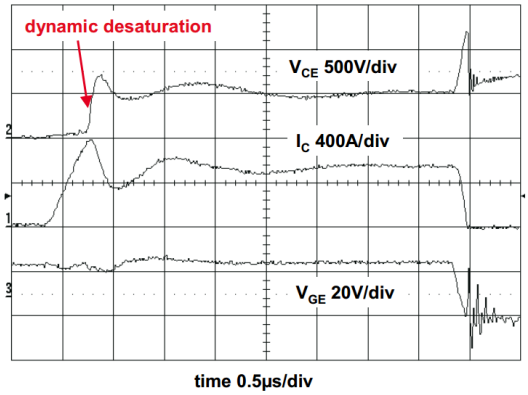


Figure 9.6.17 SC II characteristics of an IGBT with external dynamic gate voltage limitation

The SCSOA diagram (SC = short circuit) for short circuit, as shown in the IGBT datasheets or technical explanations, displays the limits for safe control of a short circuit (Figure 9.6.18 a).

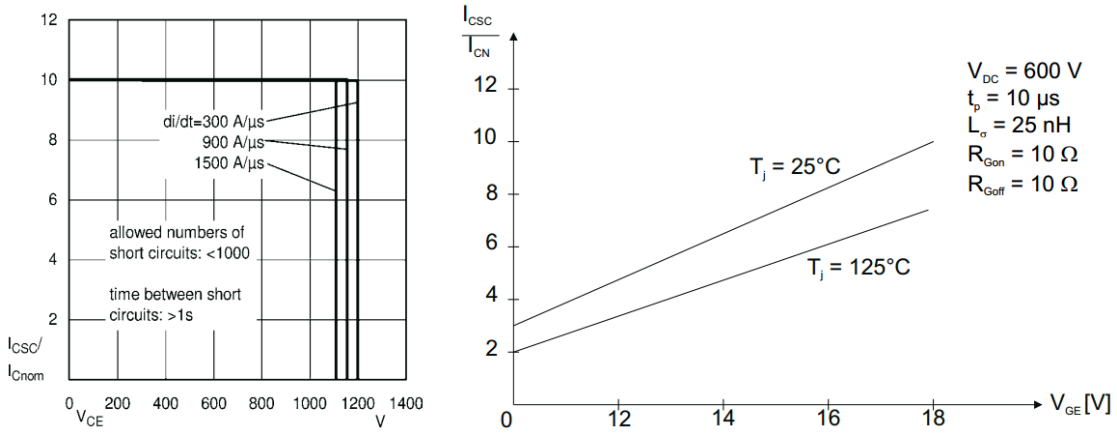


Figure 9.6.18 Short circuit specifications of an IGBT a) SCSOA; non-periodic, parameters: tsc(max), inductance in the commutation circuit, VGE, Tjmax; b) short circuit current normalised to rated current level as a function of the gate-emitter voltage

The following important conditions must be complied with in order to guarantee safe operation under short circuit conditions:

- The short circuit has to be detected and turned off within a defined maximum period of time (typically $t_{sc(max)}$= 10µs for many technologies).
- The time between two short circuits must be within a defined range (typical value for many technologies: 1s).
- The IGBT must not be subjected to more than a specified maximum number of short circuits during its entire operating time (typical value for many technologies: 1 000).

Figure 9.6.18 b) shows the influence of gate-emitter voltage and junction temperature on the static short circuit current. Short circuit I and II cause high losses in the transistor which increase the junction temperature. In such case, the negative temperature coefficient of the static short circuits current, also depicted in the IGBT and MOSFET output characteristic, proves its benefits (cf. Figure 9.6.18 b).
With respect to the turn-off overvoltage involved, a static short circuit is often not the most critical consequence, especially in applications that use modern IGBT technologies. Tests have shown that maximum overvoltage are induced by turning the IGBT off exactly at its desaturation limit. This case must always be considered when verifying the selected drive and protection concept.

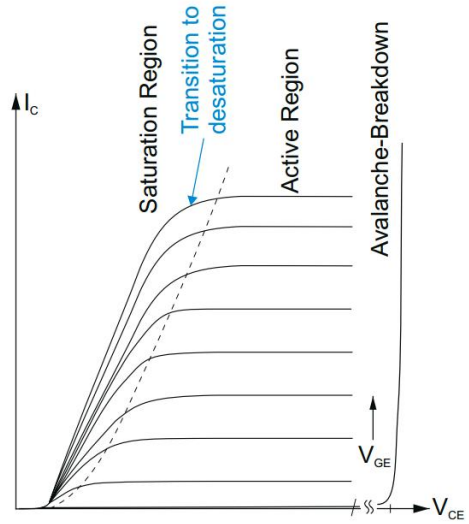


Figure 9.6.19 IGBT desaturation limit

9.6.6 Earth fault current

The earth fault current is labelled Case 3 in Figure 9.6.14. The rate of rise of the collector current di/dt depends on the earth fault inductance and the driving voltage. The earth fault circuit does not close via the DC link. The desaturation of the transistor depends on the level of the fault current. Earth fault currents occur due to a connection between a live conductor and the earth potential caused by faulty insulation or human error.

9.6.7 Fault current detection

Figure 9.6.20 shows a voltage source inverter circuit. Here, the measuring points at which fault currents can be detected are marked. The position of the measuring sensor determines which type of fault current can be detected.

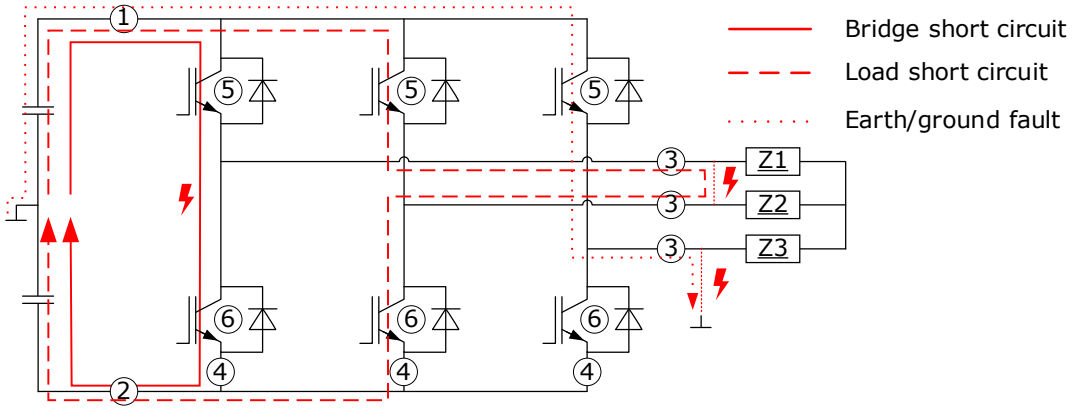


Figure 9.6.20 Voltage source inverter (VSI) with detection points for fault currents

Fault currents can be classified as follows:

- Overcurrent: detectable at points 1-7
- Arm short circuit: detectable at points 1-2 and 4-6
- Load short circuit: detectable at points 1-6
- Ground short circuit: detectable at points 1, 3, 5 or by calculating the difference between 1 and 2

In general, to control short circuit currents fast protection measures with direct control of the driver output stage are needed, since the transistor has to be switched off (with reduced switching speed, active control provided) within $t_{sc(max)}$ (typ. 10µs). To do so, fault currents may be detected at points 3, 4, 5, and 6.
Measurements at points 1-4 may be taken using measuring shunts or inductive measuring current transformers (frequently used at point 3).
Measurement shunt:

- simple measuring method
- low-resistance (1...100mW), low-inductance power shunts needed
- measuring signal is highly sensitive to interference
- measuring values are not available with potential isolation

Current sensors:

- far more expensive than measuring shunt
- measuring signal is less susceptible to interference than measuring shunt
- measuring values are available with potential isolation

Measuring points 5 and 6 represent the fault current detection directly at the terminals of the IGBT/MOSFET. The most commonly used method is v_{CEsat} or $v_{DS(on)}$ monitoring (see chapter 9.5.4.6). V_{CEsat} monitoring makes use of the relationship between collector current and collector-emitter voltage which is compared with a reference value. If the reference value is exceeded, the error memory is set and the transistor turned off. The fast desaturation process in the transistor means that short circuits are quickly detected. Temperature dependency of the output characteristic as well as parameter tolerances have negative effects on v_{CEsat} monitoring. However, the main advantage overcurrent sensing using a sense IGBT is that this protection concept is applicable to every standard IGBT or MOSFET. Current mirroring uses sense IGBT / sense MOSFET (direct measurement method).

9.6.7.1 Current sensing with sense IGBT

In a sense IGBT, a few cells are combined to create a sense-emitter, generating two parallel current arms. Information is given by the conducted collector current as soon as it passes the measuring resistor R_{Sense}. At R_{Sense} = 0 the current division ratio between both emitters is ideal, corresponding to the ratio of the number of sense-cells to the total number of cells. If R_{Sense} is increased, the current conducted in the measuring circuit will be reduced by feedback of the measuring signal. For this reason, resistance R_{Sense} should be within a range of 1...5Ω to obtain a sufficiently accurate measurement result for the collector current.
If the turn-off current threshold value is only slightly higher than the transistor rated current, the current monitoring has to be made ineffective during IGBT turn-on because of the reverse-recovery current peak of the free-wheeling diode. For very high sense-resistances ($R_{Sense} \rightarrow \infty$), the measuring voltage corresponds to the collector-emitter saturation voltage, meaning that the current sensing acts as v_{CEsat} monitoring.

9.6.8 Overtemperature

9.6.8.1 Causes

Dangerous overtemperatures occur if the maximum junction temperature specified by the device manufacturer is exceeded (e.g. T_{jmax} = 175°C...200°C).
During converter operation, overtemperatures might be generated by:

- an increase in energy dissipation caused by fault currents
- an increase in energy dissipation caused by defective drivers
- Thermal runaway caused by too high blocking current caused by too high power dissipation
- interruption of the cooling path
- failure or malfunction of the cooling system

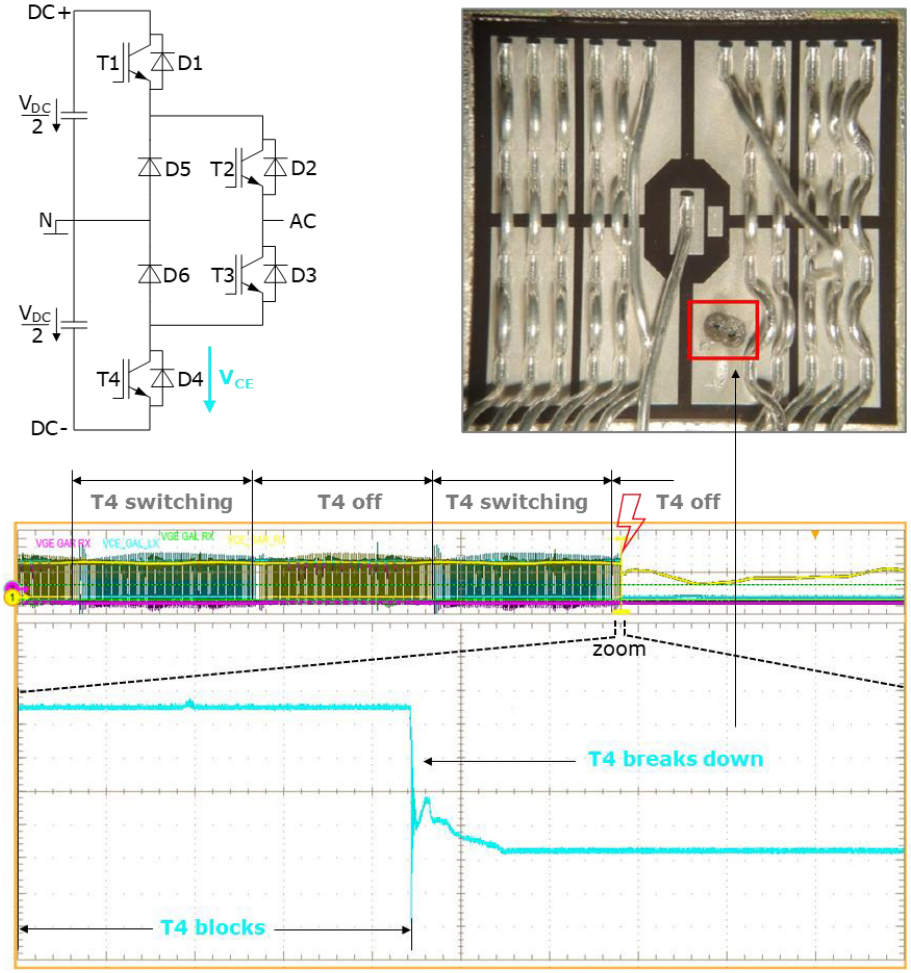


Figure 9.6.21 Thermal runaway due to too high power dissipation and consequently locally too high reverse current

Figure 9.6.21 shows the voltage measurement above the T4 switch of an NPC. As can be seen from the oscillogram, the reverse voltage at the T4 switch collapses when it is in non-switching operation. This can be explained by the fact that during the previous switching losses, the temperature in the chip rose so high that there was a strong increase in the reverse current in the blocking state. This leads to thermal runaway, which manifests itself through a hole in the chip. The fact that the hole is not at the edge of the chip is due to the temperature distribution over the chip surface. In the middle of the chip there are locally higher temperatures and thus higher reverse currents than at the edge of the chip.

9.6.8.2 Overtemperature detection

Direct measurement of the junction temperature is only possible if the temperature sensor is positioned very close to the semiconductor component (e.g. by monolithic integration or by connecting the temperature sensor and the power semiconductor chip).
Frequently, temperature is detected by evaluating the temperature-dependent blocking current of a diode, thus serving as a temperature sensor. Technologies of this kind are used in smart-power components, for example.
In transistor power module applications, temperatures are measured either outside the module at the heatsink or inside the module using temperature-dependent resistors positioned close to the power semiconductor chips on the DBC substrate.
Owing to the given thermal time constants, this measurement provides filtered information on the temperature change only (highly dynamic temperature measurement is not possible).

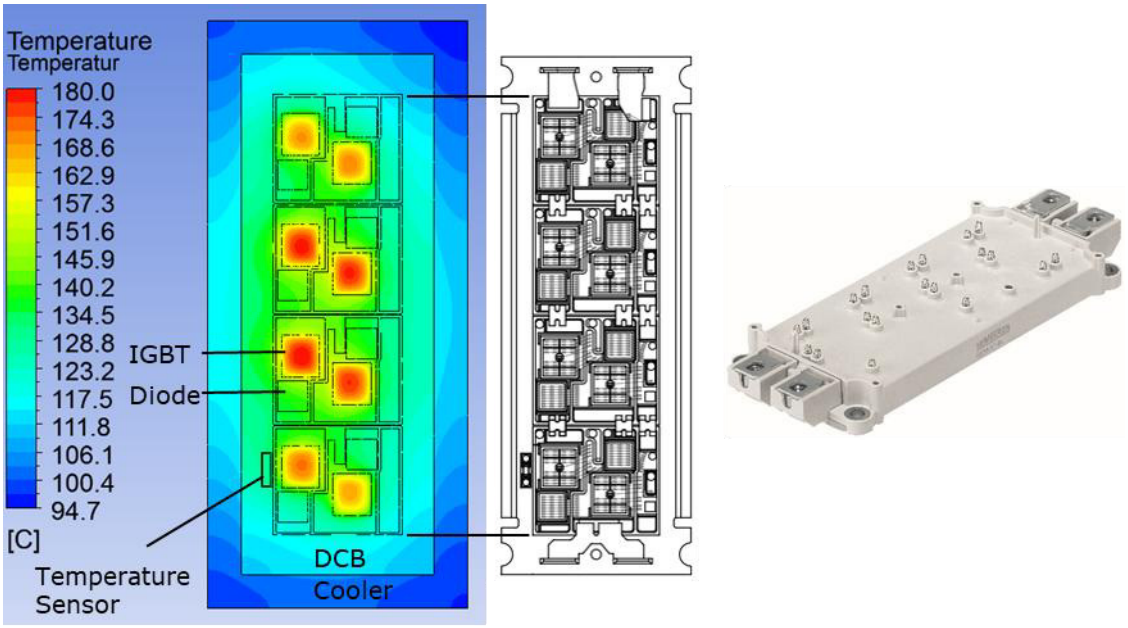


Figure 9.6.22 Thermal simulation SEMiX 4s

Table 9.6.2 shows different $R_{th(j-r)}$ and the corresponding simulated temperatures based on two different operating points of an inverter. The temperature sensor is located next to IGBT T1. In the case of power factor 0.95, the sensor temperature is higher at 102°C than at -0.95 at 95°C. The junction temperature T2/T3 is 146°C, 20K higher than T1/T4 of 126°C. The temperature sensor only provides a rough orientation.

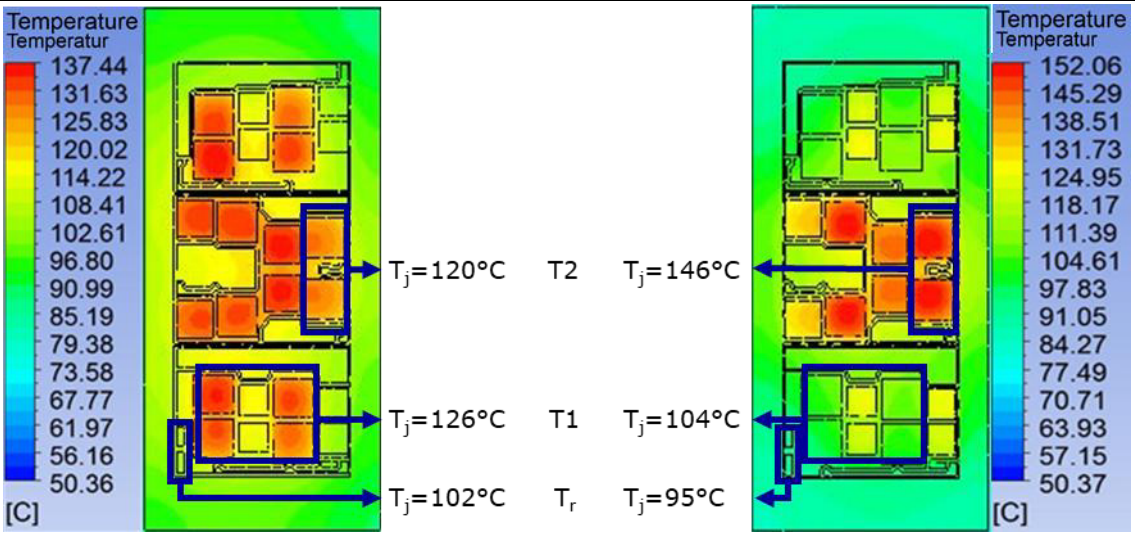
Power factor = 0.95	Power factor = -0.95
$P_{loss,T1,T4} = 287W$ $P_{loss,T2,T3} = 96W$ $T_{j,T1,T4} = 126°C$ $T_{j,T2,T3} = 120°C$ $T_r = 102°C$ $R_{th(j-r)} = \frac{T_j - T_r}{P_{loss}}$ $R_{th(j-r),T1,T4} = 0.084\frac{K}{W}$	$P_{loss,T1,T4} = 4W$ $P_{loss,T2,T3} = 187W$ $T_{j,T1,T4} = 104°C$ $T_{j,T2,T3} = 146°C$ $T_r = 95°C$ $R_{th(j-r)} = \frac{T_j - T_r}{P_{loss}}$ $R_{th(j-r),T1,T4} = 2.25\frac{K}{W}$
	

Table 9.6.2 Calculated $R_{th(j-r)}$ and simulated temperatures for power factor +/- 0.95

9.7 Use of modules in 3-level applications

9.7.1 Objectives and examples for applications

3-level topologies differ from 2-level topologies in the number of voltage levels connected to the AC output. Compared to 2-level topologies, a third potential is available in addition to the DC+ and DC- potentials with the neutral point N of the DC link (Table 9.7.1). With the definition of the output voltage $V_{out} = \varphi(AC) - \varphi(N)$ the voltage levels of the output voltage V_{out} for the respective topology can be described as follows:

$$\text{2-Level: } V_{out} = \left\{\frac{V_{DC}}{2}; -\frac{V_{DC}}{2}\right\} \qquad \text{3-Level: } V_{out} = \left\{\frac{V_{DC}}{2}; 0; -\frac{V_{DC}}{2}\right\}$$

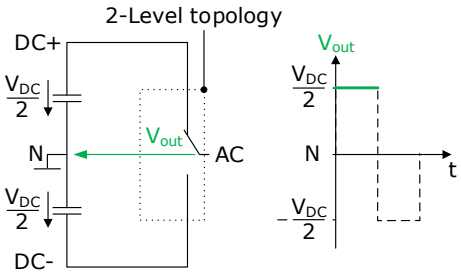
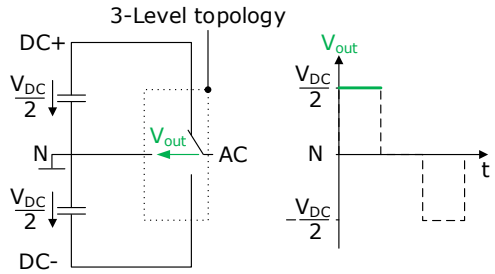
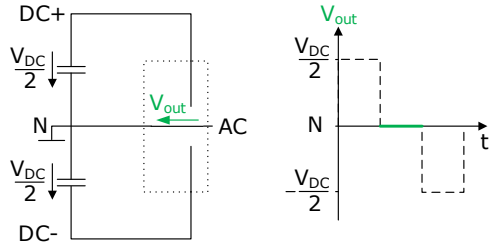
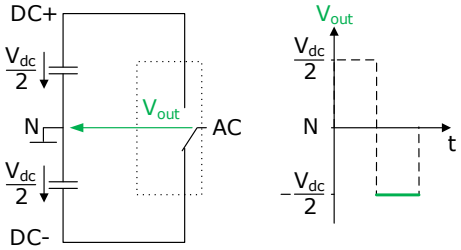
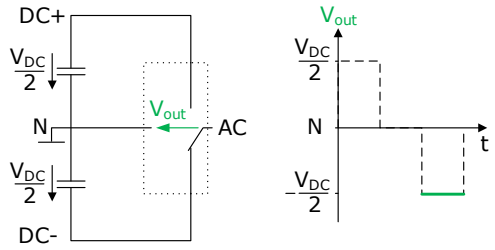
V_{out}	2-Level	3-Level
$V_{out} = \frac{V_{DC}}{2}$		
$V_{out} = 0$	Not possible due to circuitry	
$V_{out} = -\frac{V_{DC}}{2}$		

Table 9.7.1: Voltage level V_{out} for 2-level and 3-level topology

The voltage between two phases can be calculated using phases a and b as an example:

$$v_{ab} = v_{out(a)} - v_{out(b)}$$

Table 9.7.2 shows the simulated time curves of the output voltage $v_{out(a)}$, $v_{out(b)}$ and the line-to-line voltage v_{ab}. In a 2-level topology, the two voltage levels per phase lead to three voltage levels of the linked voltage v_{ab}.
In a 3-level topology, the three voltage levels per phase result in five voltage levels of the linked voltage v_{ab}. If the parameters remain the same (switching frequency, output current, DC link voltage), this means that the output voltage and the output current have a lower ripple and therefore a lower harmonic content.

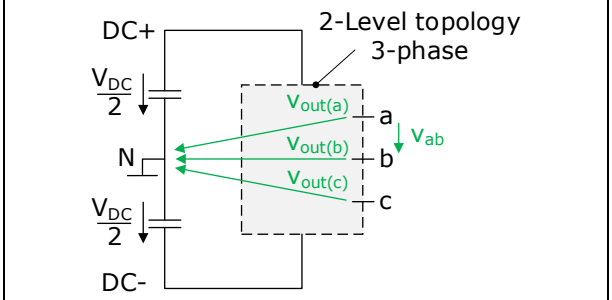
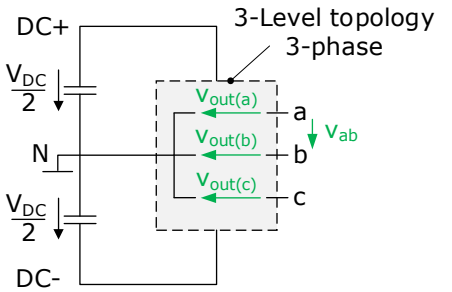
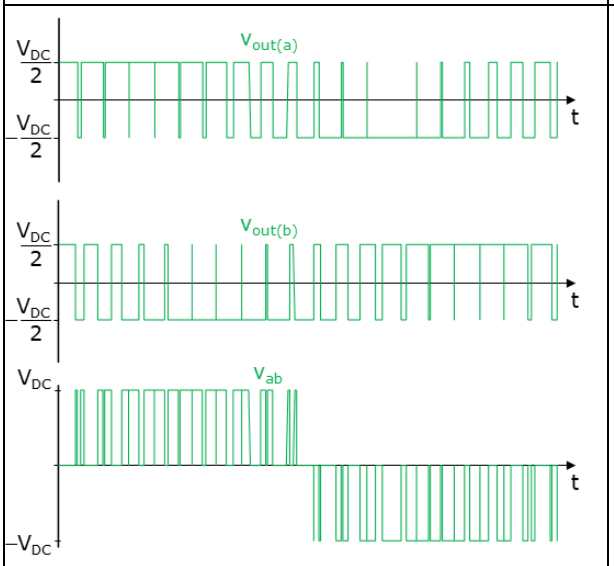
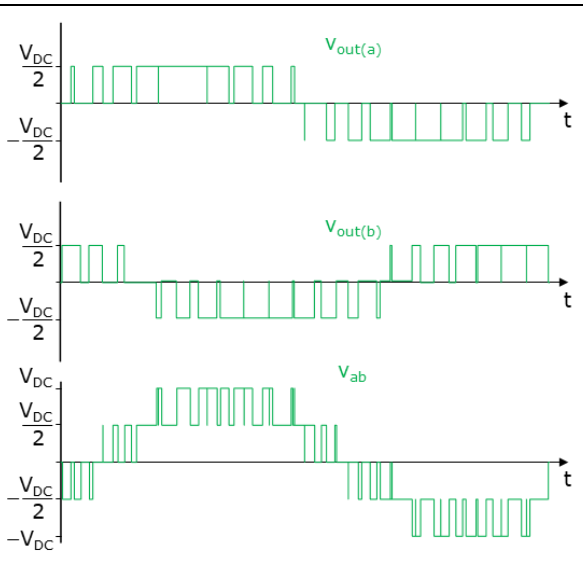
2-Level	3-Level
	
	
$v_{ab} = \{V_{DC}; 0; -V_{DC}\}$	$v_{ab} = \left\{V_{DC}; \frac{V_{DC}}{2}; 0; -\frac{V_{DC}}{2}; -V_{DC}\right\}$

Table 9.7.2: Voltage level of the output voltage v_{out} (line-neutral) and the voltage v_{ab} (line to line) for 2-level and 3-level

The best-known representatives of 3-level inverter topologies include the TNPC, NPC and ANPC designs shown in Table 9.7.3, which are used depending on the application.

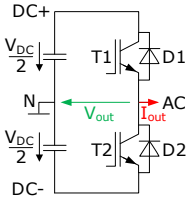
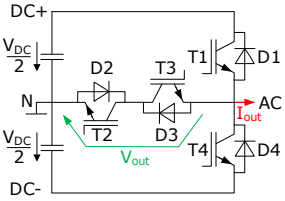
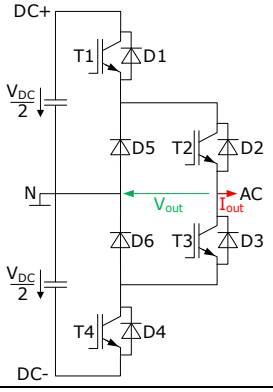
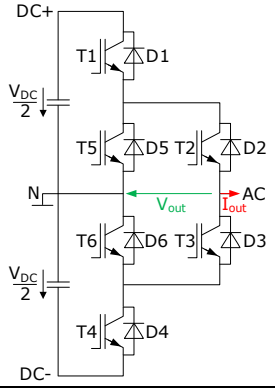
2-Level halfbridge	3-Level TNPC	3-Level NPC	3-Level ANPC
			

Table 9.7.3: 2-level halfbridge compared to 3-level topologies TNPC, NPC, ANPC

Compared to a 2-level halfbridge, a 3-level topology is associated with increased switching and control effort. This must be justified by the properties listed in Table 9.7.4 and the associated functional and financial advantages in the overall system.

Topology	Common Mode Voltage	Commutation Voltage			Device Blocking voltage capability	
		general	@V_{DC}=800V	@V_{DC}=1200V	@V_{DC}=800V	@V_{DC}=1200V
2-Level halfbridge	100%	V_{DC}	800V	1200V	1200V	1700V
3-Level TNPC	33%…66%	$\frac{V_{DC}}{2}$	400V	600V	T1,T4,D1,D4 (vertical leg)	
					1200V	1700V
					T2,T3,D2,D3 (horizontal leg)	
					650V	1200V
3-Level (A)NPC	33%…66%	$\frac{V_{DC}}{2}$	400V	600V	650V	1200V

Table 9.7.4: Comparison of different criteria between 2-level and 3-level topology

The following conclusions can be drawn from Table 9.7.4:

- The lower common mode voltage (CMV) compared to a 2-level circuit makes 3-level topologies the preferred choice for solar applications. With special CMV PWM strategies, the CMV can be reduced by up to 2/3. This results in savings in terms of cost and volume of an EMI filter.
- The third voltage level of the 3-level topology leads to a reduced harmonic content of the output current with the same mains filter as with a 2-level topology. Due to the lower harmonic content with the same switching frequency and the same mains filter, higher demands on the grid quality can be met. Alternatively, the mains filter can be reduced
- Due to the half commutation voltage and the use of components of a lower voltage class, the switching losses are lower. As the switching frequency increases, this compensates for the higher conduction losses of the two switches connected in series (horizontal branch TNPC, NPC, ANPC). This makes 3-level topologies attractive for higher switching frequencies.
- By connecting switches with a lower blocking voltage in series, 3-level topologies can be operated at high DC link and output voltages. This makes it possible to use components with a 1200V voltage class in applications with DC link voltages of 1500V_{DC} (solar).

Due to the properties mentioned above, 3-level topologies are used for applications such as solar, wind, UPS and ESS. Further details can be found in [9.51].

9.7.2 Principles and dimensioning guidelines

The function of the individual 3-level topologies can be described using the idealized time characteristic of the output voltage v_{out}, its fundamental frequency $v_{out(1)}$ and the output current i_{out} (Figure 9.7.1). The time characteristic is assigned to the four electrical quadrants Q_1 to Q_4, which result depending on the sign of the output voltage $v_{out(1)}$ and the output current i_{out}. The dwell time in each quadrant is indicated by ωt. The change in output voltage v_{out} between two voltage levels within a quadrant and the respective current direction results in two current paths for each quadrant. When the voltage changes, the current commutates between these two current paths.

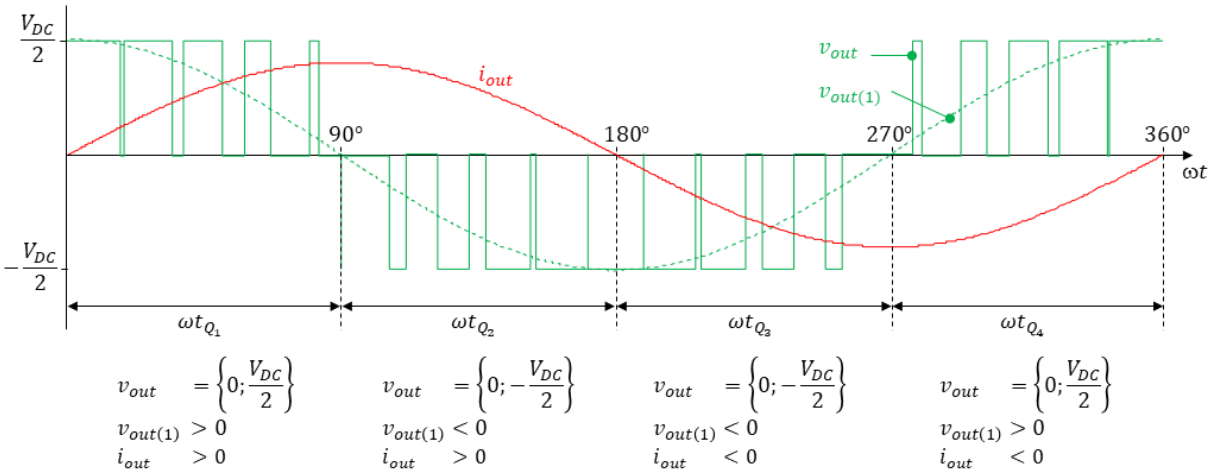


Figure 9.7.1 Time characteristic of the output voltage v_{out}, the fundamental of the output voltage $v_{out(1)}$ and the output current i_{out}

Depending on the power factor cos phi, the dwell times ωt change in the respective quadrants. This relationship is shown in Figure 9.7.2. The topologies are symmetrical. This means that the dwell times in the quadrants Q_1 and Q_3 or Q_2 and Q_4 are identical in each case.

$$t_{Q_1} = t_{Q_3}$$
$$t_{Q_2} = t_{Q_4}$$

The sum of the dwell times $t_{Q_1} + t_{Q_3}$ and $t_{Q_2} + t_{Q_4}$ represent the curves. At cosphi=1 (phase angle=0°, current and voltage in phase), the inverter is in quadrants Q_1 and Q_3 for 50% (180°) of the output period. Quadrants Q_2 and Q_4 do not occur. At cos phi=0, all four quadrants are each involved for 25% (90°). For the quadrants Q_2 and Q_4, the same statements apply at cos phi=-1 as for Q_1 and Q_3 at cos phi=1. For -1<cos phi<1, the arrow symbolizes the direction of rotation of the current-voltage pointer. Clockwise, the current leads the voltage (capacitive behaviour). Counter clockwise, the voltage leads the current (inductive behaviour). The resulting losses in the switches are identical in capacitive and inductive mode.
Depending on the topology, the voltage changes caused by switches in the quadrants result in different commutation paths, which differ in size and therefore loop inductance. Depending on the commutation path, this results in different gate resistances for the switches in order to reduce overvoltage. This means that the distribution of power loss as a function of the power factor depends on the topology used. Depending on the application and the associated power factor range, this results in certain advantages and disadvantages for the respective 3-level topology.

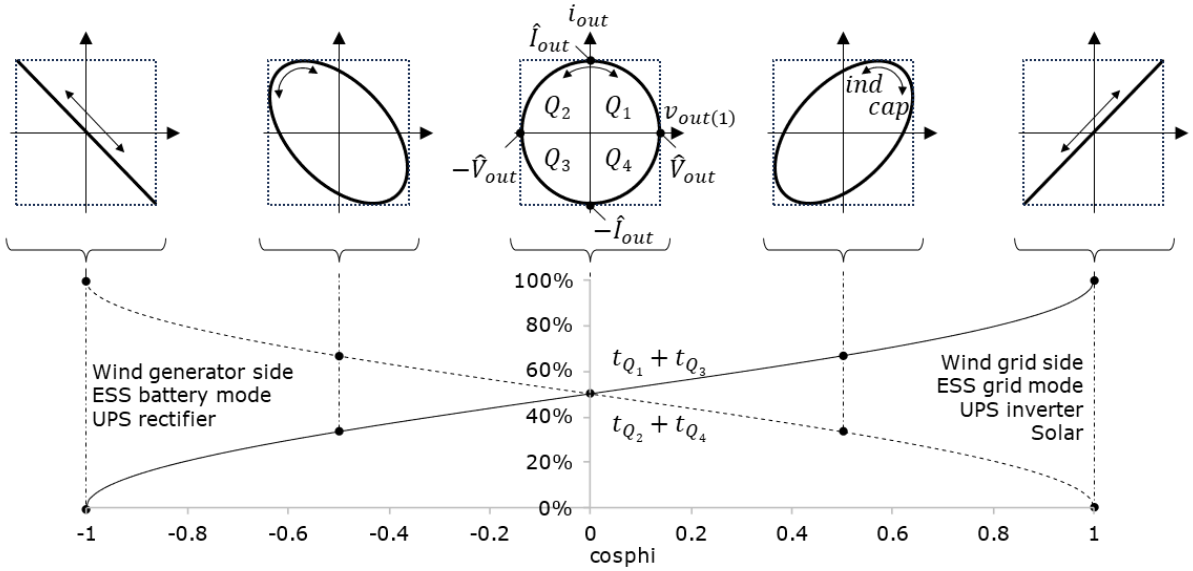


Figure 9.7.2 Percentage dwell time in the quadrant pairs Q_1 and Q_3 as well as Q_2 and Q_4 in relation to the initial period as a function of the cos phi

9.7.3 3-Level TNPC

The topology of the 3-level TNPC consists of a vertical branch (T1, T4, D1, D4) and a horizontal branch (T2, T3, D2, D3). The current commutates between these two branches. The alternating current curves in the respective quadrants are shown in Table 9.7.5. They always occur alternately via the control of the inverter. The area enclosed by both current paths represents the commutation path and is color-coded. For each of the four quadrants, there is a commutation path in which three switches are involved. In practice, the commutation paths only differ due to the module-internal structure. Theoretically, the commutation circuits are considered to be the same type of commutation circuit.
If the vertical switches carry current, the DC+ or DC- potential is applied to the AC output. This results in the requirement that the vertical switches must be able to block the full DC link voltage V_{DC}.
If the horizontal switches carry current, the N potential is present at the AC output. A maximum of half the DC link voltage $\frac{V_{DC}}{2}$ is present across the horizontal branch. Different voltage classes are therefore used for the horizontal and vertical switches (see Table 9.7.4).
The losses are made up of the conduction losses P_{cond} and the switching losses P_{sw}. The losses occurring in the blocking state can be neglected. Regardless of the power factor, there are always conduction and switching losses for the vertical branch. The composition of the losses in the horizontal branch depends on the power factor. With cos(phi)=1, only conduction losses occur in T2 and T3. The same applies to diodes D2 and D3 with a power factor of -1.

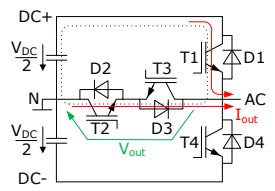
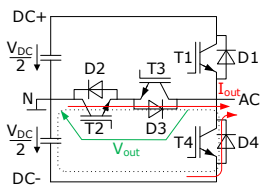
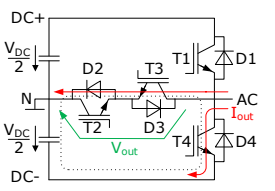
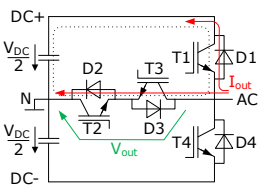
t_{Q_1}	t_{Q_2}	t_{Q_3}	t_{Q_4}
Current paths and commutation loop			
			
losses in vertical leg		Losses in horizontal leg	
T_1	$P_{sw} + P_{cond}$	–	–	–
T_2	P_{cond}	$P_{sw} + P_{cond}$	–	–
T_3	–	–	P_{cond}	$P_{sw} + P_{cond}$
T_4	–	–	$P_{sw} + P_{cond}$	–
D_1	–	–	–	$P_{sw} + P_{cond}$
D_2	–	–	$P_{sw} + P_{cond}$	P_{cond}
D_3	$P_{sw} + P_{cond}$	P_{cond}	–	–
D_4	–	$P_{sw} + P_{cond}$	–	–

Table 9.7.5 Current characteristics, commutation paths and power losses of the TNPC in the four quadrants

Typical applications for 3-level TNPC are solar applications up to max. V_{DC}=1000V and UPS. The voltage classes 1200V and 650V are typical for the vertical and horizontal switches respectively. Commutation between the vertical switches (full DC link voltage) is not provided for in the normal switching scheme. The vertical switches must therefore only be able to block the full DC link voltage.
TNPC topologies are available in various current classes (Table 9.7.6). For small to medium power classes, one module stands for one phase (“all-in-one”). A distinction is made between common collector and common emitter. Standard GB and GM modules are used for higher power classes.

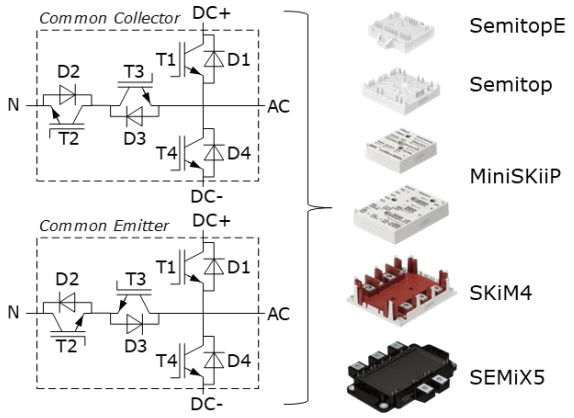
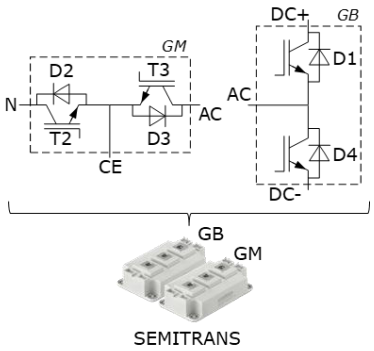
a) Modules with TNPC topology for small to medium power classes	b) GB and GM modules for higher performance classes
	

Table 9.7.6: Power modules for implementing a TNPC topology for small and medium power (a) to large power (b) classes

If the required output currents exceed the nominal module current, modules are connected in parallel. The commutation circuit shown in Table 9.7.7 is divided into two modules in this example. The connection of the two AC potentials is part of the commutation inductance and should also be as low inductive as possible. A laminated busbar with overlapping potentials enables low-inductance values to be achieved.

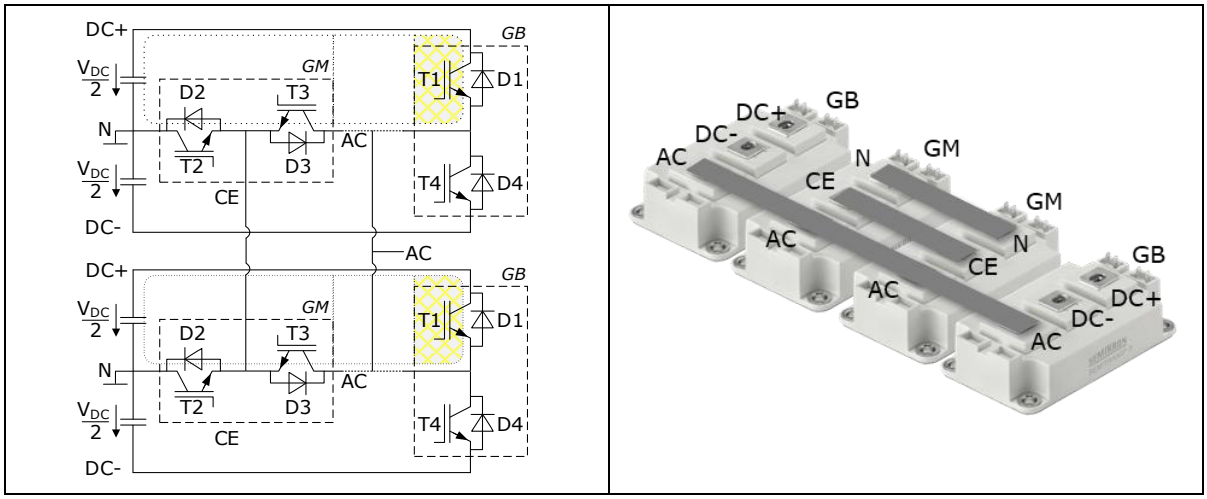


Table 9.7.7: Parallel connection of SEMITRANS 3 GB and GM module

9.7.3.1 Short circuit paths and turn-off sequences

Essential for the design of the driver is the handling of the short circuit and the overvoltage limitation. Detailed explanations can be found in [9.33].

It must be ensured that the following conditions are prevented:

- short circuit of the DC link (DC+/N, N/DC-, DC+/DC-)
- Exceeding the maximum blocking voltage of the switch

Table 9.7.8 a) shows the short circuit paths and the corresponding switch states. To avoid short circuit paths a and b, deadtimes must be implemented on the driver side between T1 and T3 and between T2 and T4. The short circuit path c does not occur in the regular circuit diagram, as commutation must always take place via the neutral path. Nevertheless, these switches must be interlocked against each other. In addition to the short circuit paths shown, the combination of all three must also be avoided (all switches switched on).

To prevent the maximum permissible voltage load on the semiconductors from being exceeded (switching off overloads or short circuit currents), turn-off sequences must be observed. The outer switches T1 and T4 must switch off first so that the current can commutate to the horizontal branch. Table 9.7.8 shows the correct (b) and incorrect (c) turn-off sequence. The aim is to switch off all active switches and generate a freewheel through the diodes.

a) Short circuit states					b) Correct turn-off sequence	c) Incorrect turn-off sequence
	T1	**T2**	**T3**	**T4**		
a	1	x	1	0		
b	0	1	x	1		
c	1	0	0	1		

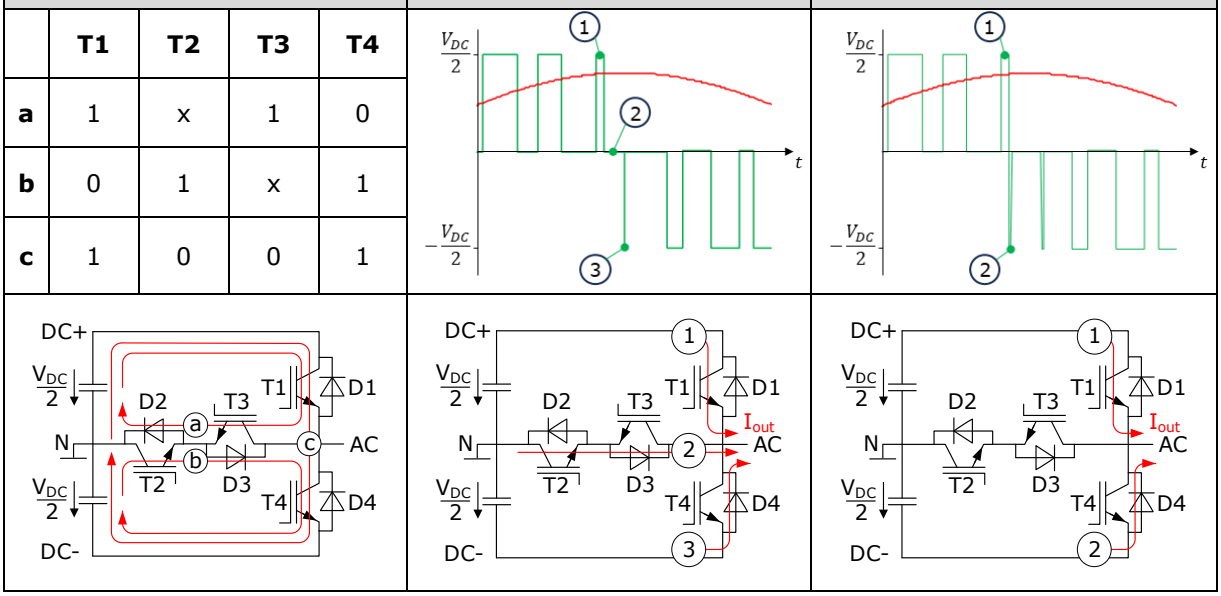


Table 9.7.8 Short circuit paths and turn-off sequence TNPC

A DC link voltage of 800V_{DC} results in a commutation voltage of 400V. If a voltage class of 650V is used for the horizontal switches, a 250V overvoltage margin is available. In the event of short circuits, it is recommended to provide active clamping on switches T2 and T3.
Chapter 9.6.2.4 describes the design of active clamping.
In the turn-off sequence according to Table 9.7.8 c), the commutation voltage is V_{DC}. An DC link voltage of 1000V_{DC} results in a 200V overvoltage reserve.

9.7.4 3-Level NPC

The topology of the 3-level NPC can be divided into an input and output stage. The switches of the input stage (T1, T4, D1, D4, D5, D6) are connected to the DC link. The switches of the output stage (T2, T3, D2, D3) are connected to the AC output.
The alternating current curves in the respective quadrants are shown in Table 9.7.9. They always occur alternately via the control of the inverter. The area enclosed by both current paths represents the commutation path and is color-coded. There are two types of commutation paths for all four quadrants:

- Short commutation path in quadrants 1 and 3
  - Commutation only takes place within the input stage and comprises two switches (T1-D5, T4-D6).
- Long commutation path in quadrants 2 and 4
  - The commutation path includes switches of the input and output stage. It comprises four switches (T2-D3-D4-D5, T3-D1-D2-D6).

If the external switches carry current (T1, T4, D1, D4) in series with the switches of the output stage (T2, T3, D2, D3), the DC+ or DC- potential is present at the AC output. In this case, the blocking switches share the full DC link voltage V_{DC}.
If the clamping diodes D5, D6 carry the current, the N potential is present at the AC output. In this case, the blocking switches share half the DC link voltage. The same voltage class is therefore used for all switches (see Table 9.7.4).
The losses are made up of the conduction losses P_{cond} and the switching losses P_{sw}. The losses occurring in the blocking state can be neglected. Regardless of the power factor, the outer switches

(T1, T4, D1, D4) always have conduction and switching losses. This is equivalent to the vertical branch in the TNPC.
The composition of the losses of the switches in the output stage (T2, T3, D2, D3) depends on the power factor. In quadrants Q_1 and Q_3, only conduction losses occur in T2 and T3. This means that with cos phi=1 the total losses over an output period are exclusively conduction losses. This is equivalent to the switches T2 and T3 in the TNPC. The diodes D2 and D3 only cause conduction losses in the quadrants Q_2 and Q_4. The switching losses of the diodes do not occur as the switch in parallel is switched on (ZVS). The clamping diodes D5 and D6 cause switching and conduction losses in quadrants Q_1 and Q_3. In quadrants Q_2 and Q_4 there are only conduction losses. At cos phi=-1, the share of switching losses in the total losses is 0%. Only conduction losses occur.
Due to the larger commutation inductance, switches T2 and T3 have a higher gate resistance than switches T1 and T4. The overvoltage must be limited when the switches themselves are switched off. Switching the switches on influences the overvoltage when diodes D1 and D4 are switched off. In quadrants Q_2 and Q_4, the use of higher gate resistors also results in higher switching losses.
As the power factor decreases, the proportion of quadrants Q_2 and Q_4 in the output period increases. This results in an asymmetrical power loss distribution over the power factor. The NPC is very suitable for applications with a limited power factor ...1.

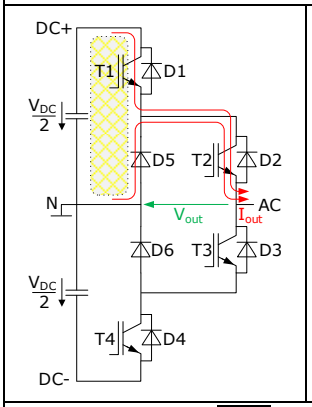
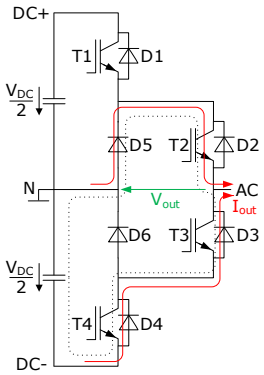
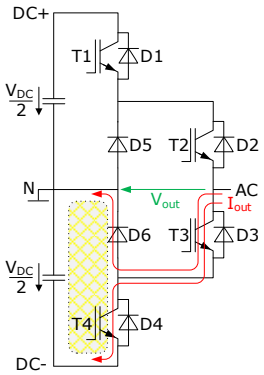
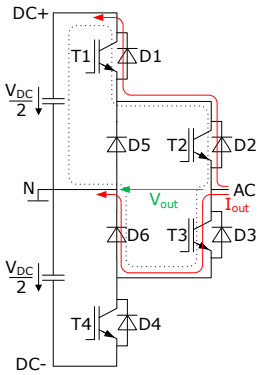
t_{Q_1}	t_{Q_2}	t_{Q_3}	t_{Q_4}
Current paths and commutation loop			
			
losses in input stage		losses in output stage	
$T1$	$P_{sw} + P_{cond}$	–	–	–
$T2$	P_{cond}	$P_{sw} + P_{cond}$	–	–
$T3$	–	–	P_{cond}	$P_{sw} + P_{cond}$
$T4$	–	–	$P_{sw} + P_{cond}$	–
$D1$	–	–	–	$P_{sw} + P_{cond}$
$D2$	–	–	–	P_{cond}
$D3$	–	P_{cond}	–	–
$D4$	–	$P_{sw} + P_{cond}$	–	–
$D5$	$P_{sw} + P_{cond}$	P_{cond}	–	–
$D6$	–	–	$P_{sw} + P_{cond}$	P_{cond}

Table 9.7.9 Current characteristics, commutation paths and power losses of the NPC in the four quadrants

Typical applications for 3-level NPC are solar applications up to max. V_{DC} = 1500V and UPS.
NPC topologies are available in different current classes (Table 9.7.10). For small to medium power classes, one module stands for one phase (“all-in-one”). For higher power classes, so-called split modules are used, which consist of a TOP and BOT module and form one phase. These are standard halfbridge modules (GB), which also contain the clamping diodes D5 and D6.

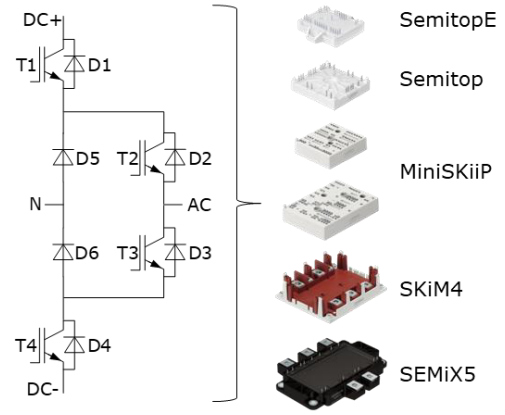
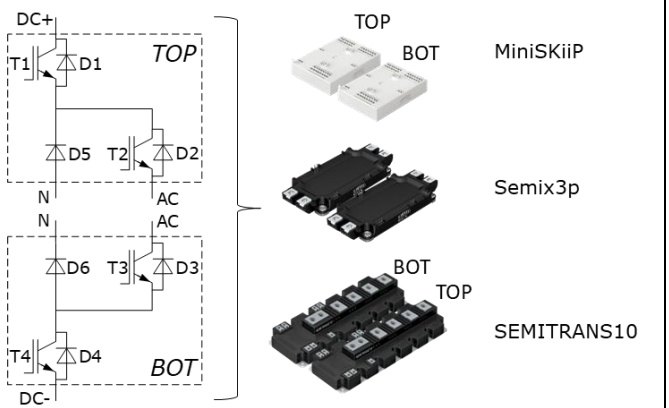
a) Modules with TNPC topology for small to medium power classes	b) Split NPC modules for higher performance classes
	

Table 9.7.10: Power modules for implementing an NPC topology for small and medium (a) power to large power (b) classes

With Split-NPC modules, the long commutation path in quadrants Q_2 and Q_4 extends across both modules. The AC potential is split and is part of the commutation path. The mechanical design has an influence on the commutation inductance.
Table 9.7.11 shows three different AC connections and their influence on the inductance of the long commutation path.

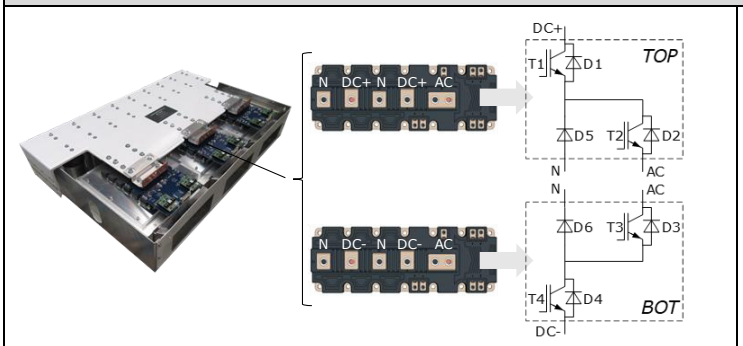
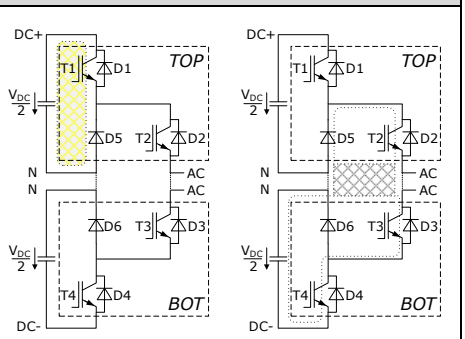
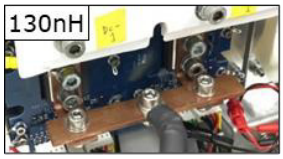
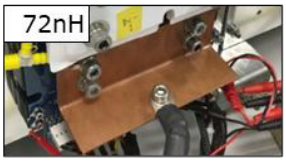
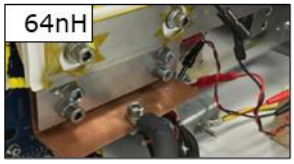
Stray Inductance in Long Commutation Loop		
		
		

Table 9.7.11: Influence of the AC connection on the inductance of the large commutation path

9.7.4.1 Short circuit paths and turn-off sequences

Essential for the design of the driver is the handling of the short circuit and the overvoltage limitation. Detailed explanations can be found in [9.33].

It must be ensured that the following conditions are prevented:

- short circuit of the DC link (DC+/N, N/DC-, DC+/DC-)
- Exceeding the maximum blocking voltage of the switch

Table 9.7.12 a) shows the short circuit paths and the corresponding switch states. To avoid short circuit paths a and b, deadtimes must be implemented in the driver between T1 and T3 and between T2 and T4. In addition to the short circuit paths shown, the combination of both must also be avoided (all switches switched on). Table 9.7.12 b) and c) show the cases in which the full DC link voltage is applied to T2 or T3. If the switches T1 and T2 or T3 and T4 carry current, the DC+ or DC- potential is present at the output. If the outer switch is switched on in each case, the full DC

link voltage V_{DC} is present at switch T2 or T3. If the DC link voltage exceeds the maximum blocking voltage of the switches, this will destroy the switch.

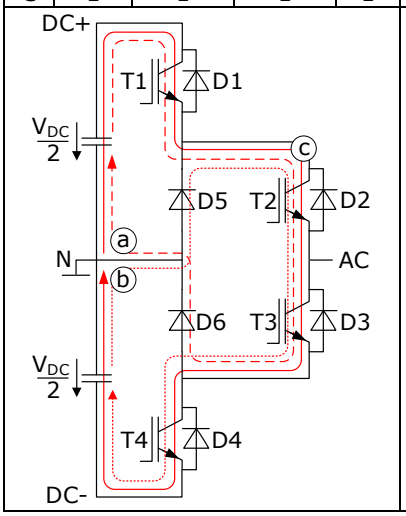
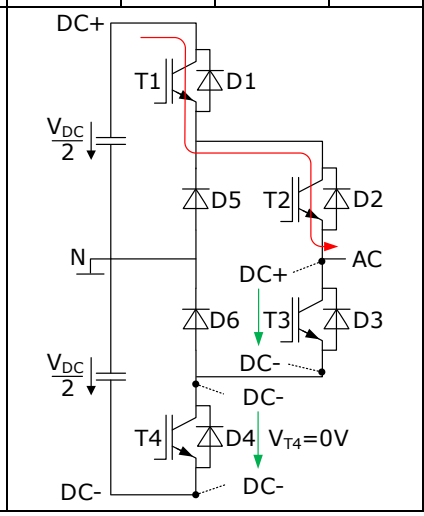
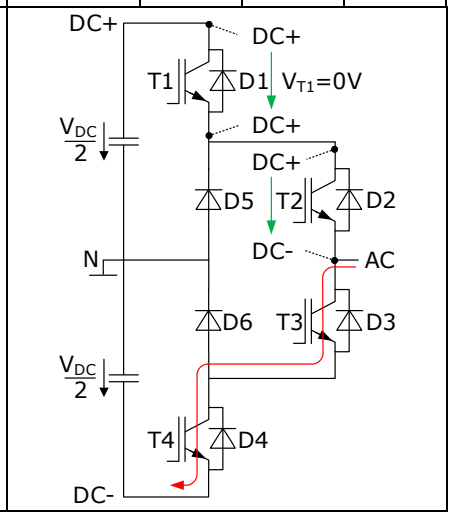
	a) Short circuit				b) Full DC link voltage across T2				c) Full DC link voltage across T3			
	T1	**T2**	**T3**	**T4**	**T1**	**T2**	**T3**	**T4**	**T1**	**T2**	**T3**	**T4**
a	1	1	1	0	1	0	1	1	1	1	0	1
b	0	1	1	1								
c	1	1	1	1								
											

Table 9.7.12 Short circuit paths and turn-off sequence NPC

To avoid critical voltage states for the switches (voltage changes at the output, switching off overloads or short circuit currents), turn-off sequences must be observed. The external switches T1 and T4 must switch off first so that the current can commutate to the clamping diode D5 or D6. Table 9.7.13 shows the correct and incorrect turn-off sequence.
The voltage change from DC+ to DC- must always take place via the neutral path in order to avoid overvoltage problems. In the case of the NPC, the full DC link voltage is applied to T2 if the turn-off sequence is incorrect. This can lead to destruction if the maximum blocking voltage of the switch is exceeded.

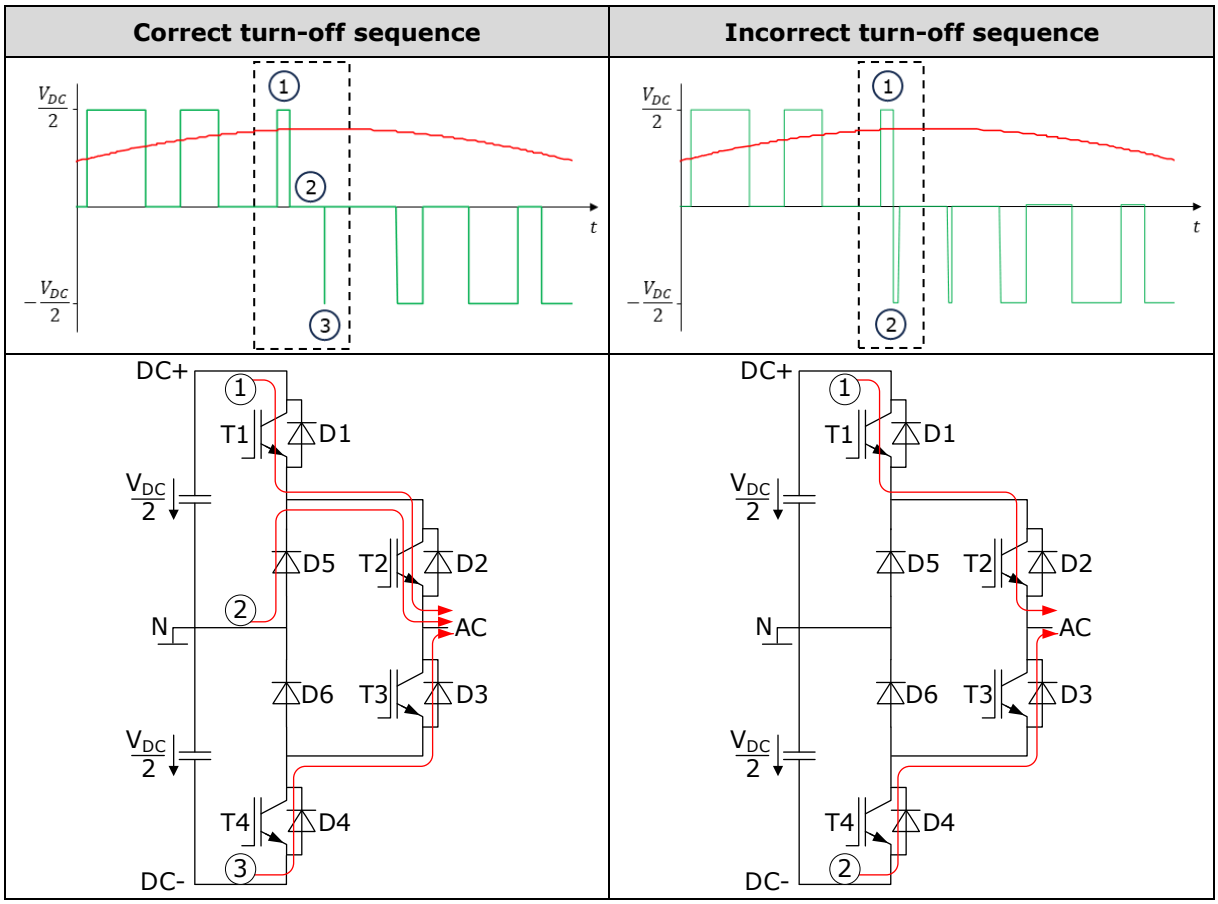


Table 9.7.13 Short circuit paths and turn-off sequence NPC

9.7.5 3-Level ANPC

The Active Neutral Point Clamp (ANPC) differs from the NPC in that it has two additional switches T5 and T6 (Table 9.7.14). This results in greater degrees of freedom with regard to control and therefore also different commutations. Various control methods are known for the ANPC. Two of the most commonly used are the PWM-1 and PWM-2 control methods [9.52], [9.53] and [9.54].

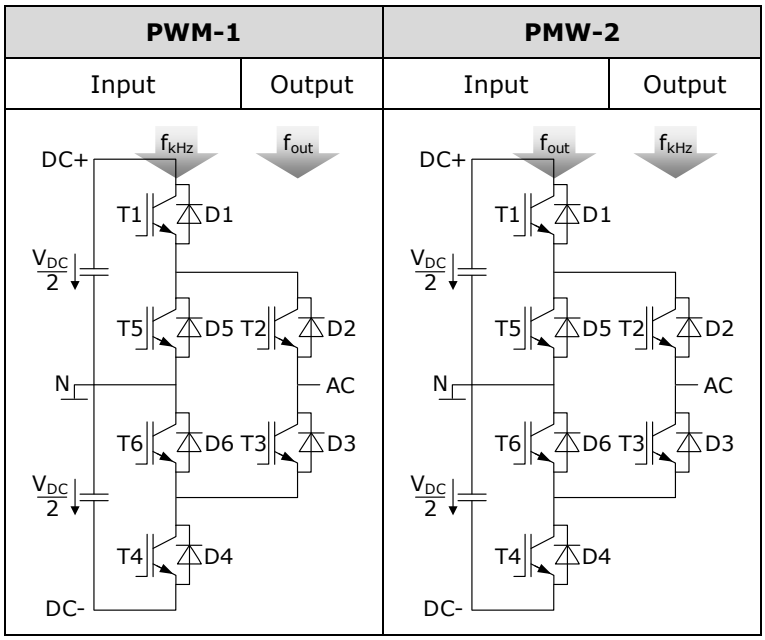


Table 9.7.14 ANPC divided into input and output stage. Assignment of the switching frequency range (output frequency f_{out}, kHz range f_{kHz}) to classify the control methods

9.7.5.1 ANPC control method PWM-1

Table 9.7.15 shows the alternating current paths and the resulting commutation paths in the individual quadrants. The input stage switches in the kHz range, the output stage switches with the period of the output current f_{out} (e.g. 50Hz). For this reason, the switching losses of the output stage are neglected in the analysis. Commutation only takes place in the input stage in all 4 quadrants. This allows the ANPC topology to be divided into three standard halfbridge modules with this control method, which reduces the challenges with regard to overvoltage within the large commutation loops during high-frequency commutation.

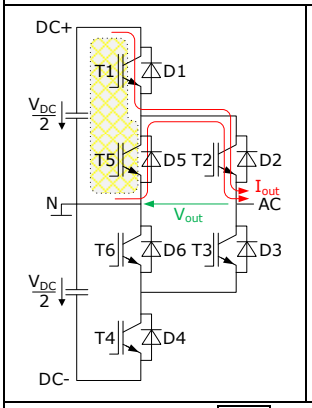
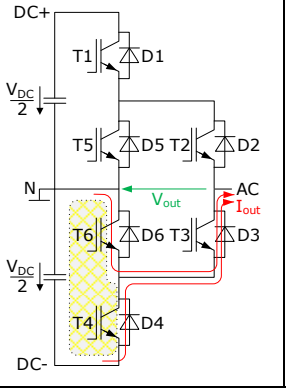
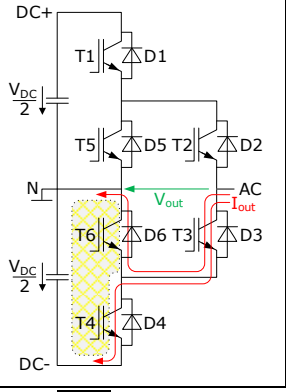
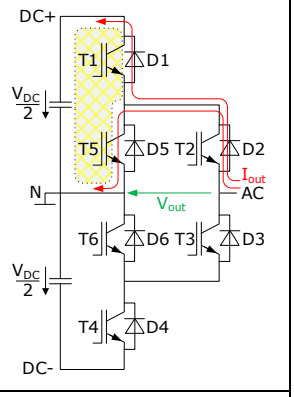
t_{Q_1}	t_{Q_2}	t_{Q_3}	t_{Q_4}
Current paths and commutation loop			
			
losses in input stage		losses in output stage	
$T1$	$P_{sw} + P_{cond}$	–	–	–
$T2$	P_{cond}	–	–	–
$T3$	–	–	P_{cond}	–
$T4$	–	–	$P_{sw} + P_{cond}$	–
$T5$	–	–		$P_{sw} + P_{cond}$
$T6$	–	$P_{sw} + P_{cond}$		–
$D1$	–	–	–	$P_{sw} + P_{cond}$
$D2$	–	–	–	P_{cond}
$D3$	–	P_{cond}	–	–
$D4$	–	$P_{sw} + P_{cond}$	–	–
$D5$	$P_{sw} + P_{cond}$	–	–	–
$D6$	–	–	$P_{sw} + P_{cond}$	–

Table 9.7.15: Current characteristics, commutation paths and power losses of the ANPC with PWM-1 control method in the four quadrants

Figure 9.7.3 shows a single-phase ANPC stack with SEMITRANS 20 halfbridge modules. The control method is based on PWM-1, resulting in exclusively small commutation paths in which only one power module is involved. This topology is typically used in wind and ESS applications.

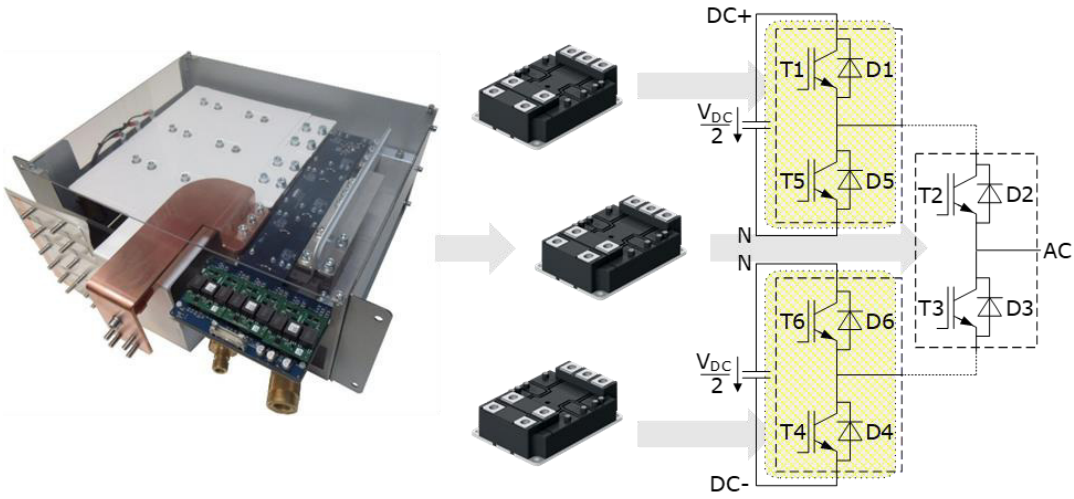


Figure 9.7.3 Single-phase ANPC stack with SEMITRANS 20 halfbridge modules

9.7.5.2 ANPC control method PWM-2

Table 9.7.16 shows the alternating current paths and the resulting commutation paths in the individual quadrants for the ANPC with PWM-2 control method. The input stage switches with the period of the output current f_{out} (e.g. 50Hz), the output stage in the kHz range. For this reason, the switching losses of the input stage are neglected in the analysis. For this reason, switches with low conduction losses can be used for the input stage and switches with low switching losses (e.g. SiC MOSFET) for the output stage. Switches from the input and output stage are always involved in the commutation in all 4 quadrants. This always results in a large commutation path, which means that the use of this control method is focused on smaller modules.

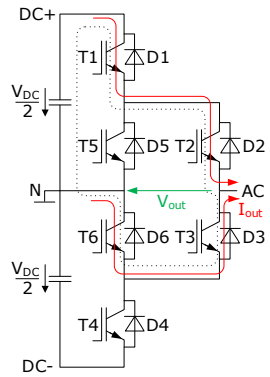
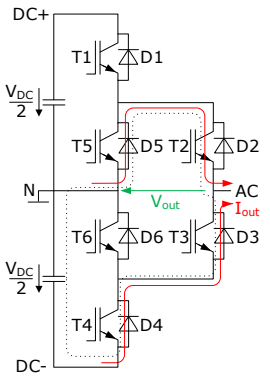
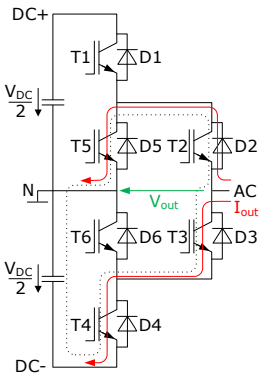
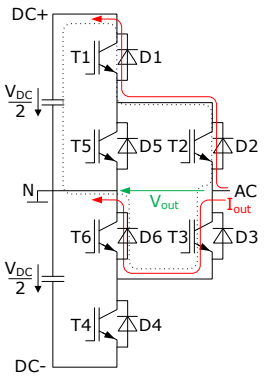
	t_{Q_1}	t_{Q_2}	t_{Q_3}	t_{Q_4}
Current paths and commutation loop				
				
	losses in input stage		losses in output stage	
$T1$	P_{cond}	–	–	–
$T2$	$P_{sw} + P_{cond}$	$P_{sw} + P_{cond}$	–	–
$T3$	–	–	$P_{sw} + P_{cond}$	$P_{sw} + P_{cond}$
$T4$	–	–	P_{cond}	–
$T5$	–	–	P_{cond}	–
$T6$	P_{cond}	–	–	–
$D1$	–	–	–	P_{cond}
$D2$	–	–	$P_{sw} + P_{cond}$	$P_{sw} + P_{cond}$
$D3$	$P_{sw} + P_{cond}$	$P_{sw} + P_{cond}$	–	–
$D4$	–	P_{cond}	–	–
$D5$	–	P_{cond}	–	–
$D6$	–	–	–	P_{cond}

Table 9.7.16: Current characteristics, commutation paths and power losses of the ANPC with PWM-2 control method in the four quadrants

9.7.5.3 Short circuit paths and turn-off sequences

Essential for the design of the driver is the handling of the short circuit and the overvoltage limitation. Detailed explanations can be found in [9.33].

It must be ensured that the following conditions are prevented:

- short circuit of the DC link (DC+/N, N/DC-, DC+/DC-)
- Exceeding the maximum blocking voltage of the switch

Table 9.7.17 a) shows the short circuit paths and the corresponding switch states. In order to avoid short circuit path a, deadtimes must be implemented in the driver between T1 and T5 and between T6 and T4. In addition to the short circuit paths shown, the combination of both must also be avoided (all switches switched on).

	Short circuit DC+ to N						Short circuit N to DC-						Short circuit DC+ to DC-					
	T1	T2	T3	T4	T5	T6	T1	T2	T3	T4	T5	T6	T1	T2	T3	T4	T5	T6
a	1	0	1	0	0	0	0	0	0	1	0	1	1	1	1	1	0	0
b	1	1	1	0	0	X	0	1	1	1	x	0	1	0	0	1	1	1

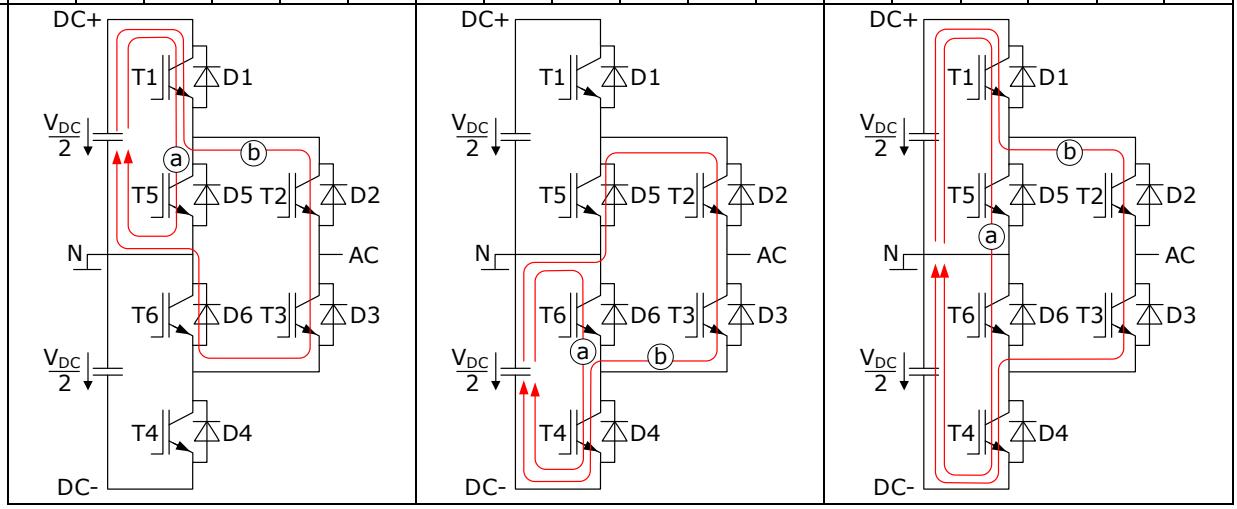


Table 9.7.17 Short circuit paths ANPC

9.7.6 Summarized comparison

Criteria	3-Level TNPC	3-Level NPC	3-Level ANPC PWM-1	3-Level ANPC PWM-2
Types of commutation loops	1	2	1	1
Switches included in commutation	3	Small loop: 2 Long loop: 4	2	4
Types of topology realization	All-in-One* GB-GM	All-in-One* TOP-BOT Split 3x GB	All-in-One* 3x GB	All-in-One*
Optimum power factor range	-1 or 1	…1	-1…1	-1…1
Switching frequency compared to the other topologies	Lower than NPC/ANPC	Higher than TNPC as devices with lower blocking voltage can be used		
Size of power modules	Small…large	Small…large	Small…large	Small…medium
Application	Solar 1000V UPS	Solar 1500V	Solar 1500V ESS, Wind	ESS
Chip optimisation	Depends on Power factor	Depends on Power factor	Independent of power factor Input: Low P_{sw} Output: Low P_{cond}	Independent of power factor Input: Low P_{cond} Output: Low P_{sw}

Table 9.7.18 Summarized comparison between TNPC, NPC, ANPC (*All switches in one module)

9.8 Soft switching as ZVS or ZCS, snubber networks

9.8.1 Objectives and areas of application

Industrial power electronic circuit engineering in the medium and upper power class range is dominated by topologies related to impressed direct voltages. In these circuits, IGBT and MOSFET are operated almost exclusively in hard switching mode, i.e. they are subject to high switching losses and power dissipation peaks, resulting in typical switching frequencies between 1kHz and 30kHz (IGBT) or 50 to 100kHz (MOSFET).
Increasing the switching frequency will generally lead to reduction in size and weight of passive energy storage components (chokes, capacitors, transformers, filters), which is of interest, for example, with respect to the integration of transformers into converter systems.
Typical areas of application are:

- Battery charging
- UPS with potential-isolated DC-DC converter
- electronic power supply units (switch-mode power supply) for general applications
- PFC circuits
- industrial power supply systems (welding, electroplating, inductive heating, x-ray, plasma, etc.).

If the required switching frequencies cannot be obtained in a hard-switch application, either interleaved technologies have to be used or the resulting switching losses have to be reduced. Basically, there are two ways of reducing switching losses:

- Implementation of additional switching loss reduction networks, whilst keeping the basic circuitry (snubber circuit)
- Soft switching as ZVS (Zero Voltage Switch) or ZCS (Zero Current Switch)

9.8.2 Switching loss reduction networks / snubber circuits

Power-electronic switches with conventional thyristors or GTOs require snubber circuits in order to guarantee operation within the safe operating area, i.e. these networks are indispensable if the components are to live up to their basic functions during switching. In contrast to this, the SOA characteristics of modern IGBT and MOSFET allow operation without the use of networks, meaning that additional networks may only serve to reduce switching losses or perform symmetry tasks in the case of cascading.
Figure 9.8.1 shows a conventional buck converter with IGBT and basic networks for turn-on and turn-off relief (reduction of switching losses).

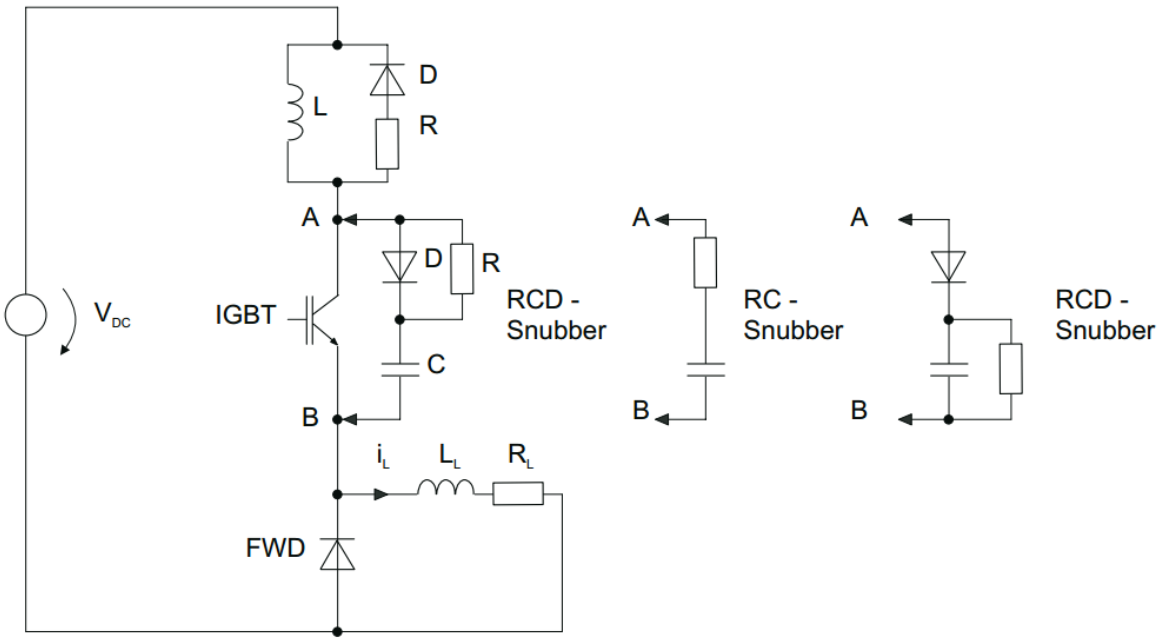


Figure 9.8.1 Buck converter with IGBT and basic switching loss reduction networks

9.8.2.1 Reduction of turn-on losses (RLD network)

To begin with, the IGBT is in off-state ($v_{CE} \approx v_{DC}$), and the load current is flowing in the freewheeling circuit. Commutation from the freewheeling diode to the IGBT is started by active IGBT turn-on. As soon as the snubber inductance L has reached a certain value, it will take up the commutation voltage almost completely (this corresponds to the input DC voltage of the converter) when the collector current rises, meaning that the collector-emitter voltage is quickly reduced to a very low level. At the same time, the network inductance will bring about a reduction in the current commutation speed.
Together, these two factors lead to a substantial decrease in IGBT turn-on losses.
The characteristics of collector current and collector-emitter voltage correspond to soft switching as explained in chapter 1.
In chapter 9.8.3 it will be shown that the use of inductances with just some microhenry are sufficient to effectively reduce IGBT and MOSFET power losses.
In addition to the reduction of IGBT turn-on losses, the turn-off losses of the freewheeling diode will also be decreased during commutation, since the reduced current commutation speed will lead to low-level reverse recovery peak currents.
The combination of R-D will create a freewheeling circuit for the network inductance, which will limit IGBT and FWD overvoltage during turn-off.
Recommendations for dimensioning:

1. The network inductance should not to be dimensioned any bigger than needed for loss reduction,
2. Reduce the inherent (internal) capacitance of the snubber inductor to a minimum,
3. R and L form the time constants (t = L/R) necessary for internal energy discharge in the inductor. This results in a minimum IGBT static off-time (duty cycle limitation) to achieve efficient reduction of turn-on power losses (no residual current in L). On the one hand, increasing R will reduce the minimum IGBT static off-time; on the other hand, however, it will lead to a higher voltage and, consequently, higher power dissipation in the power semiconductors that are turning off.

9.8.2.2 Reduction of turn-off losses (RCD snubbers)

To begin with, the IGBT is in on-state and conducts the load current.
Commutation from the IGBT to the freewheeling diode is started by active IGBT turn-off.
The load current quickly commutates from the IGBT to the parallel D-C branch, causing the collector current and the collector-emitter dv/dt to decrease at the same time.
This leads to a reduction in the IGBT turn-off losses. The characteristics for collector current and collector-emitter voltage corresponds to soft switching as explained in chapter 1.
Chapter 9.8.3 shows that the loss reduction that can be achieved with a certain capacitance strongly depends on the given transistor technology. At the end of voltage commutation, the freewheeling diode will turn on with low losses and take up the snubber capacitance current. As of the next time the IGBT turns on, the energy stored in the snubber network capacitor will be mainly converted to heat by resistor R.
Recommendations for dimensioning:

- The snubber inductance should not to be dimensioned any bigger than needed for loss reduction
- Use fast network diode with lower turn-on overvoltage (forward recovery)
- Use pulse-proof capacitors (film capacitors or similar) with low internal inductance
- Reduce loop inductance in the snubber network to a minimum
- R and C form the time constants ($t = R \cdot C$) necessary for internal energy discharge in the capacitor. This results in a minimum IGBT static off-time (duty cycle limitation) to achieve efficient reduction of turn-off power losses (no residual voltage in C). On the one hand, decreasing R will reduce the minimum IGBT static on-time; on the other hand, however, it will lead to a higher current and, consequently, greater losses when the transistor is turned on.

Note that larger inductive and capacitive snubber elements will always lead to longer commutation times!

In applications that use simple snubber networks, as described above, the total energy stored is converted to heat mainly in the network resistor but also partially in the transistor (dissipative snubber). Thus, the overall efficiency of the circuit will not be improved - irrespective of the

reduced losses in the switches. All this measure does is move the losses from the semiconductor to the snubber resistor, thus allowing higher switching frequencies.
Furthermore, numerous low-loss snubber networks (non or low-dissipative snubbers), where the energy is stored in resonant circuits or fed back to the DC link, are well-known from relevant literature. However, circuit designs such as these are often very complicated to dimension, and the layout and circuitry requirements are very challenging, too.

9.8.3 Soft switching

9.8.3.1 Load on power semiconductors

Soft switching is another possible way of reducing losses in power electronic switches. The expression "soft switching" actually refers to the operation of power electronic switches as zero-voltage switches (ZVS) or zero-current switches (ZCS) (cf. chapter 1). The many different converter circuits that working according to these principles are generally assigned to resonance or quasi-resonance technology.

ZVS (Figure 9.8.3):

- The commutation process is started by active turn-off, switching losses are reduced thanks to parallel connection of commutation capacitance C_K
- the commutation process is completed by passive, low-loss turn-on at a switch voltage $v_s \approx 0$,
- before next commutation, the direction of current flow changes in the switch that is turned on with impressed di/dt,
- Inductance in commutation circuit LK should be at the minimum

ZCS (Figure 9.8.5):

- The commutation process is started by active turn-on, switching losses are reduced thanks to series connection of commutation inductance L_K
- the commutation process is completed by passive, low-loss turn-off at a switch current $i_s \approx 0$
- before next commutation, the voltage direction changes in the switch that is turned on with impressed di/dt
- Capacitance in commutation circuit C_K should be at the minimum

Continuous soft switching is based on the condition that only one kind of commutation process - either inductive commutation / ZCS or capacitive commutation / ZVS – takes place in the commutation circuit of the converter. Owing to this restriction, the loss of one control possibility as compared with hard switching has to be accepted.
This is only achieved if the polarities of the driving commutation voltage v_K or the commutated output current i_L are reversed between two identical commutation processes.

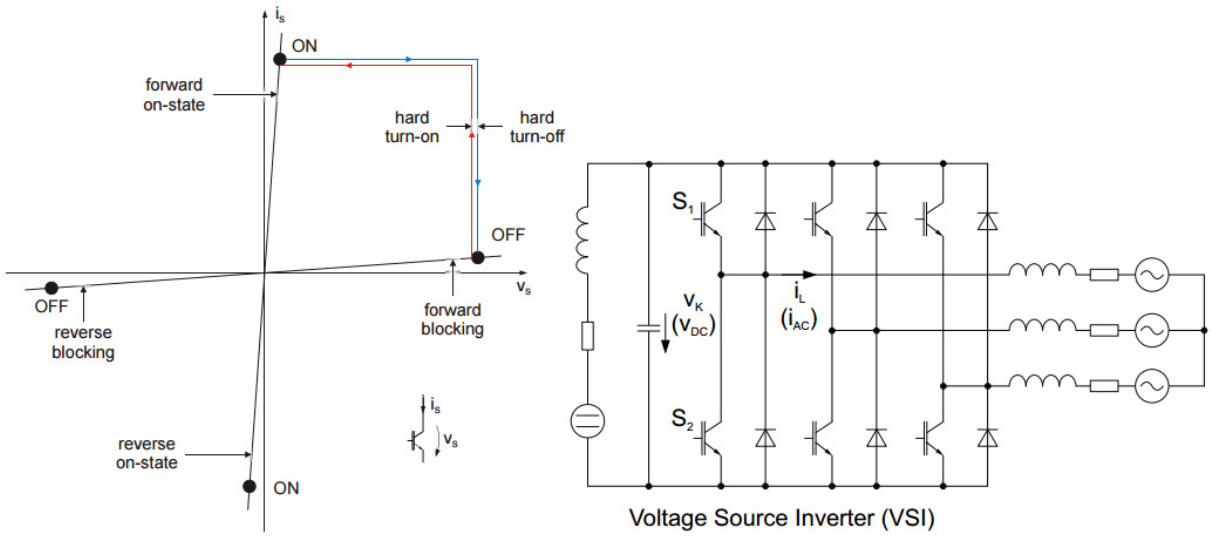


Figure 9.8.2 Operating point characteristic of switch current and voltage for hard switching (IGBT, MOSFET) and typical circuit diagram for voltage source inverter

The IGBT, MOSFET and diodes available today were developed and optimised almost exclusively for hard switch applications and display comparable features for this area of application (Figure 9.8.2).

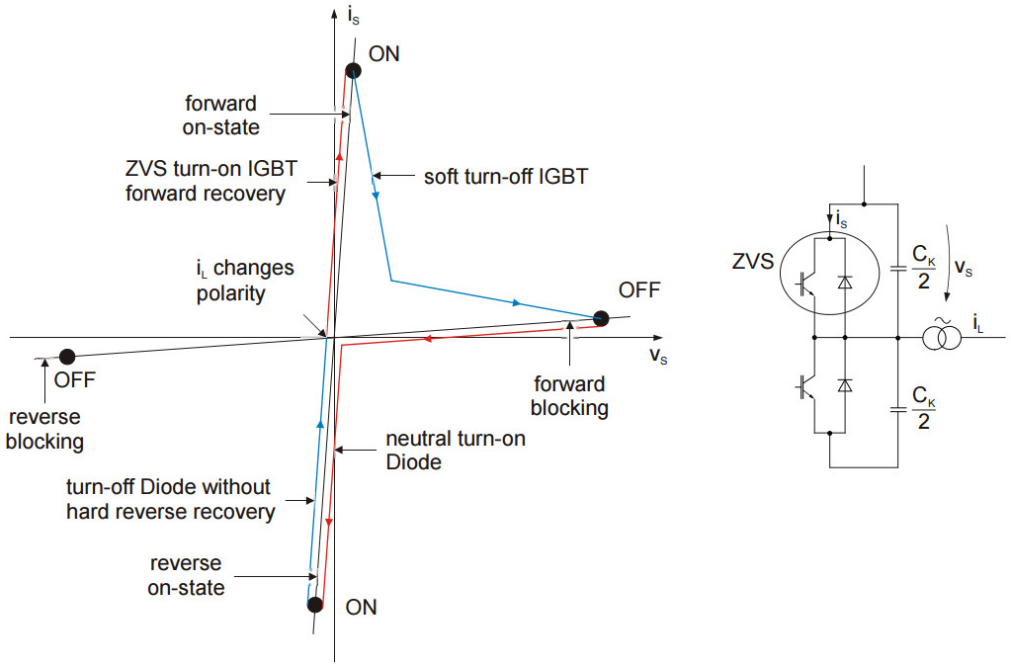


Figure 9.8.3 Operating point characteristic of switch current and voltage during soft / resonant switching as ZVS

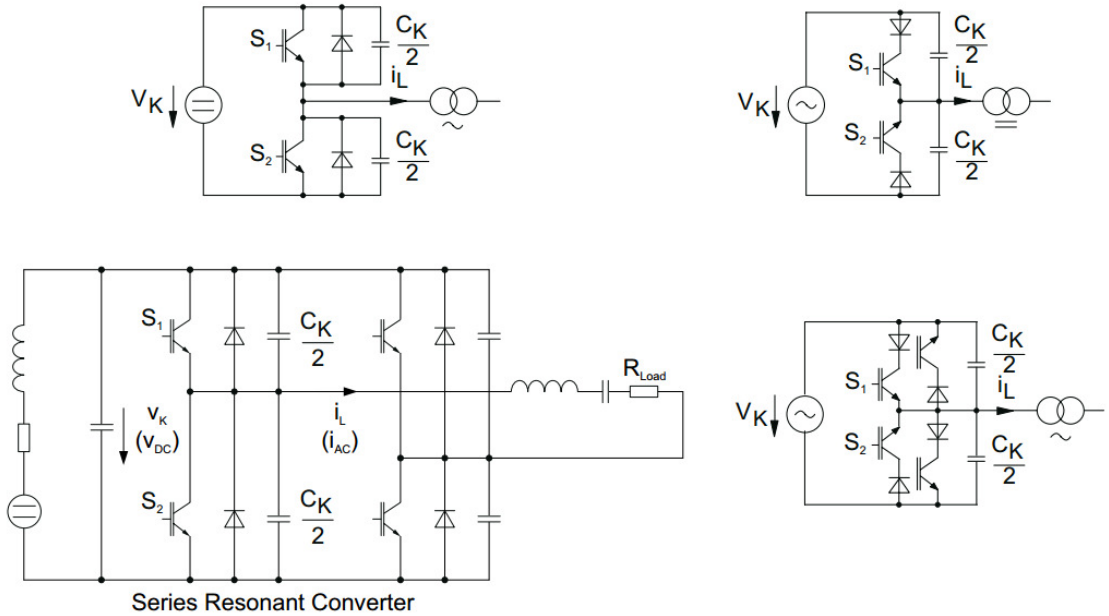


Figure 9.8.4 Sample circuit diagrams for commutation circuits with ZVS and a series resonant converter

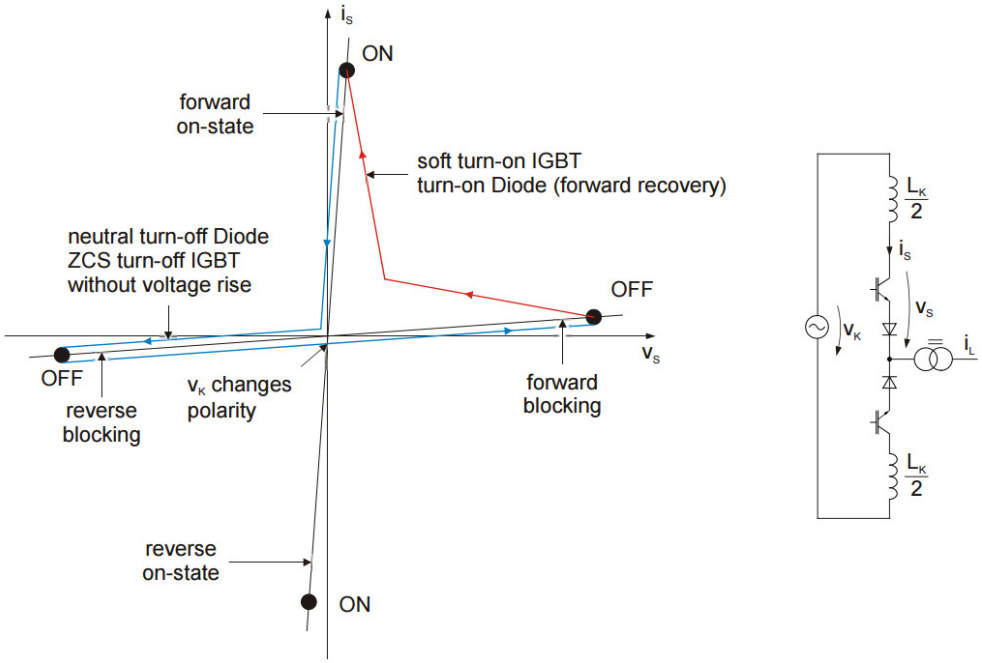


Figure 9.8.5 Operating point characteristic of switch current and voltage during soft / resonant switching as ZCS

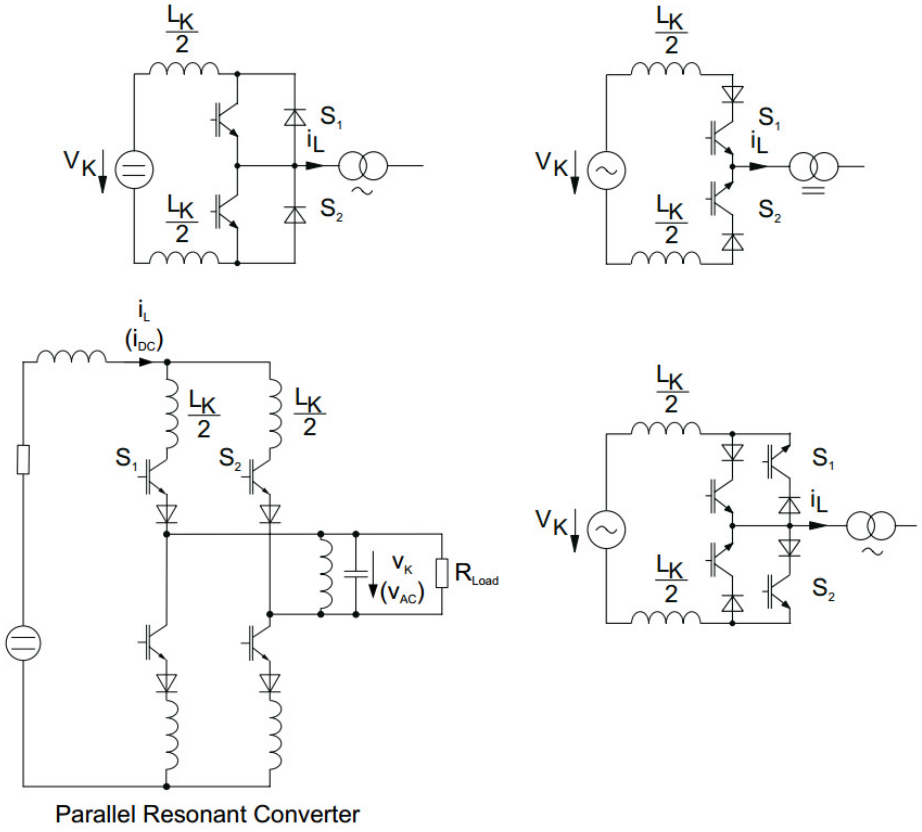


Figure 9.8.6 Sample circuit diagrams for commutation circuits with ZCS and a parallel resonant converter

A comparison of the track of the operating points in Figure 9.8.2, Figure 9.8.3 and Figure 9.8.5 shows that the area encircled by the track is different in size. The area is a relative measure of the power losses that occur during switching. During hard switching (Figure 9.8.2) the area is at its maximum. In the case of ideal resonant switching, the track of the operating point would go along the axes of the coordinate system. In real resonant or quasi-resonant switching and commutation processes, the resulting path will lie somewhere between the two aforementioned ideal conditions (Figure 9.8.3 and Figure 9.8.5).

9.8.3.2 Semiconductor and driver requirements for ZVS

Power semiconductors:

- have to feature active turn-off and demonstrate good power-loss reduction behaviour during turn-off
- For IGBT:
  - short charge carrier lifetime and low tail charge
  - low dependence of tail charge and charge carrier lifetime on the junction temperature
  - low forward turn-on overvoltage during conductivity modulation during zero-voltage turn-on with impressed di/dt
- Since ZVS-diodes do not turn off with reverse-recovery di/dt and take on reverse voltage at the same time, the requirements for reverse-recovery behaviour are not as strict as for hard switching topologies.

Driver circuit:

The driver circuit has to comply with the following minimum requirements:

- active IGBT / MOSFET turn-off and
- switch voltage monitoring and passive turn-on of ZVS at $v_S \approx 0$ V.

Modified ZVS mode:

The duration of a capacitive commutation process can be approximated as follows:

$$t_{Kc} = \frac{C_K \cdot v_K}{i_L}$$

C_K: Commutation capacitance (power loss reduction capacitance)
v_K: Commutation voltage
i_L: Load current to be commutated

With low load currents, the commutation process in power converters may last an undesirably long time, impairing circuit function. This can be avoided by using modified zero voltage switches, which will abruptly end the commutation process after a variable maximum commutation time by active turn-on towards the not yet fully recharged commutation capacitance. This can, however, result in increased switching losses.
Figure 9.8.7 shows the principle behind a modified ZVS.

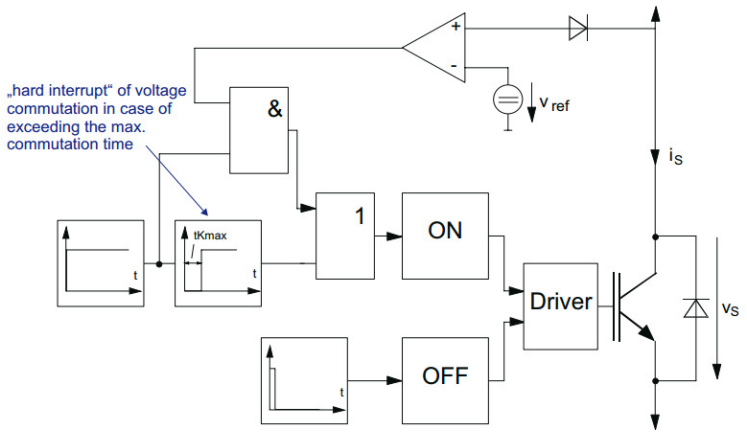


Figure 9.8.7 Modified ZVS: basic principle

9.8.3.3 Semiconductor and driver requirements for ZCS

Power semiconductors:

- have to feature active turn-on and demonstrate good power-loss reduction behaviour during turn-on
- should have low internal capacitance
- For IGBT:
  - short charge carrier lifetime
  - low dependence of storage charge and tail charge on the junction temperature
  - short dynamic saturation phase during turn-on
- Diodes: Low reverse recovery charge (Q_{rr}, t_{rr})

Driver circuit:
The driver circuit has to comply with the following minimum requirements:

- active IGBT / MOSFET turn-on and
- switch current monitoring and passive turn-off of ZCS at $i_S \approx 0$ A.

Modified ZCS mode:
The duration of an inductive commutation process can be approximated as follows:

$$t_{Ki} = \frac{L_K \cdot i_L}{v_K}$$

L_K: Inductance in the commutation circuit (power loss reduction inductance)
v_K: Commutation voltage
i_L: Load current to be commutated

At low commutation voltages or high load currents, the commutation process in power converters may last an undesirably long time, impairing circuit function. This can be avoided by using modified zero current switches, which will abruptly end the commutation process after a variable maximum commutation time by active turn-off towards the live commutation inductance. This can, however, result in increased switching losses. In connection with this, please note that in many applications zero current switches have to feature overvoltage protection.
Figure 9.8.8 shows the principle behind a modified ZCS.

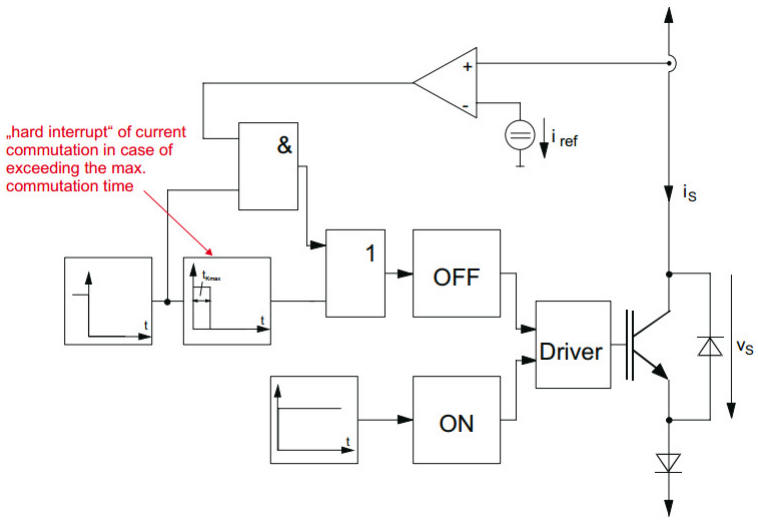


Figure 9.8.8 Modified ZCS: basic principle

9.8.3.4 Switch properties

ZVS during zero-voltage turn-on with impressed di/dt

Before the IGBT is able to conduct a current, it has to be turned on by the driver. Since conductivity modulation within the n-base will not have taken place before the current is taken up, the IGBT will react to the di/dt-impression with a transient increase in on-state voltage and, consequently, increased on-state losses for this time interval (forward recovery). Dynamic overvoltage, the duration of conductivity modulation and, hence, power dissipation depend mainly on the basic doping of the n-base, emitter efficiency, charge carrier lifetime, di/dt, final switch current value (load current) and temperature.
If the ZVS short circuit protection is based on v_{CE} measurement and evaluation, this protection has to be blanked out during di/dt impression to prevent the converter from being turned off due to the error message.

Active, soft turn-off (cf. Figure 1.1.14 in chapter 1)

During active soft IGBT turn-off, current can commutate directly to the parallel capacitance C_K with reduced collector-emitter dv/dt, resulting in reduced switching losses. The tail current characteristic, i.e. the discharge of charge stored in the IGBT after MOSFET channel blocking, is determined substantially by the collector-emitter dv/dt. Increasing the commutation capacitance will lower the initial tail current value (comparable to a capacitive current divider between IGBT and

snubber capacitor). At the same time, the tail current will be prolonged, impairing the reduction of turn-off losses.

ZVS with MOSFET

The unipolar MOSFET must not be charged or discharged with any storage charge. This results in the following specifics for use in ZVS applications:

- There is no dynamic forward overvoltage during zero-voltage turn-on with impressed di/dt.
- Within the same device rating class, the comparison with IGBT shows that turn-off switching losses in MOSFET with commutation capacitances of some nF are virtually non-existent. The relatively high output capacitance of MOSFET supports the turn-off loss reduction.
- The process where the off-state transistor is subject to high $\frac{dv_{DS}}{dt}$ is critical for MOSFET; in ZVS mode this process does not exist (cf. chapter 9.5 Driver). That is why, in principle, MOSFET may be driven by negative gate-source voltage in this case.

Fast diodes in ZVS

In ZVS operation, diodes will not turn off with reverse-recovery di/dt and take up reverse blocking voltage at the same time. The reverse-recovery behaviour of fast diodes is therefore negligible compared to hard switching.
Having said that, optimum dynamic turn-on is still required in ZVS applications. In relation to this, CAL diodes offer particular advantages.

ZCS with MOSFET

Since MOSFET do not feature dynamic saturation, MOSFET with very small (...1µH...) series soft switch inductances can almost be fully relieved of turn-on losses.
The high output capacitance of MOSFET, however, has a negative impact on the turn-on losses. If high switching frequencies are used (>50kHz), the resulting share of power losses has to be factored in to the total power losses.
Due to the unipolarity of MOSFET there will be no removal of residual storage charge during change of polarity of the switch voltage at the end of hold-off time. The relatively high output capacitance, in contrast, has to be recharged.

Fast diodes in ZCS

In ZCS mode, diodes turn off with reverse-recovery di/dt and take up reverse blocking voltage at the same time. Due to the existing commutation inductances, current will be commutated in the diodes at a lower speed than in hard-switching converters (lower reverse current peak, reduced turn-off losses). Nevertheless, the need for very good dynamic turn-off behaviour hand in hand with low turn-off losses prevails.
In addition, the use of fast diodes as series diodes of IGBT or MOSFET in ZCS mode calls for very good dynamic turn-on behaviour of the diodes (forward recovery).

9.8.3.5 Conclusion

The behaviour of power semiconductors during hard switching is not applicable to soft switching. In principle, components with a shorter charge carrier lifetime are more suitable for soft-switching applications due to the aforementioned dynamic processes. Generally speaking, the information on power electronic components specified in existing datasheets is not suitable for evaluating dynamic behaviour in ZVS and ZCS topologies.
Owing to the great variety of low-loss converter topologies with their own specific switch requirements, a general conclusion on the limitation of frequencies of IGBT and MOSFET switches cannot be drawn.

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10 Handling, Insulation and Environmental Influences

10.1 Mounting of power modules

10.1.1 Requirements on the heatsink mounting surface

To achieve a good interconnection between power module and heatsink and to obtain an optimum heat transfer, the heat sink must comply with the following specifications, illustrated in the example in Figure 10.1.1. The heatsink surface finish requirements are given in the respective "Mounting Instructions" for each product line.

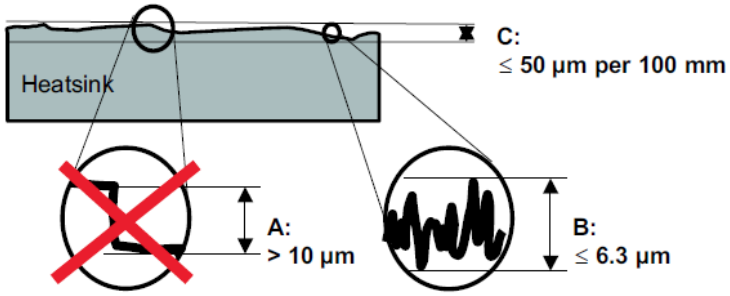


Figure 10.1.1 Mounting surface specifications for Semikron Danfoss power modules (example)

- The heatsink must be clean and free from residues, particles or dust
- Steps: no steps > 10µm
- Roughness R_z: ≤ 6.3µm for modules without and ≤ 10µm with baseplate (DIN EN ISO 4287)
- Planarity: ≤ 50µm on 100mm (DIN EN ISO 1101)

Due to the remaining unevenness of the mounting surfaces and the bending of the modules surface, a gap is left between module and heatsink when mounting a power module onto a cooling surface. With a specific thermal conductivity of $\lambda_{air} \approx 0.03 W/m \cdot K$, air is a poor conductor of heat. The gap therefore has to be filled with a more effective thermal conductor, a **T**hermal **I**nterface **M**aterial (TIM).
Please refer to chapter 5.3 for more detailed information on the properties and application of TIM materials and the modules available by Semikron Danfoss with pre-applied thermal pastes and phase changer materials.
The steps are limited to avoid the risk of cracks in the insulating ceramic. A lower roughness does not necessarily reduce the $R_{th(c-s)}$ as the roughness holds the TIM material in place and allows a good contact to the filler material of the TIM. Planarity required so that the gaps can be filled with the recommended layer thickness of the TIM material. To avoid unnecessary strain and tension of the baseplate or DBC ceramic, the heatsink has to be sufficiently stiff and has to be distortion free during assembly and transportation.

10.1.2 Mounting of power modules onto heatsink

The power module has to be placed on the matching heat sink area and then all mounting screws have to be uniformly tightened with the specified mounting torque in the recommended screw mounting sequence and in several steps with increasing tightening torques ("preload torques" to "final torque M_s"). Details on the mechanical dimensions of the fasteners, tightening sequences and torques are provided in the "Mounting Instructions" and "Technical Explanations".
Semikron Danfoss recommends the use of steel screws acc. ISO4762 of strength category 8.8 in combination with a DIN 125 washer or combined screw-and-washer assemblies to secure the modules. Setting devices such as spring washers will increase the elasticity, reduce settling effects as well reduce mechanical stress. To comply with creepage and clearance distances it is suggested to check the resulting distances according to the relevant standards (EN 50178, IEC 61800-5-1) when selecting a screw type. An overview of the mounting torque ranges M_s gives Table 10.1.1 but should be crosschecked with the datasheets.

Product Line	Module construction	Mounting screws	
		Screw Diameter	Mounting torque M_s [Nm]
SEMITRANS 2/3/4	Baseplate modules	M6	3...5
SEMITRANS 10/10+		M5	4...6
SEMITRANS 20		M6	4...6
SEMiX 2s/3s/4s/5/13s/33	Baseplate modules	M5	3...5
SEMiX 3p/6p		M5	3...6
SKiM 4/5	Baseplate-less modules	M5	2...3
SKiM 63/93		M4	3.15...3.85
SEMITOP 1	Baseplate-less modules	M4	1.35...1.65
SEMITOP 2		M4	1.8...2.2
SEMITOP 3		M4	2.25...2.75
SEMITOP 4		M4	2.47...2.6
SEMITOP E1/E2		M4	1.6...2.3
MiniSKiiP 0/1/2/3	Baseplate-less modules	M4	2<Ms<2.5
SEMIPACK 1/2/3/4/5	Baseplate modules	M5	4.25...5.75
SEMIPACK 6		M6	5.1...6.9
SEMIPONT 1	Baseplate modules	M5	2
SEMIPONT 2/3		M5	4.25...5.75
SEMIPONT 4	Baseplate-less modules	M6	4.25...5.75
SEMIPONT 5		M4	2.25....2.5
SEMIPONT 6		M4	2.55...3.45

Table 10.1.1 Mounting of Power Modules: Recommended screw diameters and permitted mounting torque ranges

An example of the mounting of a module with a particularly large footprint is shown in Figure 10.1.2.

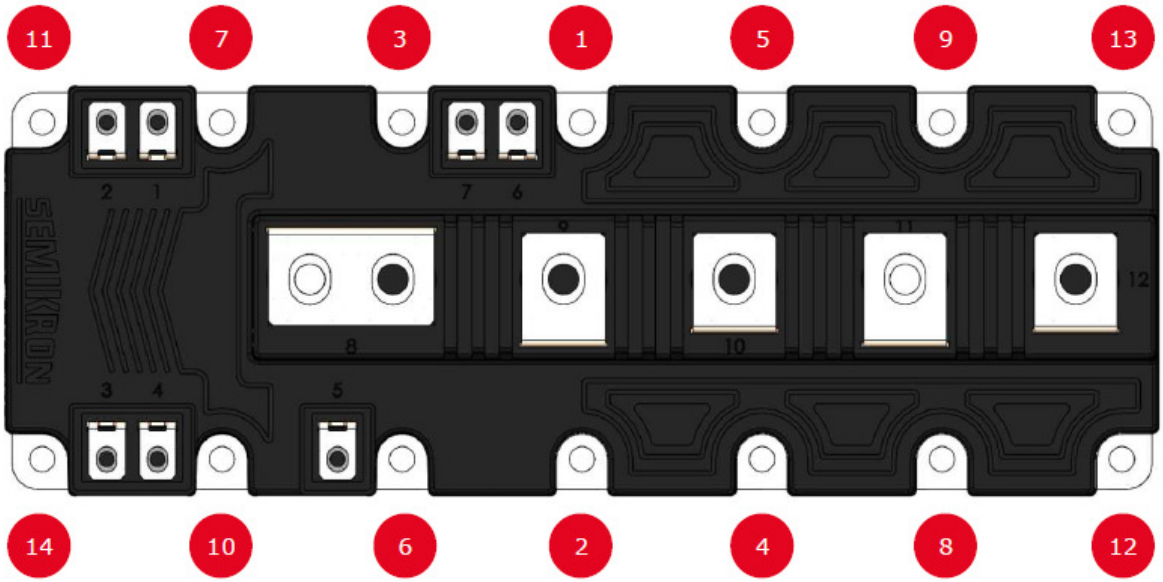


Figure 10.1.2 Recommended mounting sequence of a SEMITRANS 10 IGBT module [10.1]

10.1.3 Electrical connections

10.1.3.1 Notes for connecting screw terminals

The terminals for screw connections are built from copper often with a nickel coating. The following recommendations are valid for copper busbars, bare or with suitable plating. The module must be connected within the permissible module tolerances specified in the outline drawings in the respective data sheet. The position and tolerance of adjacent components such as PCBs, DC link, mounting bolts or cables have to be defined in such a manner, that after the connection no sustained effect on the static and / or dynamic tensile forces are exerted to the terminals.
Power modules must not be used as part of the mechanical construction. It is recommended to have a construction which leaves the power and auxiliary terminals permanently free of mechanical stress during operation. To achieve this in a wide temperature range it is advised to add suitable spacers. It must be ensured that the direction of the force always acts towards the direction of the base plate. Static forces in other directions as well as exposure to vibration and / or thermal expansion should be avoided.
Moreover, SKiiP and SKiM pressure contact IGBT modules run the risk of inadmissible relief of the pressure contacts if the effective forces are exceeded due to unsuitable connections. The definition of the terminal forces is shown in Figure 10.1.3 on the example of a SEMITRANS 10 module.

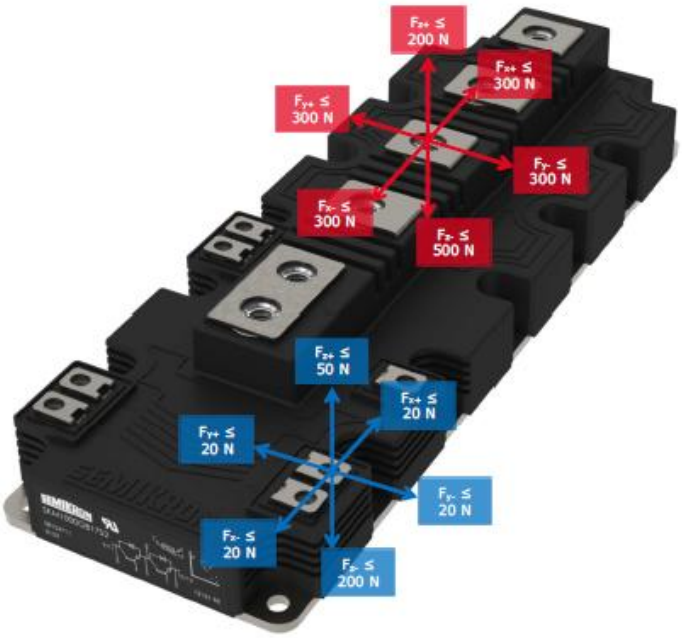


Figure 10.1.3 Maximum permitted mechanical forces at the terminals of a SEMITRANS 10 IGBT module [10.1]

The maximum permitted mechanical forces on all screw terminals as well as the mounting torque ranges M_t, and the screw-in depth limits, details on connection elements and further instructions are provided in the given "Mounting Instructions" and "Technical Explanations. Table 10.1.2 illustrates screw diameters, permitted mounting torque ranges and terminal forces of electrical connections for selected Semikron-Danfoss power modules.

Product Line	Power Terminal connection screws					Auxil. Terminal connection screws				
	Screw dia-meter	Mounting torque M_t [Nm]	F_x F_y [N]	F_{z+} [N]	F_{z-} [N]	Screw dia-meter	Mounting torque M_t [Nm]	F_x F_y [N]	F_{z+} [N]	F_{z-} [N]
SEMITRANS 2	M5	2.5…5	not speci-fied	200	250	Fast-On connectors			60	60
SEMITRANS 3	M6			250	200				60	60
SEMITRANS 4	M6			250	250	M4	1.1…2.0	n. spec.	150	250
SEMITRANS 10/10+	M8	8…10	300	200	500	M4	1.8…2.1	20	50	200
SEMITRANS 20	M8	9…11	<100	<100	500	M3	0.9…1.1	<100	<100	<100
SEMiX 2s/3s/ 4s/13s/33/5	M6	2.5…5	100	100	500	Spring-, Solder- or Press-Fit terminals				
SEMiX 3p	M6	3…6	200	200	800					
SKiM 4/5	M6	4…5	<100	<100	<100	Spring terminals				
SKiM 63/93	M6	6…8	100	100	<100					
SKiiP 3/7 (AC)	M8	13…15	<100	<100	<100	Plug connectors				
SKiiP 3/7 (DC)	M8	6…8	<100	<100	<100					
SKiiP 4 (AC)	M8	13…15	300	200	<100					
SKiiP 4 (DC)	M8	6…8	300	200	<100					
SEMIPACK 1	M5	2.55…3.45	not specified			Fast-On connectors				
SEMIPACK 2	M6	4.25…5.75								
SEMIPACK 3	M8	7.65…10.35								
SEMIPACK 4	M10	14.45…19.55								
SEMIPACK 5	M10	10.2…13.8								
SEMIPACK 6	M12	16.2…19.8								

For explanation of F_x, F_y, F_{z+}, F_{z-}: see graphical representation in Figure 10.1.3

Table 10.1.2 Diameters, permitted mounting torque ranges and terminal forces of electrical connection screws

The DC-side power connection of IGBT and MOSFET modules should be realized using symmetrically arranged DC link busbars to ensure minimum stray inductance, thus minimising switching overload. To avoid parasitic oscillations, pulse-proof low-inductance film capacitors are attached to the DC terminals in most applications (e.g. collector TOP-IGBT / emitter BOT-IGBT). Principally, the connection path between driver terminals and driver circuit must be as short as possible to minimise stray inductances, electromagnetic interferences and oscillations. This is particularly important in IGBT and MOSFET modules. Cable connections (e.g. gate and emitter connection cables) are to be twisted where possible; parallel arrangement of driver cabling and power busbars must be avoided at all cost. For more detailed explanations of these requirements, please refer to chapter 9.2.

10.1.3.2 Notes for connecting spring contact terminals

All terminals of MiniSKiiP modules respective the auxiliary terminals of SEMiX spring and SKiM modules are connected to the PCB using contact springs. Consequently, electrical load (also for testing purposes) must be applied to these power modules only after proper connection to the PCB.

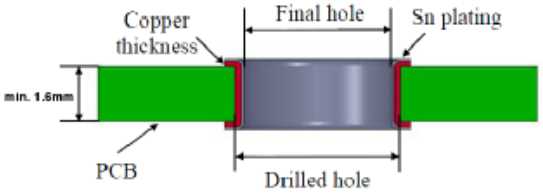
The following key requirements apply to PCBs:

- PCB material, e.g. FR4
- Conductor thickness in compliance with IEC 326-3
- Tried and tested PCB surface finishes for the conductors' pads: electroless nickel immersion gold (Ni Au) with > 5µm Ni, hot air levelling tin (HAL Sn), chemical tin (chemical Sn), tin / lead (Sn Pb)
- Due to the intrinsic instability of passivated finishes, Semikron Danfoss does not recommend the use of PCBs with organic solderability preservatives coating (OSP) finish for the conduction pads.

- Overall low-inductive layout (where possible +/- coplanar conductor paths with maximum Cu surface, gate and emitter conductor paths in parallel and as close to each other as possible)
- Contact pads with no vias and free of solder resists, solder flux, contamination, oil or other substances (if a no-clean flux is used, PCB cleaning can be omitted).
- No inadmissible tin bulges which might neutralize the spring effect (if required, a cover should be used during flow soldering process)
- Compliance with EN 50178 - A7.1.8.5, e.g. use of press-in bushes to connect the power terminals to the PCB in order to avoid contact problems due to PCB material flow

10.1.3.3 Notes for connecting Press-fit terminals

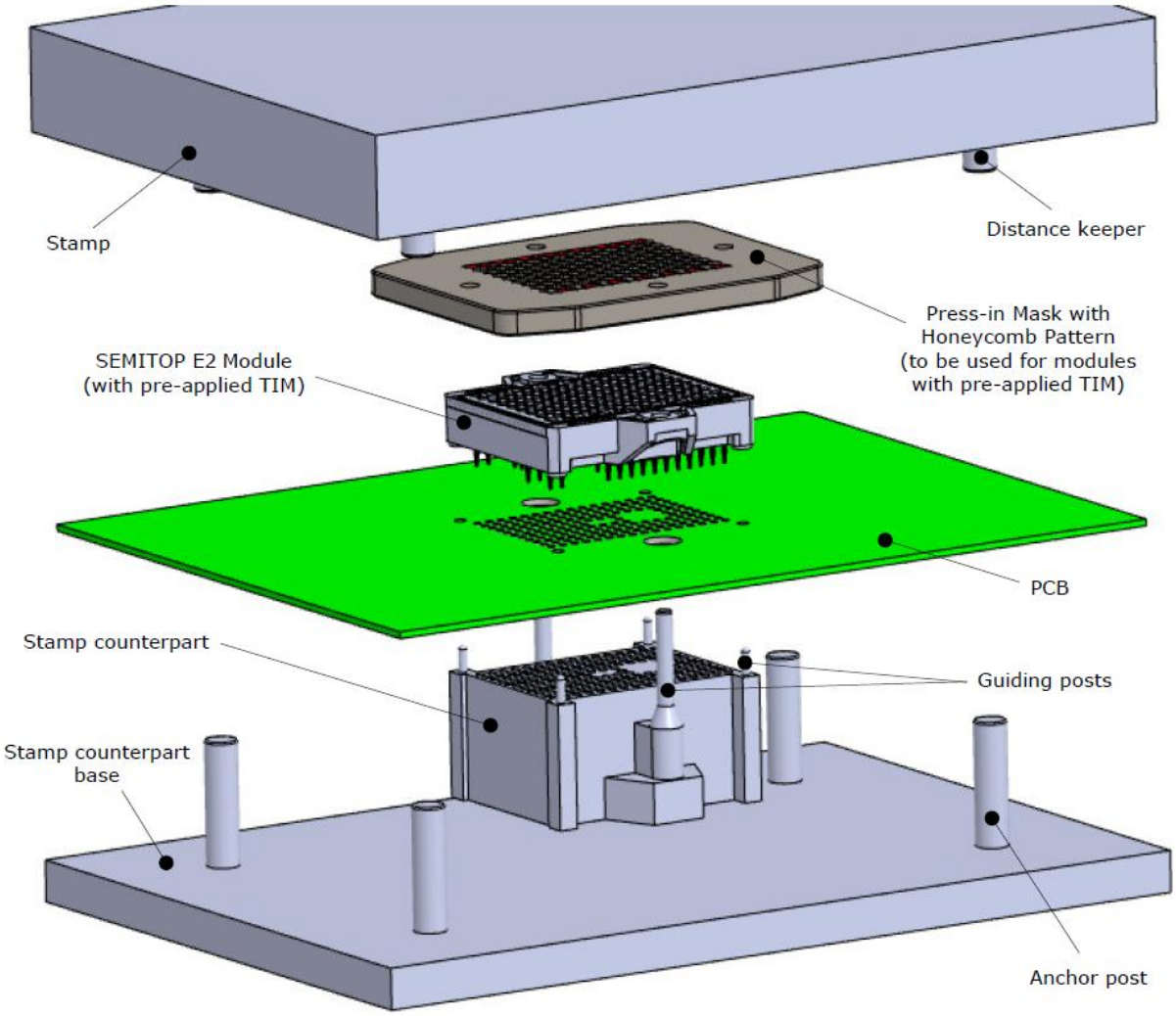
The main principle of the press-in technique is the bigger latitude of the press-in zone than of the PCB hole. By the press-in process a plastic deformation of the pin results, ensuring a gas-tight and low-ohmic resistance. Only small insertion forces are necessary with high holding forces at the same time.
To press a single pin into the PCB requires a force in the range of 35N to 70N, depending on the hole diameter. With holes at the lower limit of the specified tolerance (see Table 10.1.3) or several modules mounted at the same time press-in forces may be higher. The upper limit of the press has to be adjusted to 100N per pin, to avoid damage of the module respectively the pin.



	SEMiX 3p/5/6p SEMITOP E1/E2	SEMITOP 2p/3p/4p
Drilled hole diameter [mm]	1.125...1.175	1.575...1.625
Copper thickness in via [µm]	25...50	25...50
Final hole diameter (chemical tin) [mm]	1.02...1.09	1.47...1.54
Final hole diameter (HAL tin and Ni/Au) [mm]	0.94...1.09	1.39...1.54
Cu width of the annular ring [µm]	100	100
Minimum thickness of PCB [mm]	1.6	1.6

Table 10.1.3 Specification of plated through holes for the press-in process of Semikron Danfoss power modules

Particular attention must be paid for SMD components that need to be placed close to the module pins. A minimum distance of 4mm is required between the edge of these components and the centre of the plated through holes in order to get enough space for the pressing tool. For a successful press-in process with high process capability, it is recommended to use equipment that allows control of relevant process parameters like force and distance. In principle, Semikron Danfoss recommends servo electric presses to mate PCB and Press-fit modules. The Figure 10.1.4 shows a concept view of the equipment for press-in SEMITOP E1/E2 modules.



Picture is an example only and should not be intended as a proven design.

Figure 10.1.4 Schematic view of a setup for press-in SEMITOP E1/E2 modules [10.2]

For modules with pre-applied Thermal Interface Material (TIM), in order to prevent from any damage of the TIM layer, a "press-in mask with honeycomb pattern", like ones shown in [10.1], should be used. To ensure a proper press-fit contact, the centre of the Press-fit pin head has to be at least 0.5mm below the top surface and at least 0.5mm above the bottom surface of the PCB (see Figure 10.1.5).

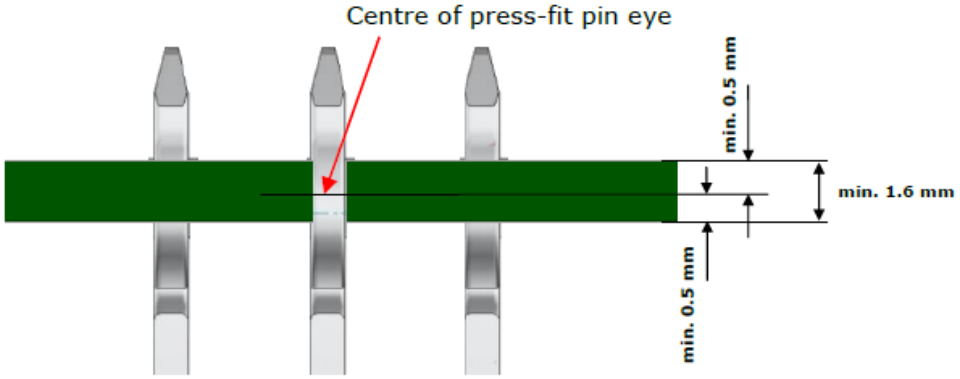


Figure 10.1.5 Press-fit zone [10.2]

The following specifications are given for press-in process of SEMITOP E1/E2 modules [10.2]:

- Press-in force (min…typ….max, per terminal): 40Nm…60Nm…100Nm
- Press-in speed (min…typ….max): 25mm/min*…50mm/min…600mm/min

(*) minimum value according to IEC 60352-5)

A typical force vs. distance profile for a press-in process is shown in Figure 10.1.6.

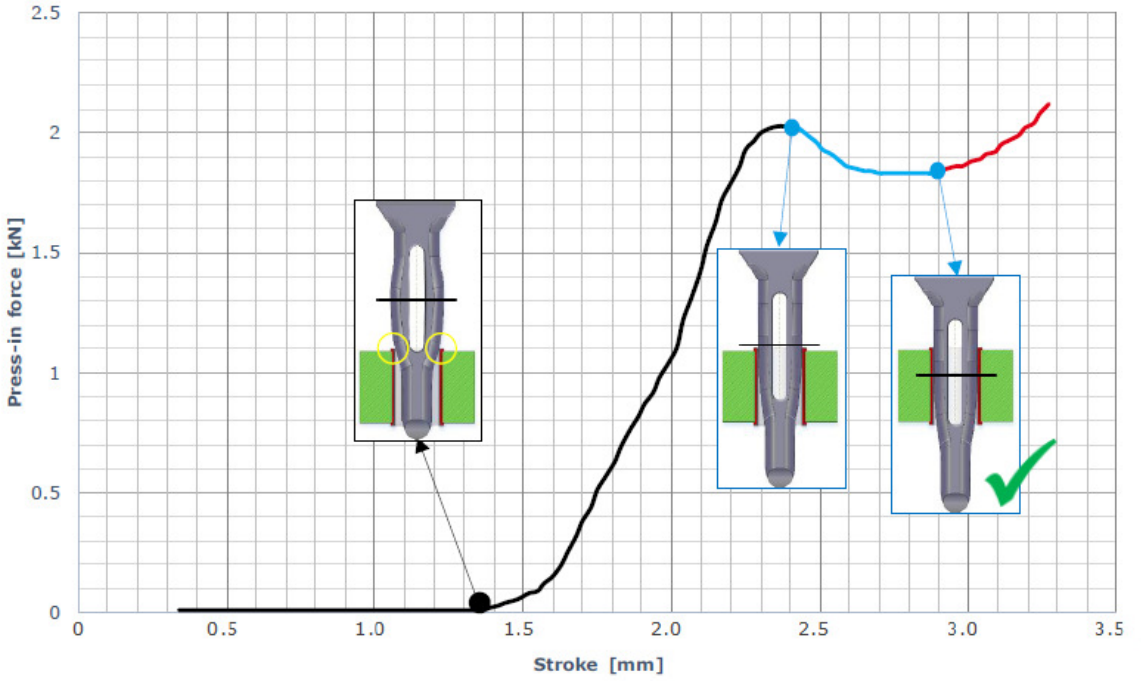


Figure 10.1.6 Typical press-in profile of a 32 pins module [10.2]

There are three main sections describing the typical press-in process (valid only for the first insertion):

- Black curve: The Press-fit terminal slides into the holes and will be deformed to fit the holes. Here, maximum deformation of Press-fit terminal occurs.
- Blue curve: The pin heads are fully inserted into the holes and slides to the final position
- Red curve: third section. Sliding of the pin is stopped. The mounting post get in contact with the PCB and they start to bend the PCB. The press-in process has to be stopped at the beginning of the red curve in order to prevent from PCB damaging.

Multiple modules can be assembled onto the same PCB. In this case, it is recommended to press modules all at once. Press-in tool must be designed in order to fulfil minimum requirements, given for the single module tool, and has to ensure the correct levelling of the modules and PCB to avoid mechanical stresses.
A detailed guidance to the press-in process is given in [10.2], for example. It also contains information on how pressed-in modules can be removed from the PCB (press-out process).
In principle, the Press-fit pins are also suitable for soldering. In case the Press-fit pin shall be soldered already in first use, the recommendation for the PCB-holes differs from the dimensions listed in Table 10.1.3, see Figure 10.1.7

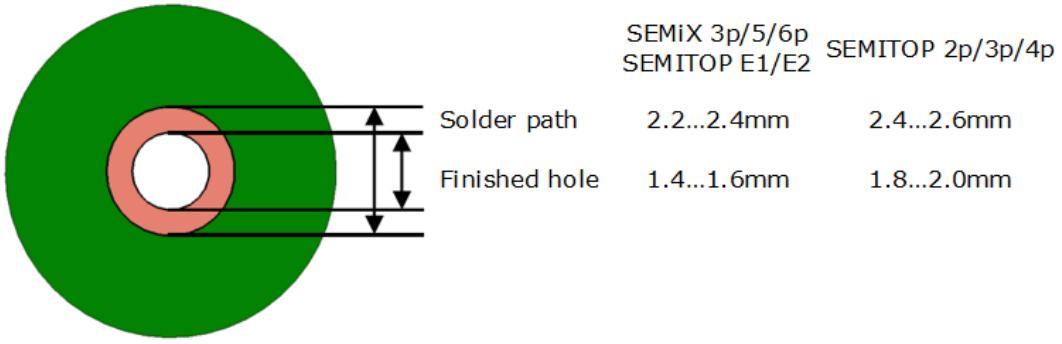


Figure 10.1.7 Recommended PTH-diameters for soldering of Press-fit pins

If the module is to be connected for a second time, i.e., if the Press-fit function has already been used, the PCB needs to be soldered to the power module.

10.1.3.4 Notes for connecting solder terminals

All Semikron Danfoss power modules with solder connectors are suitable for using the most common soldering processes:

- Hand iron soldering
- Wave soldering
- Selective soldering

Information on the requirements for reliable solder connections between the power module and the PCB soldering instructions can be found in the module datasheets and, for example, in the "Mounting Instructions" [10.2] and [10.3] for SEMITOP modules.

Hand iron soldering

For the hand soldering process of solderable SEMITOP modules, Semikron Danfoss suggests not to exceed the maximum temperature of 260°C of the joint for a maximum soldering time of 10 seconds, especially when several pins must be soldered on large tracks or thick (>100um) copper planes (IEC-EN 60068-2-20). To reduce the effort during soldering, especially at large copper tracks or copper planes, it is recommended to provide the PCB's plated through holes with specific thermal reliefs (Figure 10.1.8).



Figure 10.1.8 Plated through holes (PTH): a) without thermal relief b) with thermal relief [10.2]

Wave soldering

For the wave soldering process, the IEC60068-2-20 it is used as reference. It is recommended to follow the wave soldering profile of Figure 10.1.9. Temperature and time restrictions listed in Table 10.1.4, must be observed.

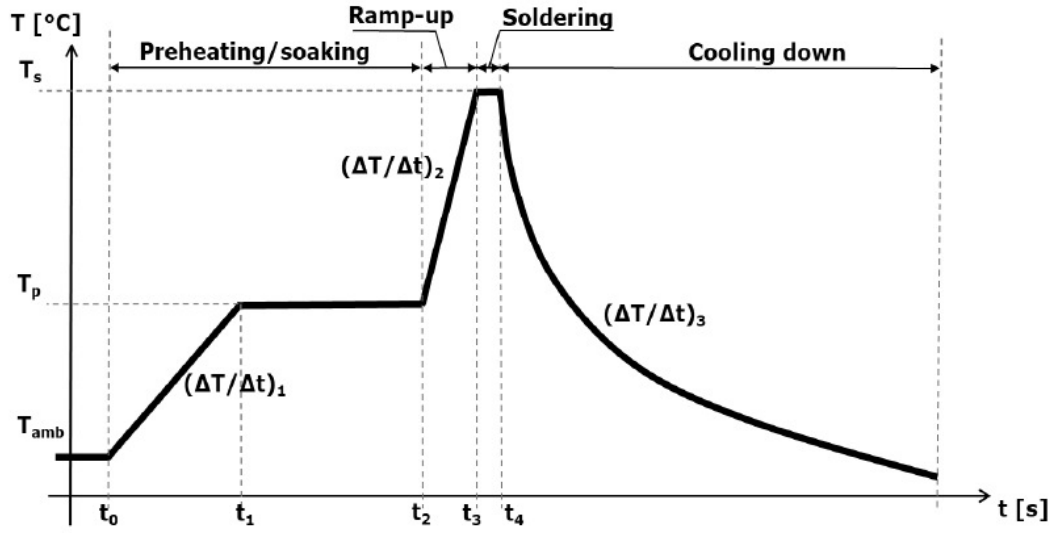


Figure 10.1.9 Wave soldering profile for SEMITOP modules [10.2], [10.3]

Soldering step	Time frame	Temperature at solder joint			Temperature gradient			Time at max. temperature
		Reference temperature	typ. [°C]	max. [°C]	Reference gradient	typ. [K/s]	max. [K/s]	max. [s]
Preheating/ soaking	t_0…t_1	T_{amb}	20	25	$(\Delta T/\Delta t)_1$	1	3	-
	t_1…t_2	T_p	95	125	-	-	-	100
Ramp-up	t_2…t_3	T_s - T_p	-	-	$(\Delta T/\Delta t)_2$	3	*)	-
Soldering	t_3…t_4	T_s - T_p	-	260	-	-	-	10
Cooling down	> t_4	-	-	-	$(\Delta T/\Delta t)_3$	-4	-6	-

*) High ΔT/Δt values might endanger integrity of the ceramic substrate so maximum gradient must be defined via design of experiment and verified by insulation tests.

Table 10.1.4 Wave soldering parameters for SEMITOP® modules

10.2 Sensitivity to ESD and measures for protection

10.2.1 ESD sensitivity of power modules with IGBT or MOSFET

ESD (**E**lectro**s**tatic **d**ischarge) is a rapid, spontaneous transfer of charge carriers induced by a high electrostatic field through a spark between two objects at different electrostatic potentials as they approach one another.
ESD can change the electrical characteristics of a semiconductor device, degrading or destroying it. ESD may also upset the normal operation of an electronic system, causing equipment malfunction or failure. Therefore, ESD is one of the most serious problems in the electronics industry and, if sufficient countermeasures are not taken, can affect production yields, manufacturing costs as well as the product quality and reliability [10.4].

Explanations of the three basic mechanisms of charge carrier generation and transfer

- Charging by Friction or Delamination (Triboelectric Charging)
- Charging by Electrostatic Induction
- Contact Charging

can be found, for example, in chapter 3.5.1 of [10.5].

In general, all power modules with IGBT, silicon or silicon carbide MOSFET are sensitive to ESD due to their thin gate insulation (gate oxide layer). This is why they are classified as Electrostatic Sensitive Devices which are prone to damage by electrostatic fields or electrostatic discharge during routine handling, testing and transportation.

10.2.2 Measures for ESD protection

When handling IGBT or MOSFET power modules, the regulations set down in the standard IEC 61326, must be adhered to. For labelling purposes, the manufacturer must place a warning label in accordance with IEC 60417-1 [10.6], Reg. No. 5134 to the packaging of electrostatically sensitive components (Figure 10.2.1).



Figure 10.2.1 Warning label for ESD packaging [10.6]

IGBT or MOSFET power modules and gate driver produced by Semikron Danfoss are supplied with gate and emitter / source terminals short-circuited by conductive ESD protection blisters, suitable packaging lined with conductive foam or rubber mats, self-sealing metal foils, with annular rivets on the terminals or caps on the connectors. If possible, this short circuit should not be removed until connecting the gate. Figure 10.2.2 shows two examples of ESD protective packaging.



a) b)

Figure 10.2.2 ESD packages: a) SEMITRANS 10 ESD protection blister with ESD marking tape; b) Gate driver PCB in its ESD protection packaging bag with ESD warning label

Inspection and further processing by customer must always be carried out by suitably clothed staff (static protective overalls, shoes and gloves, grounded wrist strap on a grounded workplace as well as static protective seats and static protective floor materials.
Before ESD-sensitive components are processed, all transportation and assembly equipment, as well as PCBs must be adjusted to the potential of the ESD-sensitive components, and electrostatic re-charge must be prevented. All staff should be trained suitably for correct ESD handling.

10.3 Coordination of insulation and high voltage testing

10.3.1 General

When selecting a power module, the user must be aware of the expected electrical and environmental conditions, as these conditions are essential for insulation coordination. Therefore, in addition to selecting the right voltage class for the power modules, the following requirements must also be analysed, to check if the modules creepage and clearance distances fit to the application:

- Maximum conductor-to-conductor AC supply voltage or highest DC supply/DC link voltage
- Grid configuration of the supply network (determines the maximum voltage between earth potential and the input terminals)
- Mains overvoltage category (see Table 10.3.1 below)
- Maximum altitude of application (see Table 10.3.2 below)
- Circuit-dependent insulation requirements for sensors and isolation barriers to control circuits, e.g. sensors connected to a mains circuit: Functional insulation will be sufficient, sensor connected to a SELV or PELV circuit: Protective separation between the load terminals of the power module and the sensor is required.

Coordination of insulation is to correlate the types and the realization of the insulation for each potential within the converter and find out the minimum requirements like distances or test voltages what the relevant standard requests. The rules to be followed bring the voltage stress requirements for electrical insulation given from the application in line with the necessary insulation withstand capability based on the experience of international standards (see chapter 10.3.4 below). The content of the chapters 10.3.1 to 10.3.5 and all tables were derived from the Semikron Danfoss Application Note AN1405 "Coordination of Isolation" Rev. 03, 2017 [10.7], which also contains calculation examples for two different applications. Please refer to it for more detailed information.

10.3.2 Categories of insulation

The coordination of insulation differs between three categories of insulation subject to their purpose. They must fulfil hierarchically graded requirements:

- *Functional insulation* isolates different potentials within a circuit and takes purely functional, but no safety-relevant aspects into account.
- *Basic insulation* separates grid-supplied circuits from earthed exposed parts and is thus vital for safety. A breakdown of the insulation does not result automatically in a danger of life due to the earthing of the exposed parts.
- *Protective separation* realized by reinforced or double (2 · -basic) insulation separates grid supplied circuits from unearthed exposed parts, on the one hand, and from control circuits, if they are directly connected to other control circuits which have exposed components. No further protection is provided for equipment users. A breakdown of this insulation could be fatal because the unearthed exposed parts can be shifted to the grid voltage. This is the reason why stricter requirements must be fulfilled.

10.3.3 Realisation of insulation

10.3.3.1 Clearance in air

The air space between conductive parts is called clearance. It must be so large that flashover is prevented at all times if voltage is applied. The determining factors for this are the highest peak voltage present and the dielectric strength of the ambient air. The peak voltage is considered by the overvoltage category of the equipment energized from grid (see below). The overvoltage category level is the degree for the expected overvoltage. In special protected circuits expected voltages are lower (= low category level) than in circuits where lightning strike can occur (= high category level). The four existing categories are described in all insulation standards with slightly different explanations but the same meaning.

Overvoltage Category (OVCAT)	Description
1	Equipment connected to a circuit where measures have been taken to reduce transient overvoltages to a low level
2	Equipment not permanently connected to the fixed installation
3	Equipment permanently connected in fixed installations (downstream of, and including, the main distribution board)
4	Equipment permanently connected at the origin of an installation (upstream of the main distribution board)

Table 10.3.1 Overvoltage categories according to IEC 61800-5-1 [10.8]

The installation altitude has a high impact on the dielectric strength of the air due to the decreasing air pressure. If the installation altitude is >2000m above sea level, the required clearance must be enlarged by an altitude correction factor which is given in IEC 60664-1, table A2. The standard does neither forbid nor permit interpolation for altitudes between the lines of the table. It is usual and it makes physically sense to interpolate.

Altitude [m]	Normal barometric pressure [hPa]	Multiplication factor for clearance
2000	800	1.00
3000	700	1.14
4000	620	1.29
5000	540	1.48
6000	470	1.70
7000	410	1.95

Table 10.3.2 Altitude correction factor according to IEC 60664-1, table A2 [10.9]

10.3.3.2 Creepage

Pollution on the surface of insulating material can create a conductive path across it. The length of this conductive part is called creepage length, creepage track or simply creepage. Dirt, salt, water

and the applied voltage have an impact on the length of the conductive path. The level of pollution and the resistance of the materials used with regard to the surface currents determine the dimensioning of the creepage. The environmental conditions correlate to four degrees of pollution.

Pollution degree (PD)	Description
1	No pollution or only dry, non-conductive pollution occurs. The pollution has no influence.
2	Normally, only non-conductive pollution occurs. Occasionally, however, a temporary conductivity caused by condensation is to be expected, when the device is out of operation. Some standards like EN50124-1 expect temporary conductivity caused by condensation in operation also.
3	Conductive pollution or dry non-conductive pollution occurs, which becomes conductive due to condensation, which is to be expected.
4	The pollution generates persistent conductivity caused, for example by conductive dust or rain or snow.

Table 10.3.3 Pollution degrees

The resistance of the insulating material is described by the comparative tracking index (CTI). It is determined by increasing a test voltage until a specified leakage current will flow in a defined test setup. The more resistant a material is, the higher the CTI-value and the shorter the creepage track may be. Insulating materials are classified in five CTI groups.

CTI group	CTI level	Example
0		Inorganic materials like glass or ceramic which do not track
1	≥600	Plastic material like PE-HD (polyethylene) or PTFE (polytetrafluoroethylene)
2	400…599	Printed circuit board (PCB) base material FR4 type KF
3a	175…399	Glass-filled PCB material FR4
3b	100…174	Foil material polyimide (e.g. Kapton) or resins (e.g. phenolic)

Table 10.3.4 Comparative tracking index (CTI) groups [10.8]

The damaging effect of creepage currents is a long-time issue. What is decisive here is the RMS value of the applied voltage, not its peak value. The period for the calculation of the RMS voltage is for this reason at least the cycle time of the application.
The phase shift between the first harmonic of the voltages must be considered by adding RMS-voltages. Often the shift is unknown or only identifiable with high effort. This is why the worst case is considered and the quadratic sum of voltages is used:

$$V_{1,3} = \sqrt{V_{1,2}^2 + V_{2,3}^2}$$

$V_{1,2}$, $V_{1,3}$, $V_{2,3}$: RMS connector voltages (phase to phase)

On the other hand, this means that the resulting sum of voltages is sometimes no conclusive.
The minimum creepage lengths required in standards were mostly determined empirically, with the tracking resistance of printed circuit boards (PCB) determined only for voltages up to 1000V and pollution degrees 1 and 2 in experimental setups, with the results adopted as a requirement. This is why the required distances here are much smaller than the CTI of the PCB material would actually require.
The minimum creepage is at least the clearance. This is why the creepage length must be at least as large as the clearance in air. For inorganic insulating materials like glass or ceramic, which do not track, the creepage distance may equal the associated clearance.

10.3.3.3 Solid insulation

Solid insulation is insulation not created solely by air or gas. Some standards require minimum material thicknesses, do not accept coating as insulation material or have special requirements for PCBs. It is not possible to generalize the demands and the relevant product standard must be checked. To verify if the solid insulation withstands the voltage load, three tests can be performed:

- Impulse withstands voltage test
- AC or DC voltage test
- Partial discharge test

Ideally, the partial discharge inception voltage is higher than the maximum peak voltage to be expected because then partial discharge will never occur. The partial discharge extinction voltage must be higher than the continuously present voltage because when partial discharge starts it must be safely interrupted again. Some standards require a partial discharge test for protective separation insulation only. It is permitted to perform the tests on the component rather than on the equipment.

10.3.4 Standards

10.3.4.1 European and international standards

High voltage equipment (AC >1000V or DC >1500V) and low voltage equipment (AC ≤1000V or DC ≤1500V) must be considered separately. Both have their own basic standards with fundamental requirements. For high voltage equipment connected to the grid, it is IEC 60071-1 and for low voltage equipment, it is IEC 60664-1.
Product standards and product group standards usually refer back to these basic standards so the requirements for all equipment are broadly independent of the used standard. There are some typically applied standards for the coordination of insulation of converters. Standards for equipment not connected to the grid are normally not based on the named basic standards. They occasionally demand severe requirements for the insulation, e.g. IEC 50124-1 for railway applications.

Standard	Description	Valid as
IEC 60071-1	Insulation coordination – Definitions, principles and rules basic standard	basic standard
IEC 60664-1	Insulation coordination for equipment within low-voltage ystems - principles, requirements and tests	basic standard
IEC 50178	Electronic equipment for use in power installations	product group standard
IEC 62477-1	Safety requirements for power electronic converter systems and equipment – general	product group standard
IEC 61204-7	Low voltage power supplies, d.c. output – safety requirements	product standard
IEC 61800-5-1	Adjustable speed electrical power drive systems – safety requirements – electrical, thermal and energy	product standard
IEC 62040-1	Uninterruptible power systems (UPS) – general and safety requirements for UPS	product standard
IEC 62109-1	Safety of power converters for use in photovoltaic power systems - general requirements	product standard
IEC 50124-1	Railway applications - insulation coordination - basic requirements - clearances and creepage distances for all electrical and electronic equipment	product standard

Table 10.3.5 Selection of European standards for the coordination of insulation [10.7]

10.3.4.2 UL standards

In general, coordination of insulation for UL is not based on IEC- or EN-standards. The requirements differ considerably for this reason. If a UL-approval for equipment is intended, the coordination of insulation will be done twice: One time for European/international standards and one time for UL. The UL basic requirements for the insulation are established for phase-to-ground rated system voltages up to 1500V in the UL-standard UL 840. The requirements of various UL

product standards are established on this basic standard or they allow using the insulation requirements of this basic standard alternatively.
Most UL-standards do not allow differing between functional and basic insulation what most times results in higher clearances within the circuit in comparison to the IEC- and EN-standards. Normally equipment designed according to IEC- and EN-standards only does not fulfil the UL insulation requirements.

Standard	Description	Valid for	Note
UL840	Insulation coordination including clearances and creepage distances for electrical equipment	basic standard	
UL 508A	Industrial control panels	product standard	UL 840 can be used alternatively
UL 1741	Inverters, converters, controllers and interconnection system equipment for use with distributed energy resources	product standard	UL 840 can be used alternatively
UL 61800-5-1	Adjustable Speed Electrical Power Drive Systems – Part 5-1: Safety Requirements – Electrical, Thermal and Energy	product standard	no alternative use of UL 840

Table 10.3.6 Selection of UL standards for the coordination of insulation [10.7]

UL 61800-5-1 has replaced UL 508C. Since 2016, UL 61800-5-1 is used for determining the insulation coordination of new products. UL 508C was withdrawn in 2020. A summary of the significant differences between UL 61800-5-1 and UL 508C is available on the UL-homepage [10.12].
UL 61800-5-1 is similar but not the same as IEC 61800-5-1. Significantly different are e.g. the spacings at the field wiring terminals of a drive. UL 61800-5-1 requests here higher distances. Please refer to the foreword of UL 61800-5-1 for a list of the differences [10.11].

10.3.5 High voltage testing

10.3.5.1 General

The electrical industry's standards for protection against electrical hazards result in safety requirements for design and production, the fulfilment of which must be assessed by means of appropriate tests. The most important tests include high-voltage (or isolation-) tests. In this context, it is important to distinguish between type tests and routine tests. The content of the chapter 10.3 and all tables were derived from the Semikron Danfoss Application Note AN 16-002 “High voltage testing”, AN 16-002, Rev. 04, 2024 [10.13].

10.3.5.2 High voltage type test

The proof of the design is done in a conformance (type) test. A high voltage is used to verify that the clearances and solid insulation of components have adequate dielectric strength to resist expected overvoltage conditions [10.8]. It also shows that the equipment is able to work safely over its complete lifetime. During the test the electrical stress on the insulation over its entire lifetime is simulated in a very short time. Here it is assumed that the failure mechanism at the end of life is the same as in the test. Using an empirical equation, the lifetime stress is transferred to a test condition [10.14], [10.15].

$$V^{n}_{\text{operating voltage}} \cdot T_{\text{lifetime}} = V^{n}_{\text{test voltage}} \cdot T_{\text{test time}}$$

This empirical equation is used in some standards to determine the conditions for a high voltage type test using an exponent of n = 6. Typically, the test voltage is calculated for an expected lifetime of 20 years. So, equipment with an operating voltage of 230V has to be high voltage tested with a voltage of 3400V for one minute.
This also means that the tested insulation is maybe aged completely during the type test and cannot be used anymore. Therefore, samples from high voltage type tests have to be scrapped or at least not be used if the safety of the user will be affected.

10.3.5.3 High voltage routine test

The test conditions of a type test therefore cannot be used in a routine test. It is not the goal of a routine test to check if the equipment design is suited for the expected electrical stress on the insulation. Routine tests are carried out only to verify that clearances and solid insulation have not been reduced or damaged during the manufacturing operations or weak materials were used. To make sure that all insulation-related production failures can be excluded the high voltage routine test is done when production is completed and the equipment does not need to be reopened again. The test is not carried out to verify the insulation of the elementary components and also the creepage distances [10.16].
The specification of a routine test must be strong enough that safety-relevant failures are detected but only minimum ageing of the device occurs. Typical routine test specifications show that less than 0.000001% of the lifetime are aged by the test under the assumption that the empiric equation from chapter 10.3.5.2 is valid.
A high voltage test in the converter assembly is a repetition of an already performed routine test in the power module production line. The voltage level for the second test shall take into consideration that the high voltage test affects the quality of the insulation. Several standards recommend reducing the voltage to 80% [10.8] or 85% [10.16], [10.17] of the first test level. High voltage tests with component data sheet values shall be avoided as well as routine incoming inspection tests.

10.3.5.4 Test conditions

Normally the high voltage test is performed with a sinusoidal AC voltage at 50Hz or 60Hz. If the circuit contains capacitors the test may be performed with a DC voltage equal to the peak value of the specified AC voltage. The DC voltage test is not fully equivalent to the AC. voltage test due to the different withstand characteristics of solid insulation for these types of voltages [10.9]. The polarity of the test voltage has an impact on the flashover voltage. For DC tests it is necessary to check both polarities [10.14].
The DC high voltage test is advised for production facilities. A DC current is less risky for the human heart in case of an accident. Additional workplace safety measures are not needed during high voltage testing with AC up to 3mA and DC up to 12mA [10.19]. The DC high voltage test, thus, has the advantage that no extra precautions are required for tests of 12mA or less. If the current is higher a special test room or a sealed off area with warning light and two-handed operation is required in many countries.
A few standards request specified ambient conditions for the high voltage test. Typical values are 15°C to 35°C ambient temperature, 45% to 75% relative humidity and an air pressure of 860hPa up to 1060hPa.

10.3.5.5 Tested insulation

Test samples can contain several circuits which may be galvanically isolated from each other. The insulation within and between these circuits is categorized in “functional”, “basic” and “reinforce or double basic insulation” (10.3.2). The high voltage test is applied only on the latter two safety-relevant insulation, non-safety-relevant functional insulation is not tested by the high voltage test.

10.3.5.6 Test procedure

Most standards for electrical equipment demand the following conditions for the test:

- External terminals of the circuit shall be connected together.
- Switchgear and controls within equipment shall be in the closed position or bypassed.
- Terminals of voltage blocking components (such as rectifier diodes) shall be connected together.

It is mandatory to connect all test sample terminals of the same circuit with each other for the high voltage test.
If the test sample consists of more circuits which are isolated from each other with basic insulation or protective separation it will be necessary to test all circuits to all adjacent circuits plus earth. Non earthed conductive parts that can be touched are separate circuits by definition. Circuits with the same test voltage can be connected and tested together. However more than one high voltage test may be necessary for the test sample.
The connection of circuits may be different for type and routine tests if they require different test voltages, explained in more detail in [10.13] using the illustrations in Figures 1 to 3 there. Surge

protective devices must be disconnected before high voltage testing. If capacitors with high capacitance are parallel to the parts between where the test voltage needs to be applied, it may be difficult, or even impossible, to perform the AC voltage test because the charging current would exceed the capacity or current set point of the voltage tester. In the latter case, those parallel capacitors could be disconnected before testing. If this is also impossible, DC testing can be taken into consideration [10.9].
An Overview of the general requirements for the high voltage test of the most relevant standards for power electronics is given in Table 1 of [10.13].

10.3.5.7 Test voltage level

The voltage level in the high voltage test is determined by the operating voltage of the equipment. For this the grounding of the connected grid is important. In a star grounded (TN) grid the voltage stress for the insulation is lower (e.g. 230V in a 3-phase system with 400V line-to-line voltage) than in a corner grounded grid with the same line-to-line voltage (here 400V).
The AC test voltage levels for basic insulation in equipment connected to a star grounded grid are shown in Table 10.3.7 according to the most relevant standards for power electronics. Also given are the levels for type tests and routine tests for typical grid voltages. Before choosing the voltage level check in the latest edition of the relevant standard if the given voltages are still valid.

Standard	**Formula for test voltage calculation**	**230V+10%**		**480V+10%**		**690V+10%**	
		Type	Routine	Type	Routine	Type	Routine
EN 50124-1 [10.24]		1390V	1200V	2680 V	1900V	3320 V	2800V
EN 50178 [10.22]	1.5·V + 750V	1133V		1470V		1900V	
IEC 60664-1 [10.9]	-	2065V		3482V		5222V	
IEC 61287-1 [10.16]	$2 \cdot V_{peak}/\sqrt{2}$ + 1000V	1506V		1610V		1880V	
IEC 61439-1 [10.17]	-	-	2000V	-	2500V	-	3000V
IEC 61800-5-1 [10.11]	V + 1200V	1453V		1505V		1640V	
IEC 62040-1 [10.20]	same as IEC 62477-1						
IEC 62109-1 [10.10]	V + 1200V	1453V		1505V		1640V	
IEC 62477-1 [10.23]	V + 1200V	1453V		1505V		1640V	
UL 1557 [10.18]	specified isolation voltage of product						
UL 1741 [10.26]	2·V + 1000V	1460V		1960V		2380V	
UL 61800-5-1 [10.11]	-	1460V	-	1960 V	-	3553 V	-

Table 10.3.7 High voltage test AC RMS voltage levels for basic insulation of equipment for star grounded grids, derived from several standards [10.13]

The voltage level spread between the standards is wide (more than a factor of 3). The goal of the semiconductor module manufacturer is to specify the isolation rating of the modules so high that it matches the requests of all relevant standards. This is much higher what most applications need. Test voltage levels for safety insulation can differ from these values considerably. In general, they are higher for the type test (Table 10.3.8).

Standard	230V+10%		480V+10%		690V+10%	
	Type	Routine	Type	Routine	Type	Routine
EN 50124-1 [10.24]	2210V	1200V	3673V	1900V	4812V	2800V
EN 50178 [10.22]	1133V		1470V		1900V	
IEC 60664-1 [10.9]	4130V		6964V		10444V	
IEC 61287-1 [10.16]	1506V		1610V		1880V	
IEC 61439-1 [10.17]	-	2000V	-	2500V	-	3000V
IEC 61800-5-1 [10.11]	2906V	1453V	3010V	1505V	3280V	1640V
IEC 62040-1 [10.20]	same as IEC 62477-1					
IEC 62109-1 [10.10]	2906V	1453V	3010V	1505V	3280V	1640V
IEC 62477-1 [10.23]	2906V	1453V	3010V	1505V	3280V	1640V
UL 1557 [10.18]	specified isolation voltage of product					
UL 1741 [10.26]	1460V		1960V		2380V	
UL 61800-5-1 [10.11]	2906V	-	3010V	-	3280V	-

Table 10.3.8 High voltage test AC RMS voltage levels for protective separation of equipment for star grounded grids, derived from several standards [10.13]

Power modules have no integrated protective separation. The test levels given here are therefore only relevant for equipment testing. The test voltage must be increased continuously to the maximum level within a minimum time period. Some standards define this time, e.g. 5s minimum time [10.9], [10.24].

10.3.5.8 Test failures

Different words are used in the standards for defining the various failure modes:

- An electrical breakdown is a failure of insulation under electrical stress when the discharge completely bridges the insulation, thus reducing the voltage between the electrodes almost to zero [10.8].
- Disruptive discharge: passage of an arc following dielectric breakdown [10.21]
- Sparkover: disruptive discharge in a gaseous or liquid dielectric [10.21]
- Flashover: disruptive discharge over the surface of a solid dielectric surrounded by a gaseous or liquid medium [10.21]
- Puncture: disruptive discharge through a solid dielectric [10.21]

The failure criteria for the high voltage test vary in the different standards. The test is considered successfully passed if:

- No disruptive discharge (sparkover, flashover or puncture) occurs [10.9]. A leakage current that is monitored during the test is not exceeded.
- No breakdown [10.18] or insulation breakdown [10.8] occurs.

Due to these differences the failure criteria of the application relevant standard must be taken into account. A general failure criterion is not defined.

10.3.5.9 Kinds of high voltage testing

Impulse voltage test

The impulse voltage test is intended to simulate overvoltage of atmospheric origin. It also covers overvoltage due to switching of equipment. The test is successfully passed if no puncture, flashover, or sparkover occurs [10.8]. It is used to verify that the clearances and solid insulation of components have adequate dielectric strength. Advantage of this test is the very short test time that minimizes the electrical stress for the insulation. This prevents any ageing effect on the component.
Solid insulation has a different withstand characteristic compared to clearance if the time of stress is increased. In general, the withstand capability will be decreased significantly. Therefore, the high voltage test, which is specified for the verification of the withstand capability of solid insulation, is not allowed to be replaced by an impulse voltage test. The impulse voltage test is not able to check if the insulation of components will work safely during the complete lifetime as in the high voltage type test. Exclusively the impulse voltage test will detect unintended insulation weaknesses as well as the high voltage routine test.

Partial discharge test

The partial discharge test must confirm that the solid insulation used in components and subassemblies remains partial-discharge-free with the specified voltage range [10.8]. Partial discharges in clearances which do not result in breakdown are disregarded [10.9]. This test does not detect sparkover and the test level is normally lower than overvoltage that can be expected from atmospheric origin.
Partial discharge tests for solid insulation must be specified if the applied peak value exceeds 700V and if the average field strength is higher than 1kV/mm [10.9].

Insulation resistance test

The measurement of the insulation resistance is done to evaluate the general condition of the insulation. It is normally made during regular maintenance and any additional ageing effect from testing should be prevented. The measurement result gives an indication of ageing of the insulation by comparison with previous results (over a period of years) but no hint to weaknesses in the isolation system. Reduced clearances of equipment and consequential flashovers are not tested here due to test voltages being far below expected overvoltage of atmospheric origin.

10.4 Environmental conditions for storage, transportation and operation

10.4.1 General

This chapter refers to the classification and description of environmental conditions according to IEC 60721-3-x (Classification of environmental conditions including Part 3-0 (introduction), Part 3-1 (storage), Part 3-2 (transportation and handling), Part 3-3 (stationary use at weather-protected locations). Other parts of this standard are not covered here, such as Part 3-4 (stationary use at non-weather-protected locations), Part 3-5 (ground vehicle installations), Part 3-6 (ship environment), and Part 3-7 (portable, non-stationary installations). The terms and definitions given in IEC 60721-1 "Classification of environmental conditions - Part 1: Environmental parameters and their severities" apply here as well.
As illustrated in Figure 10.4.1, devices containing power modules (or discrete power semiconductors) are exposed to many different kinds of environmental stress, which are summarised accordingly in the environmental conditions stipulated in IEC 60721-3-x.

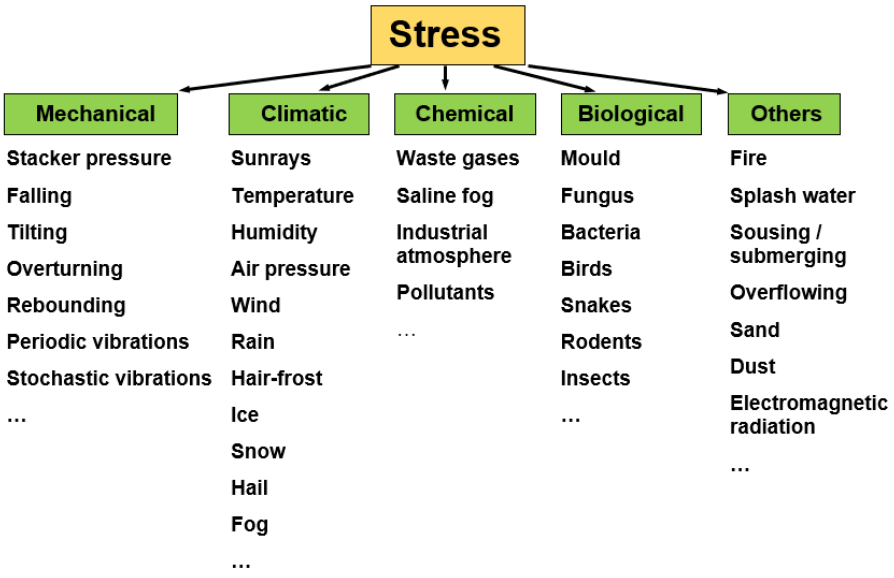


Figure 10.4.1 Environmental stress factors during storage, transportation/handling and operation as per IEC 60721-3

Environmental conditions which can be then expected to occur in the field application must be factored in during the development and construction of electronic devices already. This also includes the selection of suitable power modules or discrete semiconductors, as well as its cooling and assembly.

Consequently, in order to comply with the environmental provisions determined by application specifics, operating location, the conditions of storage and transportation to the final place of use, as well as conditions during down-time, the selection of components on the basis of environmental conditions is to be iteratively combined with design measures for protection from environmental impacts.

Several classes for climatic conditions (K), special climatic conditions (Z), biological conditions (B), mechanically active substances (S), and mechanical conditions (M) are specified. For a given location or product environmental conditions are categorised as a total set of classes according to the "**nAXY**" environmental classification code:

The first digit (n) identifies the area of application that the requirements defined by the subsequent digits apply to:
n: 1: Storage
2: Transportation and Handling
3: Operation

The first capital letter (A) determines the type of environmental quantity the limits refer to:
A: K: Climatic conditions
Z: Special climatic conditions
B: Biological conditions
S: Mechanically active substances
M: Mechanical conditions

The third and fourth digit (XY) determine the limits of the environmental quantity under A:
XY: Numbering (in ascending order by degree of severity)

The classes defined in previous versions of IEC 60721-3 - frequently mentioned in previous chapters and datasheets only used 1 digit (x) in the third position. These designations have been replaced by new classes that better reflect the environmental conditions. The actual classes use used 2 digits (XY) in the third and fourth position.
Usually, higher degree classes include the requirements of lower degree classes. In addition, assembly, maintenance and repair conditions are to be taken into account, insofar as these are likely to deviate from the storage and operating conditions.

10.4.2 Operating conditions for electrical devices in stationary, weather-protected use

10.4.2.1 Climatic conditions

Climatic conditions include air temperature, absolute and relative air humidity, condensation, rate of temperature change, barometric pressure, solar and heat radiation, air movement, water from sources other than rain and ice/frost formation. The following descriptions of the climate classes comply with the original formulations in IEC 60721-3-3:

Class 3K20 (formerly 3K1): Enclosed, fully air-conditioned locations. Air temperature and humidity control is used continuously to maintain the required conditions.

Class 3K21 (formerly 3K2): Enclosed locations with continuously temperature control. Humidity is not normally controlled. Heating, cooling or humidification is used where necessary to maintain the required conditions, especially where there is a large difference between them and the open-air climate. Installed products may be exposed to secondary effects of solar radiation due to increased ambient temperature and to heat radiation. They may also be exposed to movements of surrounding air due to draughts in buildings, for example through open windows, or due to special process conditions.

Class 3K22 (formerly 3K3): Temperature controlled, enclosed locations. Humidity is not controlled. Heating or cooling is used to maintain the required conditions, especially where there is a large difference between them and the open-air climate.

Class 3K23 (formerly 3K4): Enclosed locations having no temperature or humidity control. Heating may be used to raise low temperatures, especially where there is a large difference between the conditions of this class and the open-air climate. Installed products may be subjected to formation of ice.

Class 3K24 (formerly 3K5): Enclosed locations having neither temperature nor humidity control. The location may have openings directly to the open air. The climatic conditions of this class may be affected to a varying extent by the conditions of the open-air climate and the construction of the building. Installed products may be subjected to formation of ice.

Climatic parameter	Unit	3K20	3K21	3K22	3K23	3K24
Low air temperature	°C	+20 [4)]	+15	+5	-5	-25
High air temperature	°C	+25	+32	+40	+55	+55
Low relative humidity [1)]	%	20	10	5	10	5
High relative humidity [1)]	%	75	75	85	10	5
Low absolute humidity [1)]	g/m²	4	2	1	0.5	0.5
High absolute humidity [1)]	g/m²	15	22	25	29	29
Rate of change of temperature [2)]	°C/min	0.1	0.5	0.5	0.5	0.5
Low air pressure [6)]	kPa	70	70	70	70	70
High air pressure [6)]	kPa	106	106	106	106	106
Solar radiation [7)]	W/m²	no	500	700	700	700
Heat radiation	-	no	[5)]	[5)]	[5)]	[5)]
Movement of surrounding air [3)]	m/s	0.5	1.0	1.0	1.0	5.0
Condensation	-	no	no [8)]	no [8)]	yes	yes
Water from sources other than rain	-	no	no [8)]	no [8)]	dripping water	dripping water
Formation of ice and frost (including freezethaw)	-	no	no [8)]	no [8)]	yes	yes

Table 10.4.1 Classification of climatic conditions (from table 1 of IEC 60721-3-3)

Remarks

[1)] The low and high relative humidity severities are limited by the low and high absolute humidity and high and low temperature. The extreme severities of relative humidity, absolute humidity and temperature cannot occur simultaneously (see annex A of IEC 60721-3-3
[2)] Averaged over a period of time of 5 min.
[3)] A cooling system based on non-assisted convection may be disturbed by adverse movement of surrounding air.
[4)] These are air-conditioned locations with a tolerance of ±2 °C on the stated temperature value.
[5)] Conditions occurring at the location concerned to be selected from table 2 of IEC 60721-3-3
[6)] If applicable, a special value may be also selected from table 2 of IEC 60721-3-3.
[7)] Secondary effects from the solar radiation behave as heating effect.
[8)] Limited to no occurrence of condensation.

10.4.2.2 Mechanical environmental conditions

Figure 6.2.2 illustrates the various types of mechanical stress listed in the environmental conditions in accordance with IEC 60721-3-3.

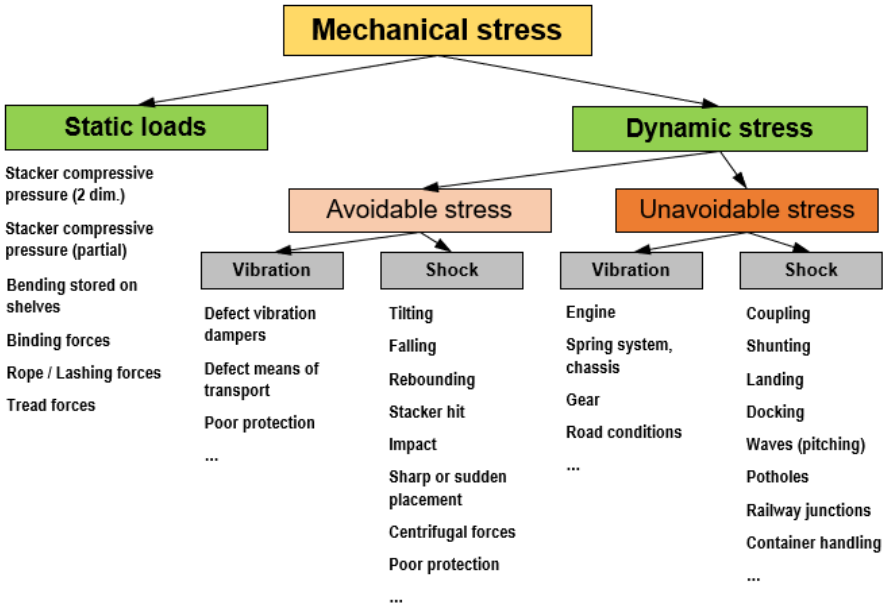


Figure 10.4.2 Types of mechanical stress according to the environmental conditions listed in IEC 60721-3-3

Mechanical conditions relate to the levels of vibration and shock that may exist at the location, for example, as a result of normal operations, for example due to vehicle movement in the vicinity

These conditions - classified by 3 categories sorted in ascending order with reference to their degree of mechanical impact inside a location – are specified in the IEC 60721-3-3, Table 5. These conditions are:

Class 3M10 (formerly 3M1): Locations where vibrations and shocks are insignificant.

Class 3M11 (formerly 3M2): Locations with low vibrations and insignificant shocks, e.g. from air conditioning systems, machines or passing vehicles in the vicinity (random stationary vibration 0.1 $(m/s^2)^2/Hz$; frequency range 5…200Hz; no shock).

Class 3M12 (formerly 3M5 and higher): Locations exposed to strong vibrations and shocks, e.g. near running heavy machinery and conveyor belts (random stationary vibration 0.1 $(m/s^2)^2/Hz$; frequency range 5…200Hz; shock $20m/s^2$).

In addition to the vibration level and the shock energy content, the determination of the appropriate mechanical stress class depends on the type of electronic device and its fixture (rigid, flexible, on vibration dampers).

10.4.2.3 Biological environmental conditions

Biological environmental conditions are classified by 3 categories sorted in ascending order according to the degree of contamination by mould / fungus formation, rodents and other animal pests. The following descriptions of the biological environmental classes are typical but may not be complete and comply with the original formulations in the standard IEC 60721-3-3. Compared to older editions, the designations of classes have been retained:

Class 3B1: Locations with environmental controls in place to prevent the growth of mould and physical controls are in place to prevent attacks by animals

Class 3B2: Locations without environmental or physical controls in place to prevent mould growth or attacks by animals, except termites.

Class 3B3: Locations where attacks by termites or similar fauna may occur.

10.4.2.4 Environmental impacts due to chemically active substances

Pollution of the atmosphere is mainly caused by chemical emissions from industrial processes industrial activities, motor vehicles and heating systems. Another chemical influence is caused caused by aerosols from sea and road salts. Pollution can affect the function and materials of products. Details on the categorisation of these conditions can be found in the standard DIN EN

ISO 9223:2012-05 "Corrosion of metals and alloys - Corrosivity of atmospheres - Classification, determination and estimation".

10.4.2.5 Environmental impact caused by mechanically active substances

Impact caused by mechanically active substances such as sand particles in the air and dust particles in air or precipitation are classified into 3 categories arranged in ascending order with reference to their degree of environmental impact. The class-descriptions - complying with the original formulations in IEC 60721-3-3 – are:

Class 3S5 (formerly 3S1): Locations where precautions have been taken to minimize the presence of dust and sand. Ingress of sand is prevented.

Class 3S6 (formerly 3S2): Locations not situated in proximity to dust or sand sources and with no special precautions to minimize the ingress of dust or sand (setting of sedimentary dust 6mg/(m²·d)).

Class 3S7 (formerly 3S3): Enclosed locations in close proximity to sand or dust sources, including urban areas and with no special precautions to minimize the ingress of dust or sand (turbulent (suspended) dust 600mg/(m²·h); but no windblown dust).

10.5 Effects of climatic environments on power modules

10.5.1 Preface

The content and all figures of the chapter 10.5 are from the Semikron Danfoss Application Note AN 16-001 "Effect of Humidity and Condensation on Power Electronics Systems" Rev. 01 [10.27].

10.5.2 Climatic environments

When discussing the "environment" around an electronic system, one must differentiate between the outdoor macro-environment and the micro-environments near or within the power semiconductor module (Figure 10.5.1).

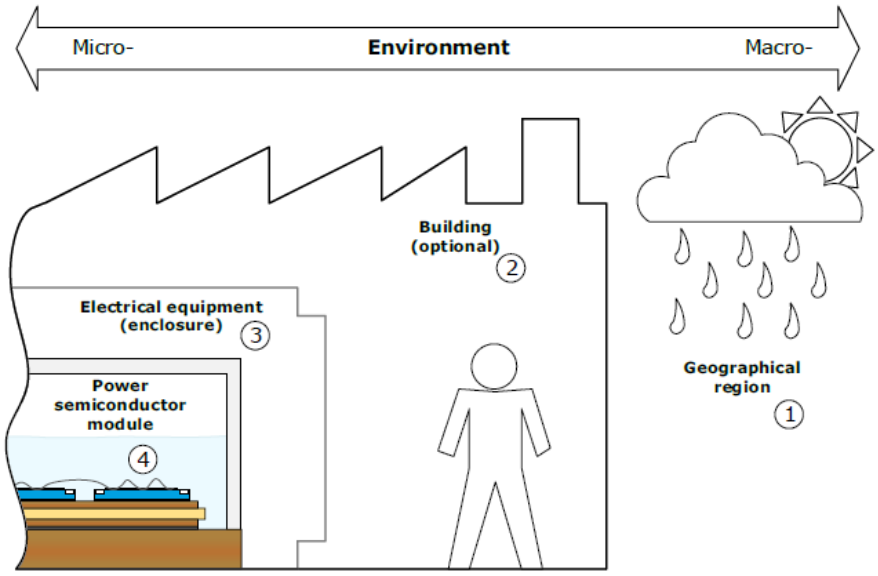


Figure 10.5.1 Four different environments within an application [10.27]

The outdoor macro-environment (Figure 10.5.1, ①) is generally well understood, with regular weather reports available, as well as standards defining the characteristics (temperature, humidity, pressure, etc.). Conversely, the micro-environments in (Figure 10.5.1, ④) and around (Figure 10.5.1, ③) a power semiconductor module are less well defined, though they are determined by the outdoor macro-environment and operation of the power electronics system (power level, cooling, etc.).
As already described in chapter 10.4.2 defines the IEC 60721-3-3 standard the permissible macro-environmental conditions where electrical equipment will be installed (i.e., Figure 10.5.1, ①, ②). While this standard cannot be applied directly to the semiconductor modules (a component), it does give a clear definition of the outside environment that must be protected against (by means

of an enclosure, etc.). Furthermore, the IEC "climatograms" provide an effective means of understanding the relationships between temperature and humidity, no matter in which environment they occur.
Figure 10.5.2 shows a generic example of such a climatogram where the air temperature and relative humidity are given on the major axes and the absolute humidity is plotted as a series of curves. Using three variables a preferred area of operation for power electronics systems can be defined, outside which damage or reduced lifetime could occur. The goal of the designer is to understand how these variables affect one another and keep the operating point of the system within the preferred operating area through system design and operation.

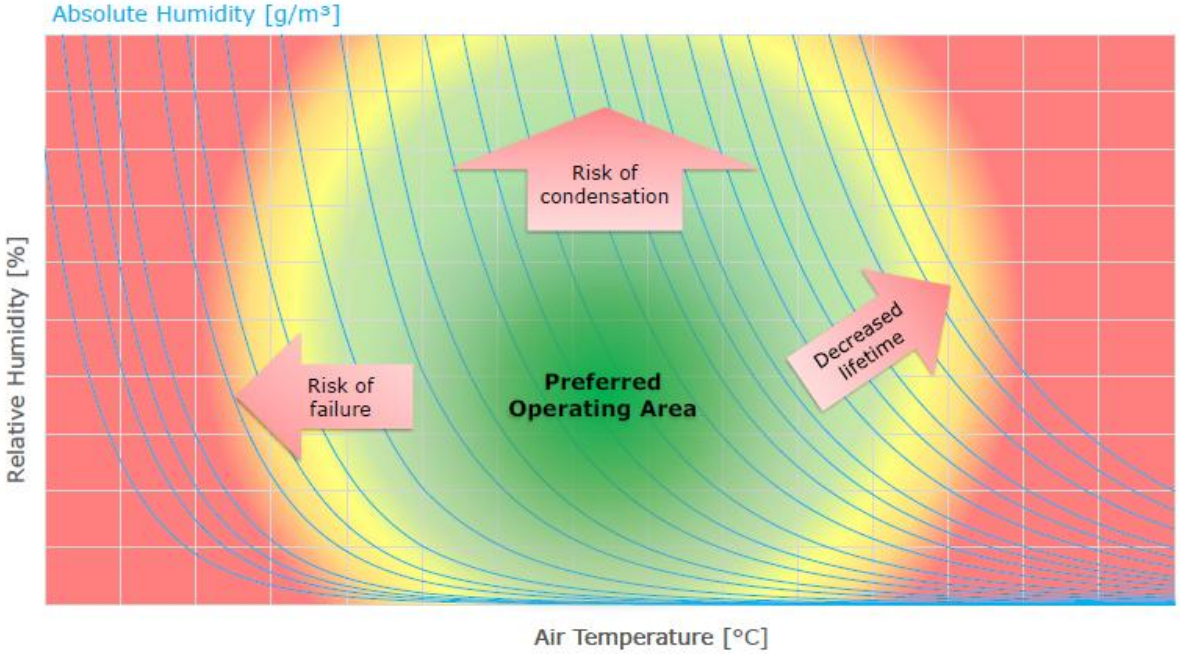


Figure 10.5.2 Preferred macro-environment for power electronics [10.27]

10.5.3 Humidity

Water in its most common form causes problems with electrical circuits due to its electrically conductive and corrosive nature. Another effect is caused by water in the vapour state. This vapour is diffused into the surrounding air and behaves according to the temperature and pressure in a given volume. The presence of water vapour in air is referred to as humidity and is defined in different ways:

- Absolute humidity (AH): The density of water vapour in air, typically expressed as grams/cubic meter [g/m³].
- Relative humidity (RH): The ratio of the partial pressure of the water vapour to the saturation vapour pressure, typically expressed as a percentage [%].

Absolute and relative humidity are interrelated and are functions of temperature and pressure. Most environment and product specifications use relative humidity as this can be easily measured using sensors. However, as will be shown the relative humidity for a given amount of humid air can change even if the number of water molecules remains constant.

10.5.4 Condensation

When water vapour present in air changes state from a gas into a liquid, it forms condensation on surfaces (or frost in low temperatures). The temperature at which condensation occurs is called the dew point and varies with the relative humidity.
Figure 10.5.3 shows the relationship between relative humidity, air temperature, and dew point based on a Magnus equation approximation. For a given pressure and humidity, if the temperature of a volume of air (or object) drops below the dew point, condensation will occur in that area. More specifically, the chart shows the temperature (dew point) at which the relative humidity of a certain volume of air will become 100% based on the overall conditions.

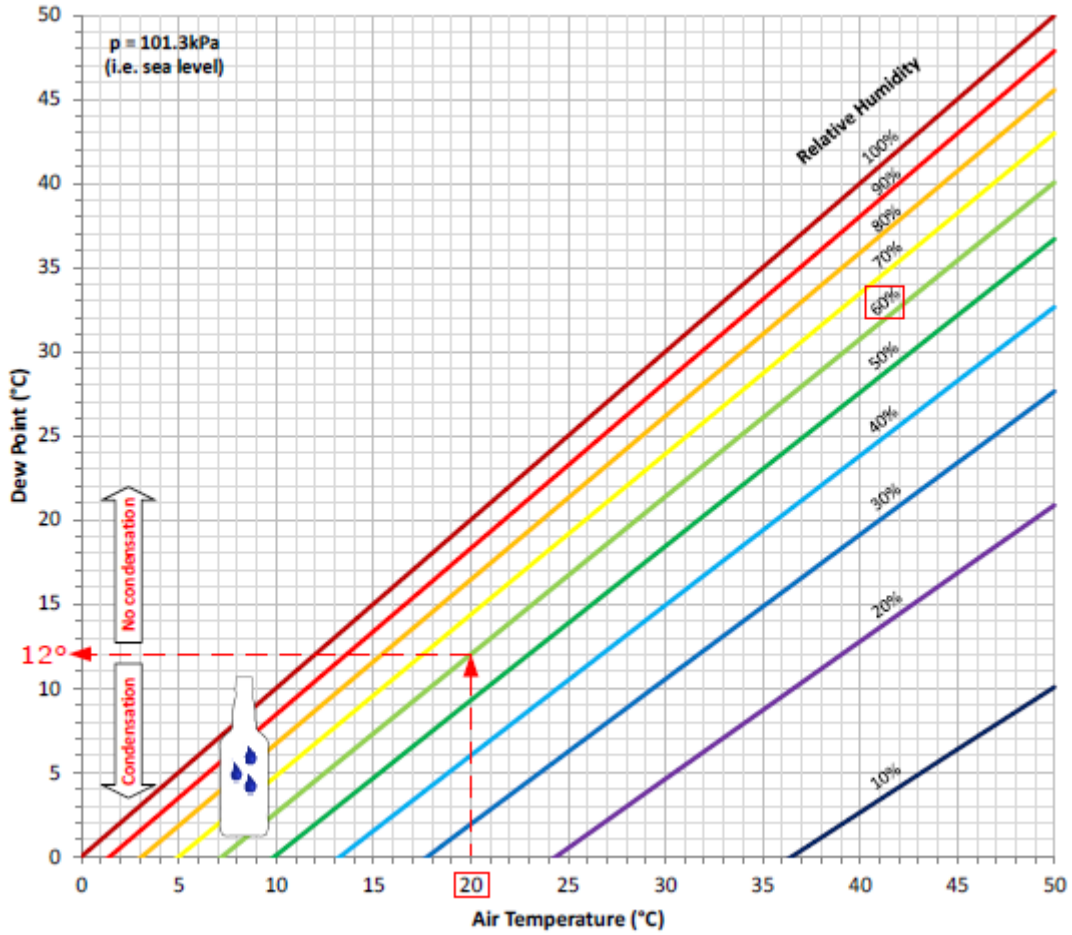


Figure 10.5.3 Determining dew point using the Magnus equation [10.27]

The dew effect can also occur in the micro-environment (Figure 1, ④) inside a power semiconductor module. The IEC climatogram provides an alternate method of calculating [10.28], [10.29] when this condensation will occur and illustrates the variability of relative humidity even when the amount of water vapour remains the same (Figure 4). Using a hypothetical power semiconductor module, the following assumptions are made:

- The volume of the module (and enclosed parcel of air) is fixed ($V_{State1} = V_{State2} = V_{State3}$)
- The module is permeable (n_{total} is variable)
- Pressure is dominated by the outside environment ($p_{State1} = p_{State2} = p_{State3}$)
- The absolute humidity is fixed ($AH_{State1} = AH_{State2} = AH_{State3}$; n_{water} is constant because volume is constant)

In this scenario, when the temperature drops, the partial pressure of the water vapour reduces slightly according to the ideal gas law ($p \cdot V = n \cdot R \cdot T$). However, the saturation vapour pressure drops dramatically and since relative humidity is a ratio of these two values, the relative humidity increases.

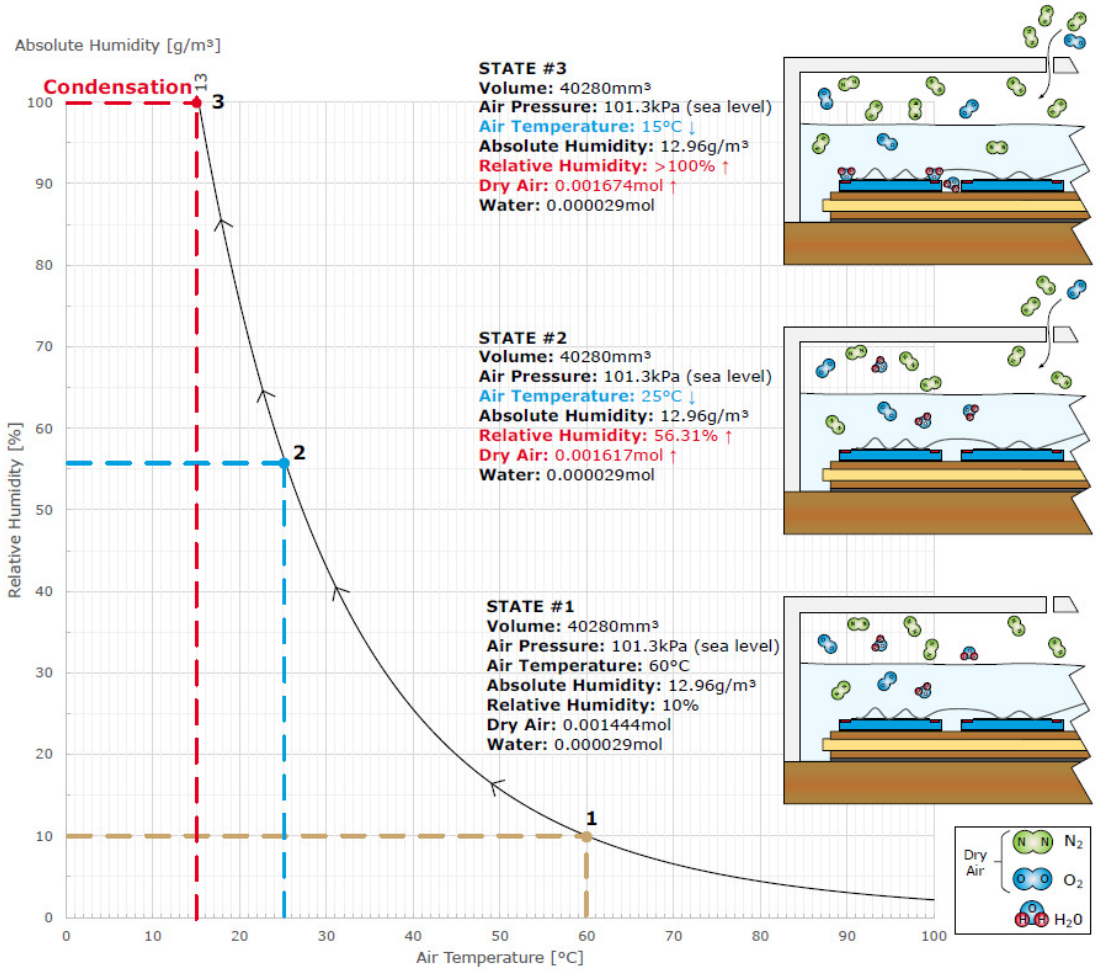


Figure 10.5.4 Determining Variability of relative humidity in a power module [10.27]

Most electrical equipment is designed to operate within an IEC 60721-3-3 climatic class 3K22 (formerly 3K3). In addition to temperature and pressure ranges, the 3K22 class gives an allowable range of relative humidity from 5% to 85%, without allowing condensation to form. Furthermore, the absolute humidity is limited to 25g/m³. While the 3K22 range only defines an allowable temperature range of 5° to 40°C, it is common to allow a larger temperature range (-40°C to 85°C) which results in an extended operating area as shown in blue in Figure 10.5.5.

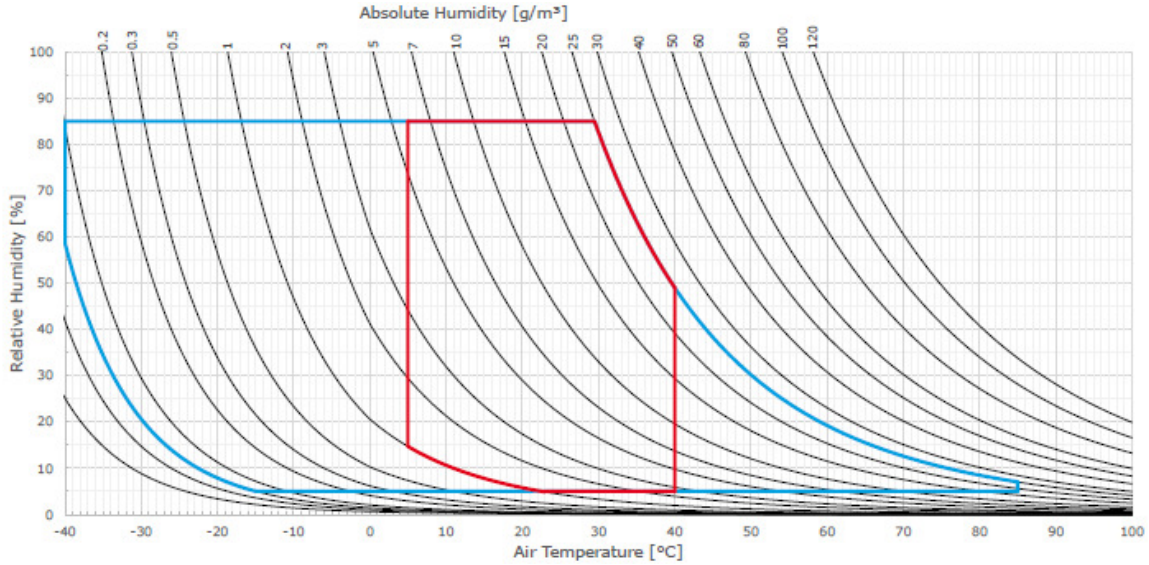


Figure 10.5.5 Permissible macro-environments for electrical equipment per IEC 60721-3-3 class: 3K22 (red) and with extended temperature range (blue) [10.27]

10.5.5 Sources and impact of humidity and condensation on power modules

10.5.5.1 Humidity

Most industrial power modules consist of a plastic housing containing chips that have been encapsulated in a cured silicone-based gel ("soft mould", "sil-gel") that provides electrical insulation between conductors. However, the module is not hermetically sealed (gas tight) so atmospheric gas can permeate the module through openings at power terminals, etc.
The soft mould also contains diffused air (Figure 10.5.6). Therefore, water molecules can also propagate through the soft mould in the same manner that they mix with air, albeit at a slower rate (e.g. 0.04mm/s @ 18°C, 1mm/s @ 100°C). Once inside the soft mould, the water molecules have the following effects:

Reduced blocking voltage: When the heat sink temperature decreases, the diffused air inside the silicone holds less moisture. Water molecules will therefore accumulate on colder surfaces thermally coupled to the heat sink, such as the substrate, terminals and semiconductor surfaces. Furthermore, the water molecules are attracted to the charged semiconductor surfaces due to their dipole characteristic and align themselves in the electric field (Figure 10.5.6). This leads to disruption of electric field lines at the semiconductor edge termination that can lead to reduced blocking voltage.

Semiconductor corrosion: The effect of corrosion on semiconductor chip passivation is well-known [10.30]. With applied voltage and humidity, the chip edge passivation corrodes until breakdown occurs and the semiconductor fails. The semiconductor corrosion is a long-term aging effect that is investigated in power module reliability tests, e.g. the "High Humidity High Temperature Reverse Bias" (H³TRB) and the "High Voltage High Humidity High Temperature Reverse Bias" (HV-H³TRB) test, see descriptions of these tests in chapters 4.4.4 and 4.4.5.

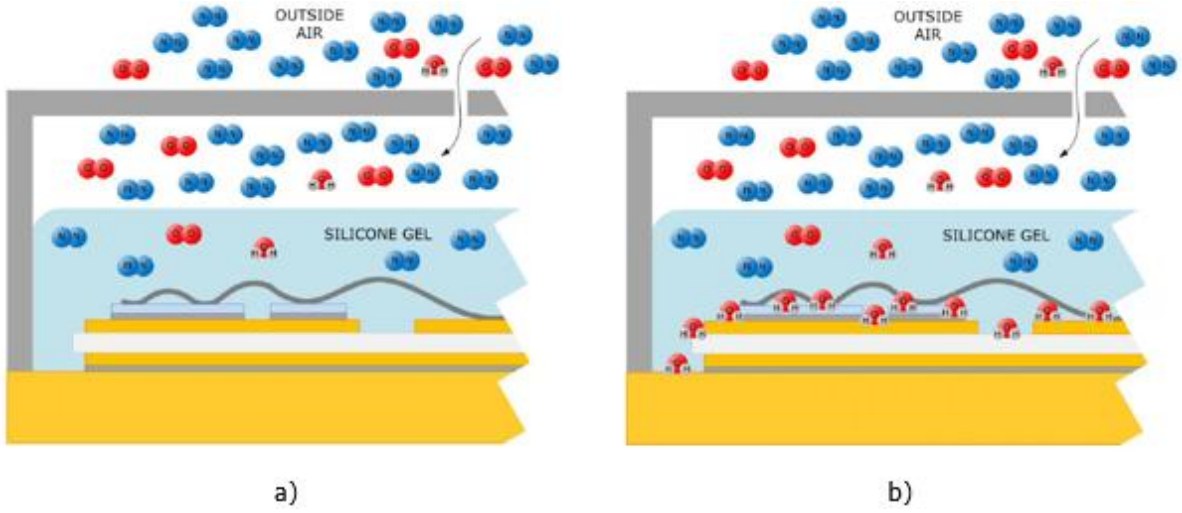


Figure 10.5.6 Behaviour of water molecules into the silicone: a) Diffusion in the air; b) accumulate on surfaces, driven by their dipole characteristic and condensation [10.27]

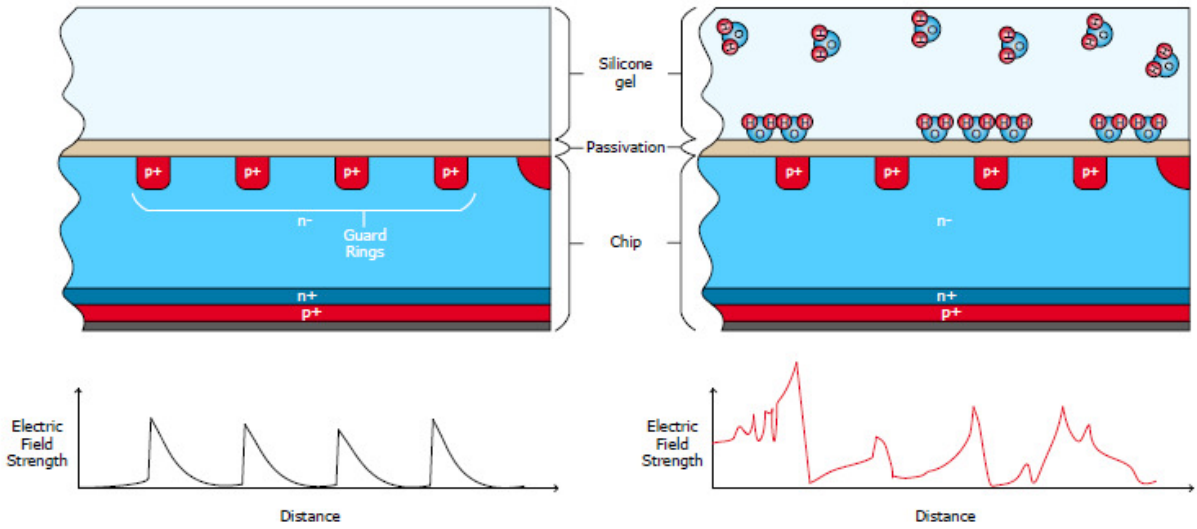


Figure 10.5.7 Disruption of voltage gradient at edge termination [10.27]

10.5.5.2 Condensation

Once water vapour has condensed into a liquid, the effects on a power electronic system are much more obvious. Droplets of water forming on a heat sink may be an indication that condensation is occurring inside the power module. If possible, this condensation should be checked for during operation, as the water may evaporate when the unit is not operating and no evidence will be visible.

10.5.5.3 Transport and storage

Power electronics shipped over long distances or stored for long periods may acquire water vapour within the packaging, potentially leading to catastrophic failure when voltage is applied. Information on suitable packaging and commissioning procedures can be found in [10.27].

10.5.5.4 Changes in relative air pressure

The effects of air pressure at a particular location are already factored into the prevailing temperature and humidity in a macro-environment and thus atmospheric pressure can generally be neglected for a given application. However, in enclosures that have been sealed to outside air flow (e.g. IP65), a change in internal air pressure (typically due to a change in temperature) can result in high relative humidity within the enclosure. For sealed enclosures this air pressure differential may be reduced though the use of vents.

10.5.5.5 Changes in air temperature

Operating point

One of the main causes for temperature disparities within a unit is the operation of the system itself. Electrical operation of the system causes the temperature of components and the internal cabinet air temperature to rise. A sudden change in operation can cause the heat sink to cool much more rapidly than the air temperature of the enclosure, possibly creating a condition where the heat sink temperature falls below the dew point. Therefore, it is critical to be aware of any changes from operation at full power to another mode, such as small or no load/standby mode or unexpected or interruption of operation, e.g. due to faults.

An explanation of how this can occur is given in Figure 10.5.8. Note that this risk is also present when the air temperature drops during the transition between day and night. As the inlet air temperature (fed from outside ambient air) on an air-cooled heat sink drops in the evening the heat sink may be cooled to below the dew point (calculated using Figure 10.5.3).

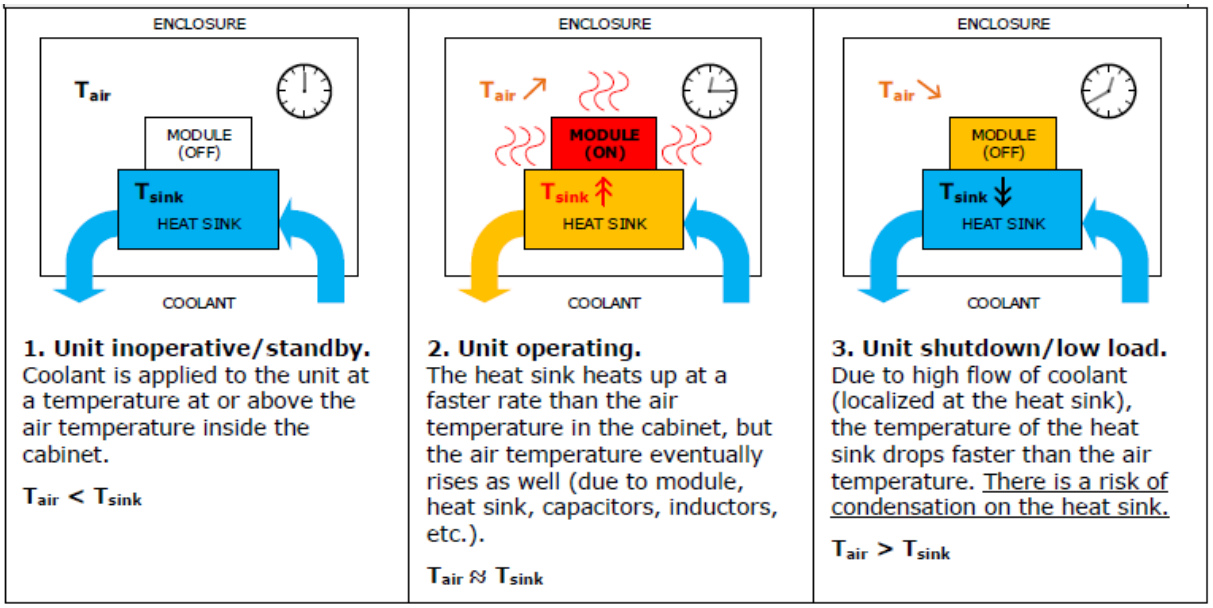


Figure 10.5.8 Possible temperature disparity due to system operation [10.27]

Temperature differentials within a cabinet

As a result of changing operating points or the cabinet design, condensation may occur on certain areas (cold spots) within the cabinet. Experience has shown the following areas have the highest risk:

- Fresh air inlet ports.
- Coolant inlet manifolds and piping.
- Outer (metallic) walls of the cabinet.
- Heat sinks and any components to which they are thermally coupled.
- Areas with low air flow relative to other portions of the cabinet.
- Large (dense) metallic components with a long thermal time constant.

Condensation on cabinet ceilings and walls may drop onto the power module, electronics or bus bars, causing short circuits.

10.5.6 Mitigation techniques

10.5.6.1 General

Mitigating humidity and/or condensation within an enclosure can be roughly divided into two approaches (Figure 10.5.9):

- Reduction of absolute humidity: Removal of water vapour (drying) through dehumidifiers, desiccants, or a combination of long-term heat plus air flow.
- Reduction of relative humidity: Increase of air temperature through heating (dedicated heater or system operating point)
- Control of individual component temperature (e.g. heat sinks) to avoid falling below the
- dew point by load-dependent control of the air or liquid coolant (see chapters below).

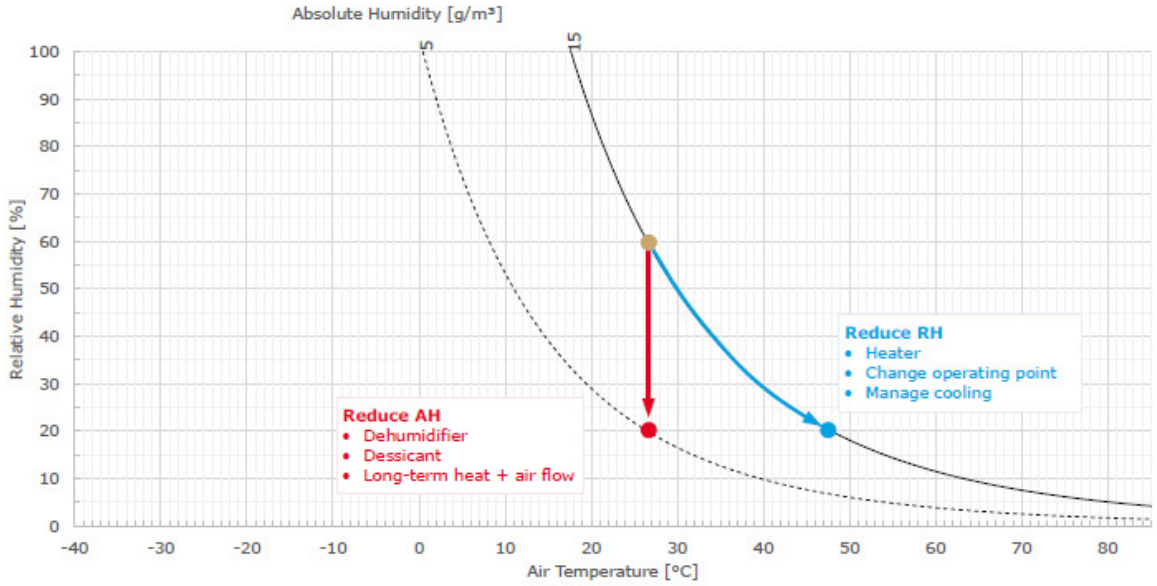


Figure 10.5.9 Approaches to mitigating humidity [10.27]

10.5.6.2 Fan control (aircooled system)

The temperature of the heat sink is monitored, and the fan speed is adjusted to prevent air below a minimum temperature from passing over the heat sink fins. Below a set point, the fan is completely off (or operating at minimum speed). After the set point is reached, the fan starts to operate and increases speed as the temperature increases. At high loads, the fan operates at full speed. If the unit suddenly reduces output power, the fan should switch off immediately to avoid the behaviour described above at high humidity. This regulation method is costly but has the advantage that the stress on semiconductors and fan is low. In addition, overall system efficiency may be increased by reducing the power consumed by the fans when the converter load is low.

10.5.6.3 Coolant temperature control (liquid cooled system)

The coolant temperature should be warm enough such that the heat sink surface temperature never drops below the dew point. Ideally, the coolant temperature should be above the internal cabinet ambient temperature. Two methods for coolant temperature control are proposed (Figure 10.5.10):

- Use of a three-way thermostatic control valve: At low temperatures (a common set point is between 25°C and 30°C) the coolant will flow through a bypass loop and not through the heat exchanger. Upon reaching the set point, the valve starts to open and tries to keep the temperature constant. At higher power, the coolant flows entirely through the heat exchanger.
- Use of a coolant heater: Heating of the coolant is necessary to:
- Reduce localized relative humidity inside or near the power module after commissioning and when restarting after a long period of idle operation before applying voltage.
- Prevent condensation on the heat sink when the internal cabinet air temperature is hotter than the heat sink.

When using an efficient heat exchanger and/or operating at full power, the inlet temperature is normally several degrees above the ambient temperature. At high internal cabinet temperatures with low load and high humidity, it may be necessary to increase coolant temperature further to prevent condensation.

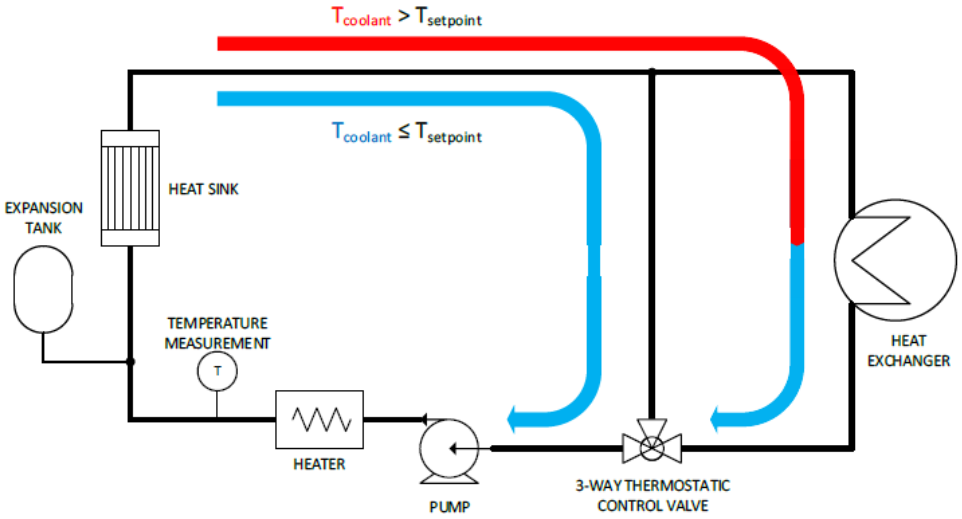


Figure 10.5.10 Coolant loop with bypass and heater [10.27]

10.5.6.4 Pre-heating procedures prior to start-up

Experiments with power modules in an environment with 85% relative humidity have shown that using a coolant temperature at least 5K hotter than the ambient air temperature will reduce the relative humidity inside the module. Figure 10.5.11 describes the results of such a test in which the humidity beneath the silicone gel inside a module was measured as warm coolant (40°C) was applied in a high humidity environment with different ambient temperatures.

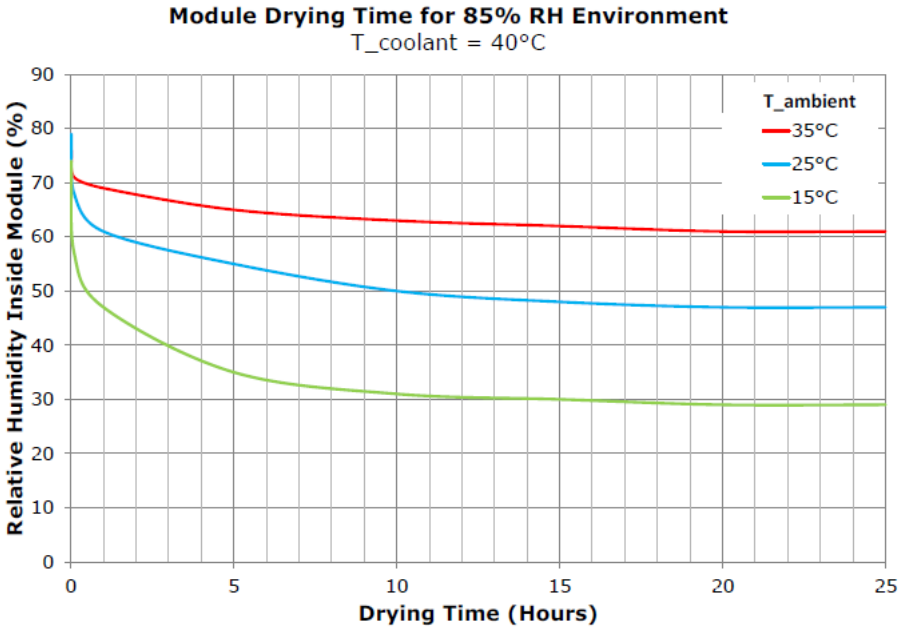


Figure 10.5.11 Results of experiment involving heated coolant to reduce humidity [10.27]

In this particular experiment, the steady state value of relative humidity is reached within 24 hours and the characteristic roughly follows an inverse exponential curve. Based on the above test results and experience with real customer applications, the following is recommended:

- For systems where there is risk that the power modules have been exposed to high humidity during transportation or storage prior to initial operation (commissioning), coolant with a minimum temperature of 25°C and at least 5K above the ambient air temperature should be applied for 24 hours prior to the application of high voltage (>50V DC).
- For commissioned systems (installed outdoors or in high humidity environments) that have been inoperative for more than 8 hours, coolant with a temperature at least 5°C above the ambient air temperature should be applied for 1 hour prior to the application of high voltage (>50V DC).

10.5.6.5 Cabinet heaters

As described previously, for a fixed absolute humidity, increasing the ambient (dry) air temperature will decrease the relative humidity. Industrial cabinet heaters are commercially available to facilitate this. Consisting of a resistive heating element, thermostat and occasionally a fan for air circulation these units serve to:

- Reduce relative humidity inside a cabinet after initial commissioning.
- Drive humid air out of a cabinet through vents.
- Prevent condensation from forming on internal cabinet walls/ceiling.
- Prevent condensation on internal metal parts when the external ambient gets hotter.
- Pre-heat an electrical cabinet prior to operation (if the minimum operating temperature is not met) and protect the electronics during operation in low ambient temperatures.
- Maintain active parts at higher-than ambient temperatures during standby.

While simple on/off operation is possible with a temperature set point (e.g. with a thermostat), a heater can also be controlled by a hygrostat to ensure that the air temperature inside the cabinet does not fall below the dew point. Heaters should be placed at the bottom of the cabinet and should have sufficient power to heat the inner ambient to a defined level at a low external ambient temperature.

10.5.6.6 Dehumidifiers

The most direct method of humidity reduction is to remove the moisture from the air using a dehumidifier. A dehumidifier consists of a cooled coil over which the humid air is forced. Moisture in the air condenses on the coil and is drained or pumped out of the system. Industrial cabinet dehumidifiers are available.
Dehumidifiers are typically placed at the bottom and side of a cabinet and the condensate hose is routed through the wall or floor to drain outside. Consideration should be given to making sure air circulates through the dehumidifier, either through internal cabinet fans or by positioning the internal dehumidifier fans.

10.5.6.7 Vents

For small, sealed enclosures where it is necessary to equalize pressure, specialized snap-in or screw-in vents are available [10.31]. These vents incorporate a semi-permeable hydrophobic membrane that allows vapour to pass through while keeping out water droplets and other contamination (Figure 10.5.12). It is important to understand that these vents may allow water vapour to pass through, so they do not necessarily reduce the absolute humidity. However, they are important in ensuring that a mismatch in pressure does not occur resulting in high relative humidity inside the enclosure.

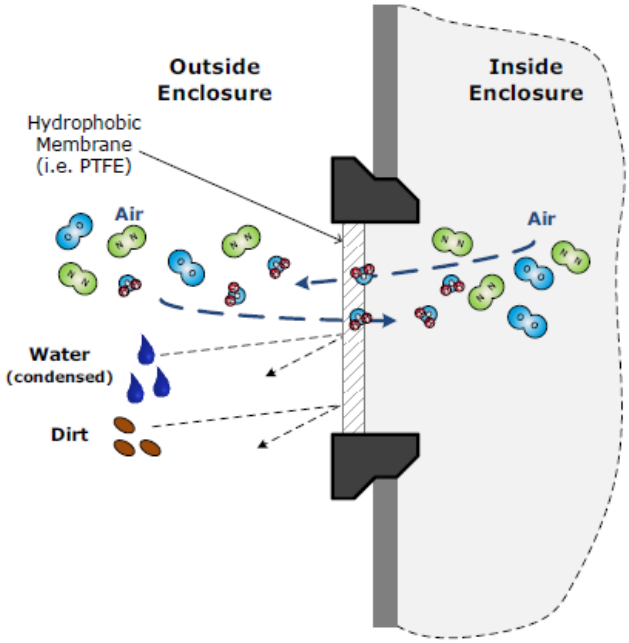


Figure 10.5.12 Vent plug operation [10.27]

10.5.6.8 Desiccants

Desiccants are hygroscopic materials that absorb and store moisture from the air. They normally consist of a silica gel (or other natural material such as clay) packaged in a permeable membrane through which moist air can pass. Because they entrap water vapour, their capacity is limited and they will eventually become saturated. For this reason, desiccants are typically only used during transportation of sealed containers for entrapping residual water vapour.

10.5.6.9 Removal of DC link voltage

As noted above, applied voltage accelerates long-term corrosion of the semiconductor's chip metallisation. Many power electronic systems have long periods of standby operation where a high voltage is present on the DC link but the system is not processing any power. In these applications, discharging the DC link when the system is standby mode could improve lifetime in high-humidity environments where this corrosion mechanism may be present. As this typically requires opening a contactor and a discharge (and pre-charge) process, this technique must be considered in the design process in a system and may be difficult to implement after system design (e.g. additional wear may be incurred in other components from repeated cycling).

10.5.7 Conclusions for optimal cabinet designs

Power modules (and other components in the power circuit) are at risk from water in both the liquid (condensation) and gaseous (humidity) states. A failure can occur either in the short-term (voltage flashover) or long-term (corrosion). Mitigation starts with understanding the relationships between absolute humidity, relative humidity, and temperature around the power electronics (macro-environment) and inferring what might be the environmental conditions inside a power semiconductor module (micro-environment). Steps can then be taken either through system design (e.g. air flow, temperature control) or operating point (e.g. coolant control) to reduce the conditions where high relative humidity or condensation may occur near or inside a power module. The external macro-environment (and its associated pollution, temperature and humidity levels) is usually the main factor in determining whether an electrical cabinet is required to be sealed.
For the purposes of this discussion, a sealed (closed) cabinet is defined as one having an IEC ingress protection (IP) rating of 65 or higher [10.32]. This means the cabinet is protected against dust ingress and low power water jets sprayed from any direction. However, this also implies that the air flow between the inside of the cabinet and the outside environment is limited and therefore differentials in temperature and pressure might occur. Conversely, an open cabinet is defined as one in which there is a free exchange of the outside air with the inside of the cabinet.

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11 Terms and Symbols

Symbol	Designation
a	Maximum acceleration under vibration
A	Area
AH	Absolute humidity
AMB	Active metal brazing
ANPC	3-level Active neutral point clamped converter
α	Heat transfer coefficient
α_{npn}, α_{pnp}	Current gain of npn transistor part, of pnp transistor part (thyristor)
$B_{25/85}$, $B_{100/125}$	Exponents of temperature sensor equation with temperature range
B2, B6	1-phase rectifier bridge, 3-phase rectifier bridge
BW	Bandwidth
C_{CE}	Collector - emitter capacitance (IGBT)
C_{CHC}	Capacitance chip-case (baseplate)
C_{DC}, $C_{DC\text{-}link}$	Capacitance of DC-link capacitor bank
C_{DS}	Drain - source capacitance (MOSFET)
C_{GC}	Gate - collector (Miller) capacitance (IGBT)
C_{GE}	Gate - emitter capacitance (IGBT)
C_{GD}	Gate - drain (Miller) capacitance (MOSFET)
C_{GS}	Gate - source capacitance between (MOSFET)
C_{GK}	external capacitance between gate and cathode (thyristor driver)
C_{ies}	Small signal input capacitance, collector-emitter short-circuited (IGBT)
C_{iss}	Small signal input capacitance, drain-source short-circuited (MOSFET)
C_{IN}	Input capacitance
C_j	Junction capacitance
C_K	Commutation capacitance
C_L	Capacitance of load capacitor
C_{max}	Maximum permissible capacitance of DC-link capacitor
CMV	Common mode voltage
C_{oes}	Small signal Output capacitance, gate-emitter short-circuited (IGBT)
C_{oss}	Small signal Output capacitance, gate-source short-circuited (MOSFET)
c_p	Specific heat capacity --> capacitance?
C_{ps}	Coupling capacitance, primary to secondary winding
C_{res}	Small signal reverse transfer capacitance (IGBT)
C_{rss}	Small signal reverse transfer capacitance (MOSFET)
CSI	Current source inverter
$C_{snubber}$	Snubber capacitor capacitance
C_{th}	Thermal capacitance
CTE	Coefficient of thermal expansion
CTI	Comparative tracking index
D, DC	Duty cycle ($f \cdot t_p$)
DBB	Danfoss Bond Buffer technology
DBC	Direct Bonded Copper
di/dt	Current slope
$(di/dt)_{cr}$	Critical rate of rise of on-state current (thyristor)
$(dv/dt)_{cr}$	Critical rate of rise of off-state voltage (thyristor)
DGS	Dynamic Gate Stress (test)
DRB	Dynamic Reverse Bias (test)
DSC	Double sided cooling
d_{tp}	thickness of thermal paste
dv/dt	Voltage slope
dV/dt	Volume flow
ΔI_r	Maximum variation in blocking/leakage current
Δp	pressure drop of coolant
E_A	Activation energy
E_{cond}	Energy during conduction time
ED	Intermittent duty
E_{off}	Energy during turn-off
E_{on}	Energy during turn-on

EOL	End of Life
E_P	Maximum permissible non-repetitive peak pulse energy (2ms rectangular pulse)
E_{rec}	Energy (rectifier circuit)
E_{rr}	Energy during reverse recovery (diode)
E_{RSM}	Non repetitive peak reverse avalanche energy
E_{tp}	dielectric strength of thermal paste
EGW	Ethylene Glycol Water mixture
η	Efficiency
f	Operating frequency
f_{clock}	Gate driver internal clock frequency
F	Mounting force
Φ	Power factor angle of the short circuit circuit impedance
f_{Alt}	Frequency of the superimposed AC voltage
f_{Fan}	Supply voltage frequency for fan operation
F_i	Form factor
FIT	Failures in time
f_{max}	Maximum frequency
f_{out}	Output frequency
FRT	Fault Ride Through
f_{sw}	Switching frequency
F_x	Terminal force in x-Direction (modules)
F_y	Terminal force in y-Direction (modules)
F_{z+}	Terminal pulling force in z-Direction (modules)
F_{z-}	Terminal pushing force in z-Direction (modules)
g_{fs}	Forward transconductance
g_{tp} (g)	specific gravity of thermal paste
HTGB	High Temperature Gate Bias (test)
HTFB	High Temperature Forward Bias (test)
HTRB	High Temperature Reverse Bias (test)
H³TRB	High Humidity High Temperature Reverse Bias (test)
HV-H³TRB	High Voltage High Humidity High Temperature Reverse Bias (test)
HIN	PWM signal input high side switch
HTS	High Temperature Storage (test)
i^2t	Peak load integral
I_{actual}	Actual measured current level per halfbridge (SKiiP)
$I_{AC\text{-}terminal}$	AC-terminal current
$I_{analogOUT}$	Current sensor reference value (SKiiP)
I_{BOT},	BOTOM side IGBT current
$I_{C(BOT)}$	BOTOM side IGBT collector current
I_C	Continuous collector current
I_{CES}	Collector-emitter cut-off current , gate-emitter short-circuited (IGBT)
I_{cm}	Common mode current
$I_{C(max)}$	Maximum value of collector current
I_{cnom}	Nominal collector current
$I_{C(off)}$	Actual turn-off current (IGBT)
I_{Cpuls}	Pulsed collector current
I_{CRM}	Repetitive peak collector current
I_{CSM}	Non-repetitive peak collector current
$I_{C/SC}$	Collector current on the end of short circuit II
$I_{C/SCM}$	Short circuit II peak collector current
I_D, I_{DC}	Direct output current (rectifier)
I_D	Continuous drain current (MOSFET)
$I_{D(CL)}$	Direct output current with capacitive load
$I_{digiout}$	digital output sink current
I_{DD}	Direct forward off-state current (thyristor)
I_{dm}	Differential mode current
I_{DM}	Peak value drain current
I_{Dnom}	Nominal drain current (MOSFET)
I_{DR}	Continuous reverse drain current (MOSFET inverse diode forward current)
I_{DRM}	Peak value of reverse drain current, (MOSFET inverse diode forward current)
I_{DSS}	Drain-Source cut-off current, gate-source short-circuited (MOSFET)
I_E	Continuous emitter current

I_F, i_F	Forward current
I_{Fnom}	Nominal forward current
$I_{F(CL)}$	Mean forward current with capacitive load
$I_{F(OV)}$	Overload forward current (diode)
I_{Fan}	Fan operational current
I_{FAV}	Mean forward current
I_{FM}	Peak forward current
I_{FN}	Recommended mean forward current
I_{FRM}	Repetitive peak forward current
I_{FRMS}	RMS forward current
I_{FSM}	Surge forward current
I_G	Gate current
I_{GAV}	Gate current, average value
I_{GC}	Displacement current through the Miller capacitance (IGBT)
I_{GD}	Gate non-trigger current
I_{GES}	Gate-emitter leakage current, collector emitter short-circuited (IGBT)
I_{Goff}	max. turn-off output current (driver)
I_{Gon}	max. turn-on output current (driver)
I_{GSS}	Gate-source leakage current, drain-source short-circuited (MOSFET)
I_{GT}	Minimum gate trigger current
I_H	Holding current
I_{iH}	Input signal current (High)
I_{ign}	Recommended trigger current (pulse transformer)
I_K	Short circuit current of thyristor gate driver
I_L	Latching current
I_{load}	Load current
I_M	Maximum peak current obtainable at a rise time lower than 1µs (pulse transformers)
i_{max}	Maximum non-repetitive surge current (varistor)
I_{max}	Maximum turn-off collector current (usually with active short circuit turn-off)
$I_{max(EO)}$	Maximum error-output current (SKiiP)
$I_{max\ (peak)}$	Maximum peak current of power section (SKiiP)
IMS	Insulated Metal Substrates
I_n	Rated current (fuse)
I_N	Nominal direct current
$I_{(LT)}$	Let-through (conducting) current (fuse)
I_{nom}	Nominal current
I_{Omax}	Max. output current (driver)
I_{out}	Output current of a circuit
I_{outAV}	Output average current (driver)
$I_{outPEAK}$	Output peak current (driver)
$I_{outsens}$	AC sensing range
$I_{outtrip}$	AC over current trip level
$I_{overload}$	Overload current for a specified time
$I_{peak(1)}$	magnitude of current's first harmonic
I_p	Cut-off (Let-through) current (fuse)
I_{ps}	Prospective short circuit current (fuse)
I_R	Reverse current
i_{rc}	Discharged capacitor current (RC-snubber)
I_{RD}	Direct reverse current (thyristor)
I_{RMS}	Maximum RMS current of an AC-controller
I_{rr}, i_{rr}	Reverse recovery current
I_{RRM}	Peak reverse recovery current
I_{RSM}	Maximum non-repetitive peak reverse current (avalanche diodes)
I_S	Primary side supply current (driver)
I_{sc}	Short-circuit current (IGBT, MOSFET)
I_{S0}	Supply current primary side (driver) at no load
I_T, i_T	On-state current (thyristor)
$I_{T(OV)}$	Overload on-state current (thyristor)
I_{TAV}	Mean on-state current
I_{TM}	Peak on-state current
I_{TOP}	TOP side IGBT current

I_{TRIPSC}	Overcurrent trip level (SKiiP)
I_{TRMS}	RMS on-state current
$I_{t(RMS)}$	RMS terminal current
I_{TSM}	Surge on-state current
I_V	RMS phase current
I_z	Tail current (IGBT)
j	current density
K_B	Boltzmann constant
K_i	Exponent of switching loss current dependency
k_{ing}	Correction factor for uneven heat profile at the outlet of heatsink 1 (thermal stacking)
k_v	Exponent of switching loss voltage dependency
λ	Thermal conductivity
L	inductance
L_{Busbar}	Parasitic busbar inductance
L_C	Parasitic TOP-collector inductance
L_{cap}	Parasitic inductance of DC link capacitors
L_{CE}	Total parasitic inductance between TOP-collector and BOTTOM-emitter
L_{DS}	Parasitic drain-source inductance
L_{DC+}, L_{DC-}	Busbar parasitic inductances
L_E	Parasitic BOTTOM-emitter inductance
L_{EC}	Parasitic connection inductance between TOP-emitter and BOTTOM-collector
$L_{EE'}$	IGBT Emitter/inverse diode anode terminal parasitic inductance (IGBT module)
L_{ESR}	series inductance of DC-link capacitor
L_{ext}	External circuit inductance (short circuit)
L_G	Parasitic gate inductances
LIN	PWM signal input low side switch
$L_{CC'}$	IGBT Collector/inverse diode cathode terminal parasitic inductance (IGBT module)
L_K	Commutation inductance
L_p	Inductance of the primary winding at 1 kHz (pulse transformer)
L_R	Series inductance
L_s	Commutation loop inductance (pulse transformer)
$L_{snubber}$	Snubber capacitor series inductance
L_{sp}	Stray inductance (pulse transformer primary side)
L_{ss}	Stray inductance (pulse transformer secondary side)
L_σ	Stray inductance
LSC	Line side converter
LTS	Low temperature storage (test)
m	Modulation factor
M	Mounting torque
M_{GE}	Mutual gate inductance between main current path and gate circuit
M_s	Mounting torque on heat sink
M_t, M_{ac}, M_{dc}	Mounting torque for terminals, AC terminals, DC terminals
MSC	Machine side converter
MTBF	Mean time between failure
MTTF	Mean time to failure
μ_p	hole mobility
μ_n	electron mobility
N_A	Acceptor density
n_{av}	Density of the electrons generated by dynamic avalanche
N_D	Donator density
N_{eff}	Effective charge carrier density
N_f	number of failures
N_p/N_s	Ratio of winding primary to secondary
NPC	3-level Neutral point clamped converter
NTC	Negative temperature coefficient (e.g. temperature sensor)
OVCAT	Overvoltage category
ω	Supply angular frequency
p	Hole density
p	Pressure
P_{AV}	(Maximum permissible) average power dissipation

PC	Power Cycling (test)
P_{cond}	Forward (on-state) power dissipation
P_D	Power dissipation (diode)
PELV	Protective Extra Low Voltage
P_{Fan}	Power consumption of fan
P_{FAV}	Mean forward power dissipation (diode)
P_{FM}	Peak forward power dissipation (diode)
P_{GM}	Peak gate power dissipation
P_{GAV}	Gate power dissipation, average value
PGW	Propylene Glycol Water mixture
P_{loss}	Power dissipation
P_{off}	Turn-off power dissipation
P_{on}	Turn-on power dissipation
P_{pulse}	Power dissipation per pulse
P_R	Reverse power dissipation, Power dissipation of resistor R
P_{RAV}	Mean reverse power dissipation
P_{RRM}	Peak repetitive reverse power dissipation
P_{RSM}	Non-repetitive peak reverse power dissipation
P_{sw}	Switching power dissipation
PTC	Positive temperature coefficient (e.g. temperature sensor)
P_{TAV}	Mean on-state power dissipation (Thyristor)
$P_{terminal}$	Terminal power dissipation (modules)
P_{tot}	Total power dissipation
P_{ZSM}	Non repetitive peak power dissipation (Zener diodes)
ρ	Density of air (cooling)
q	Elementary charge
Q_c	Capacitive charge (SiC SBD)
Q_f	Charge recovered during the reverse current fall time
Q_G	Gate charge (IGBT, MOSFET)
$Q_{out/pulse}$	Output charge per pulse (driver)
Q_{rr}	Reverse recovery (recovered) charge
Q_{rrf}	Reverse recovery fall time charge
Q_s	Storage charge
R	Universal gas constant
$R_{CC'+EE'}$	Parasitic ohmic terminal-to-terminal lead resistances (IGBT modules)
r_{CE}	On-state slope resistance (IGBT)
R_{CE}	Resistor for V_{CE} monitoring
R_{clmp}	Resistor included in an active gate clamping circuit
R_{EX}	External emitter resistor (IGBT paralleling)
R_{ESR}	DC-link capacitor series resistance
$R_{DS(on)}$, $r_{DS(on)}$	Drain-source on-resistance (MOSFET)
rec. (120°)	Rectangular current waveform (e.g. 120° conduction angle)
$R_{DD'+SS'}$	Parasitic ohmic terminal-to-terminal lead resistances (MOSFET modules)
R_{EX}	Auxiliary emitter series resistance (paralleled IGBT)
r_F	Forward slope resistance (diode)
R_G	External gate circuit resistance
R_{GE}	External resistance gate-emitter
R_{Gint}	Internal gate resistance (IGBT, MOSFET)
R_{GK}	external resistance gate-cathode
R_{goff}, $R_{goff,min}$	External turn-off gate series resistance, minimum value
R_{gon}, $R_{gon,min}$	External turn-on gate series resistance, minimum value
R_{GS}	external resistance gate-source
RH	Relative humidity
$RH_{storage}$	Relative storage humidity
R_{IN}	Input resistance
R_{iso}	Insulation resistance
R_L	Total load circuit resistance
$R_{min(CL)}$	Minimum series resistance for capacitive load
R_P	Recommended parallel resistance for a series connection of semiconductors
R_p	DC resistance of the primary winding
R_s	DC resistance of each secondary winding
$R_{softcharge}$	Recommended DC-link charge resistance

$R_{(T)}$	Temperature-dependent Resistance (temperature sensor)
r_T	On-state slope resistance (thyristor)
R_{th}	Thermal resistance
$R_{th(c-a)}$	Thermal resistance case to ambient
$R_{th(c-s)}$	thermal resistance case to heat sink
$R_{th(j-a)}$	Thermal resistance junction to ambient
$R_{th(j-c)}$	Thermal resistance junction to case
$R_{th(j-r)}$	Thermal resistance junction to reference point (temperature sensor)
$R_{th(j-s)}$	Thermal resistance junction to heatsink
$R_{th(j-T)}$	Thermal resistance junction to terminal
$R_{th(r-a)}$	Thermal resistance reference point (temperature sensor) to ambient
$R_{th(s-a)}$	Thermal resistance heatsink to ambient
R_{tp}	resistivity of thermal paste
R_{TS}	resistance of a temperature sensor
R_z	Roughness (mounting surface)
ρ	Specific density
S	soft factor (Diode)
SAM	Scanning Acoustic Microscope
SBD	Schottky Barrier Diode
SELV	Safety Extra Low Voltage
sin. (180°)	Sinusoidal current waveform (half-sine waves, 180° conduction angle)
SMPS	Switch-mode power supply
SSC	Single sided cooling
t	Time
t_a	Arcing time (fuse)
T_a	Ambient temperature
Tau, τ	Time constant
T_c	Case temperature
TC	Temperature coefficient, thermal cycling (test)
t_{cond}	Conducting time
$T_{coolant}$	Coolant temperature
$T_{c(op)}$	Case operating temperature
t_d	Delay time
$t_{d(err)}$	Propagation delay time at ERROR (driver)
$t_{d(err)io}$	ERROR input-output propagation delay time (driver)
$t_{d(off)}$	Turn-off delay time
$t_{d(off)io}$	Input-output turn-off propagation delay time (driver)
$t_{d(on)}$	Turn-on delay time
$t_{d(on)io}$	Input-output turn-on propagation delay time (driver)
$T_{DriverTrip}$	PCB overtemperature trip level (SKiiP)
t_f	Current fall time (IGBT, MOSFET)
t_{fr}	Forward recovery time
t_{gd}	Gate controlled delay time (thyristor)
t_{gr}	Gate controlled rise time (thyristor)
t_{hw}	Duration of the half-sine wave for which I_{FSM} [I_{TSM}] has been specified
t_i	Integration time for Q_{rr}
TIM	Thermal interface material
T_j	Junction temperature
T_{jm}	Medium junction temperature
$T_{j(max)}$	Maximum junction temperature
$T_{j(op)}$	Operational junction temperature
$T_{j(op)-ol}$	Maximum junction temperature at limited overload (Gen. 7 IGBT)
$T_{j(op,max)}$	Maximum operational junction temperature
t_{jitter}	jitter clock time
t_{Kc}	Duration of capacitive commutation process (modified ZVS mode)
t_{Ki}	Duration of capacitive commutation process (modified ZCS mode)
$T_{lifetime}$	Service lifetime (insolation)
TNPC	3-level T-type neutral point clamped converter
t_{off}	Turn-off time
t_{on}	Turn-on time
t_{op}	(Total) Operating (clearing) time (fuse)
T_{op}	Operational temperature range

t_p	Pulse duration
T_p	Plateau temperature (wave soldering profile)
t_{pa}	Melting (pre-arcing) time (fuse)
$t_{p(off,IGBT)}$	Effective lead time of freewheeling diode during IGBT off-state
t_{psc}	Turn-on time during short-circuit
t_{pRESET}	Min. pulse width ERROR memory RESET time
$t_{pReset(OCP)}$	Overcurrent reset time (SKiiP)
t_q	Circuit commutated turn-off time (thyristor)
t_{Qn}	dwell times in the quadrants Q_n (3-level topologies)
t_r	Rise time
t_R	Reverse blocking time
T_r	Reference point temperature (temperature sensor)
t_{rr}	Reverse recovery time
t_{rrf}	Reverse recovery fall time
t_s	Storage time
T_s	Heatsink temperature
t_{SC}	Short circuit time
$t_{sc(max)}$	Maximum permissible short circuit time
t_{SIS}	Short-pulse suppression time
T_{sold}	Solder temperature
T_{stg}	Storage temperature
t_{stg}	storage time
t_{TD}	Interlock time
$T_{terminal}$	Terminal temperature
$T_{test\ time}$	Insulation test time
T_{Trip}	Trip level of over temperature protection (SKiiP)
T_{vj}	(Virtual) junction temperature
t_{vpa}	Virtual pre-arcing (melting) time (fuse)
t_z	Tail time (IGBT)
τ_{HL}	high-injection charge carrier lifetime
τ_{eff}	effective charge carrier lifetime
UPS	Uninterruptable power supply
V	Volume
v_{ab}	Line-to-line voltage
V_{air}	Air volume
v_{air}	Air velocity
V_{AK}	Anode-cathode voltage
V_{Alt}	RMS voltage superimposed on the DC output voltage
V_B	No-load voltage of thyristor gate driver
$V_{(BR)}$	Breakdown voltage
$V_{(BR)CES}$	Collector-emitter breakdown voltage, gate-emitter short circuited
$V_{(BR)DSS}$	Drain-source breakdown voltage, gate-source short circuited
V_{cap}	Capacitor voltage
V_{CC}	Collector-emitter supply voltage
V_{CE}	Collector-emitter voltage
$V_{CE(clamp)}$	Collector-emitter clamping voltage during turn-off
$V_{CE(max,T)}$	Highest collector-emitter voltage occurring at the module terminals
V_{CE_peak}	Collector-emitter peak voltage (dynamic gate control)
V_{CE0}	Collector-emitter threshold voltage (IGBT forward characteristic)
V_{CEdyn}	Dynamic threshold voltage for collector-emitter voltage monitoring (driver)
V_{CES}	Maximum collector-emitter voltage with gate-emitter short circuited
V_{CEsat}	Collector-emitter saturation voltage
V_{CEstat}	Static threshold voltage value for collector-emitter voltage monitoring (driver)
$V_{coolant}$	Volume of liquid coolant
V_D	Direct output voltage (bridge rectifier)
V_{DC}	DC link voltage
V_{DCTRIP}	Trip level of DC link voltage monitoring (SKiiP)
V_{DD}	Drain-source supply voltage (MOSFET), direct off-state voltage (thyristor)
V_{diff}	Diffusion voltage at the pn-junction
V_{drift}	Drift voltage at the pn-junction
V_{DGR}	Drain-gate voltage with specified input resistance
V_{DRM}	Repetitive peak off-state voltage

V_{DS}	Drain-source voltage
V_{DSon}	Drain-source on-state voltage
$V_{DS(max,T)}$	Maximum drain-source voltage at the module terminals
V_{DSS}	Maximum drain-source voltage, gate-source short circuited
V_{DWM}	Crest (peak) working off-state voltage
V_{EC}	Emitter-collector voltage
V_F, v_F	Forward voltage
V_{F0}	Forward threshold voltage (diode)
V_{Fan}	Operating voltage fan
v_{fluid}	Cooling fluid volume per unit time
V_{GD}	Gate non-trigger voltage
V_{GE}	Gate-emitter voltage
$V_{GE(off)}$	Gate-emitter turn-off control voltage
$V_{GE(on)}$	Gate-emitter turn-on control voltage
$V_{GE(pl)}$	Gate-emitter plateau voltage
$V_{GE(th)}$	Gate-emitter threshold voltage
V_{GES}	Gate-emitter voltage, collector-emitter short-circuited
V_{GG}	Gate driver output stage supply voltage
V_{GK}	Gate-cathode voltage
V_{GS}	Gate-source voltage
$V_{GS(off)}$	Gate-source turn-off control voltage
$V_{GS(on)}$	Gate-source turn-on control voltage
$V_{GS(th)}$	Gate-source threshold voltage
V_{GSS}	Gate-source voltage, drain-source short circuited
V_{GT}	Gate trigger voltage
V_{iH}	Input HIGH signal voltage (driver, SKiiP)
V_{in}	Input voltage
V_{isol}	Insulation test voltage (RMS)
V_{isolPD}	Partial discharge extinction voltage
V_{iT-}, V_{iT+}	Input threshold voltage (LOW) max., (HIGH) min. (driver, SKiiP)
$V_{iT-HALT}$, $V_{iT+HALT}$	Input threshold voltage LOW HALT (HALT->LOW), HIGH HALT (LOW ->High (SKiiP 4)
$V_{L\sigma}$	Inductive voltage across the parasitic stray inductance (IGBT, MOSFET)
V_M	Peak pulse voltage
V_n	Rated AC voltage (fuse)
V_{nom}	Rated Voltage (pulse transformer)
$V_{operating\ voltage}$	Operating voltage (Insulation)
V_{oH}, V_{oL}	Logic HIGH output voltage, logic LOW output voltage (driver)
V_{out}	Output voltage
V_R	(Direct) reverse voltage
V_{RD}	Direct reverse voltage
V_{RGM}	Peak reverse gate voltage
V_{RGO}	No-load reverse gate voltage
V_{RRM}	Repetitive peak reverse voltage
V_{RSM}	Non-repetitive peak reverse voltage
V_{RWM}	Crest (peak) working reverse voltage
v_s	(Monitored) switch voltage (ZVS mode)
V_S	Primary side supply voltage (driver)
V_{SD}	Source-drain voltage (inverse diode forward voltage)
VSI	Voltage source inverter
V_T, v_T	On-state voltage (thyistor)
$V_{(TO)}$	Threshold voltage (thyristor, on state)
V_V, V_{VRMS}	RMS supply voltage (Line-Line or Line-Neutral)
v_w	Water volume per unit time
V_w	Water volume
V_Z	DC-link voltage
w	Weight
W_{max}	Maximum energy absorption (varistor)
w_B	Base width (semiconductor)
w_h	Heatsink weight (SKiiP)
W1C	Single phase AC controller connection
W3C	Three phase AC controller connection

Z_{th}	Transient thermal impedance
$Z_{th(c-a)}$	Transient thermal impedance case to ambient
$Z_{th(j-c)}$	Transient thermal impedance junction to case
$Z_{th(j-s)}$	Transient thermal impedance junction to heat sink
$Z_{th(r-a)}$	Transient thermal impedance reference (sensor) to ambient
$Z_{th(s-a)}$	Transient thermal impedance heat sink to ambient
ZCS	Zero current switching
ZVS	Zero voltage switching

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Application Manual Power Semiconductors

Today, IGBT and power MOSFET modules are instrumental in power electronic systems and are increasingly gaining ground in new fields. This goes hand in hand with the ever increasing need for rectifier diodes and thyristors as cost-efficient means of connecting to the power supply grid. This application manual is intended to assist users with component selection and application. This manual contains basic explanations and background information on semiconductor physics where needed to provide a better understanding of the application possibilities and limits. A larger section of the manual contains descriptions of different packaging technologies, examining the different impacts on module properties and ratings in field applications. This section is rounded off with statements on component reliability and service life, as well as the relevant test procedures.

The manual also explains the structure of data sheets and provides useful tips on how to interpret data sheet specifications. An important focus of the manual is the examination of application-specific aspects which must be taken into account in component selection and application. This includes, for example, electric circuits for the most important operating scenarios, driver technology and component protection, thermal dimensioning and heat sink solutions, notes on parallel and series circuits, notes on optimum power layouts with regard to parasitic elements, as well as requirements associated with certain ambient conditions.

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09/2025

230B7224